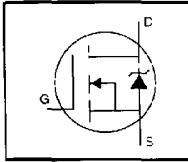


**HEXFET® Power MOSFET**

- Ultra Low Gate Charge
- Reduced Gate Drive Requirement
- Enhanced 30V V<sub>GS</sub> Rating
- Reduced C<sub>iss</sub>, C<sub>oss</sub>, C<sub>rss</sub>
- Extremely High Frequency Operation
- Repetitive Avalanche Rated



$V_{DSS} = 600V$

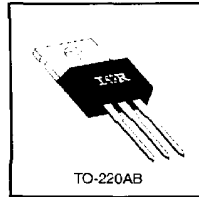
$R_{DS(on)} = 1.2\Omega$

$I_D = 6.2A$

**Description**

This new series of Low Charge HEXFETs achieve significantly lower gate charge over conventional MOSFETs. Utilizing the new LCDMOS technology, the device improvements are achieved without added product cost, allowing for reduced gate drive requirements and total system savings. In addition, reduced switching losses and improved efficiency are achievable in a variety of high frequency applications. Frequencies of a few MHz at high current are possible using the new Low Charge MOSFETs.

These device improvements combined with the proven ruggedness and reliability that are characteristic of HEXFETs offer the designer a new standard in power transistors for switching applications.



**Absolute Maximum Ratings**

Parameter	Max.	Units
$I_C$ @ $T_C = 25^\circ C$	6.2	A
Continuous Drain Current, $V_{GS} @ 10 V$		
$I_D$ @ $T_C = 100^\circ C$	3.9	
Continuous Drain Current, $V_{GS} @ 10 V$		
$I_{DM}$	25	
Pulsed Drain Current (1)		
$P_D$ @ $T_C = 25^\circ C$	125	W
Power Dissipation		
Linear Derating Factor	1.0	W/°C
$V_{GS}$	±30	V
Gate-to-Source Voltage		
$E_{AS}$	530	mJ
Single Pulse Avalanche Energy (2)		
$I_{AR}$	6.2	A
Avalanche Current (1)		
$E_{AR}$	13	mJ
Repetitive Avalanche Energy (2)		
$dv/dt$	3.0	V/ns
Peak Diode Recovery $dv/dt$ (3)		
$T_J$	-55 to -150	°C
Operating Junction and Storage Temperature Range		
$T_{STG}$		
Soldering Temperature, for 10 seconds	300 (1.8mm) from case)	
Mounting Torque, 6-32 or M3 screw	10 lbf·in (1.1 N·m)	

**Thermal Resistance**

Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	—	—	1.0	°C/W
Junction-to-Case				
$R_{\theta CS}$	—	0.50	—	
Case-to-Sink, Flat, Greased Surface				
$R_{\theta JA}$	—	—	62	
Junction-to-Ambient				

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## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions
V <sub>BR(DSS)</sub>	600	—	—	V	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA
ΔV <sub>BR(DSS)/ΔT<sub>J</sub></sub>	—	0.70	—	V/°C	Reference to 25°C, I <sub>D</sub> =1mA
R <sub>DS(on)</sub>	—	—	1.2	Ω	V <sub>GS</sub> =10V, I <sub>D</sub> =3.7A ④
V <sub>GS(th)</sub>	2.0	—	4.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA
g <sub>fs</sub>	3.7	—	—	S	V <sub>DS</sub> =100V, I <sub>D</sub> =3.7A ④
I <sub>DSS</sub>	—	—	100	μA	V <sub>DS</sub> =600V, V <sub>GS</sub> =0V
I <sub>GSS</sub>	—	—	100	nA	V <sub>GS</sub> =20V
I <sub>SS</sub>	—	—	100	nA	V <sub>DS</sub> =480V, V <sub>GS</sub> =0V, T <sub>J</sub> =125°C
Q <sub>g</sub>	—	—	39	nC	I <sub>D</sub> =6.2A
Q <sub>gs</sub>	—	—	10	nC	V <sub>DS</sub> =360V
Q <sub>gd</sub>	—	—	9	nC	V <sub>GS</sub> =10V See Fig. 6 and 13 ③
t <sub>d(on)</sub>	—	12	—	ns	V <sub>DD</sub> =30CV
t <sub>r</sub>	—	20	—	ns	I <sub>D</sub> =6.2A
t <sub>d(off)</sub>	—	27	—	ns	R <sub>G</sub> =9.1Ω
t <sub>f</sub>	—	17	—	ns	R <sub>D</sub> =471Ω See Figure 10 ③
L <sub>D</sub>	—	4.5	—	nH	Between lead, 6 mm (0.25in.) from package and center of die contact
L <sub>S</sub>	—	7.5	—	nH	
C <sub>iss</sub>	—	1100	—	pF	V <sub>GS</sub> =0V
C <sub>oss</sub>	—	140	—	pF	V <sub>DS</sub> =25V
C <sub>rss</sub>	—	15	—	pF	f=1.0MHz See Figure 5



## Source-Drain Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I <sub>S</sub>	—	—	6.2	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	—	—	25	A	
V <sub>SD</sub>	—	—	1.5	V	T <sub>J</sub> =25°C, I <sub>S</sub> =6.2A, V <sub>GS</sub> =0V ④
t <sub>r</sub>	—	440	680	ns	T <sub>J</sub> =25°C, I <sub>F</sub> =6.2A
Q <sub>rr</sub>	—	2.1	3.2	μC	dI/dt=100A/μs ④
t <sub>on</sub>	—	—	—	ns	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )

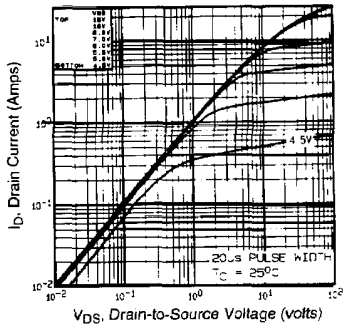
### Notes:

① Repetitive rating; pulse width limited by max. junction temperature (See Figure 11)

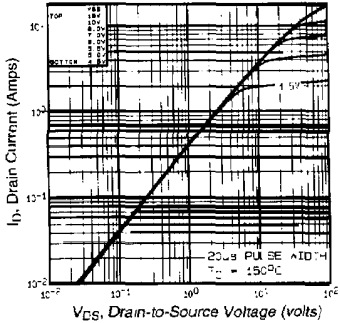
② V<sub>DD</sub>=50V, starting T<sub>J</sub>=25°C, L=25mH  
R<sub>G</sub>=25Ω, I<sub>AS</sub>=6.2A (See Figure 12)

③ I<sub>SD</sub>≤6.2A, dI/dt≤80A/μs, V<sub>DD</sub>≤V<sub>BR(DSS)</sub>,  
T<sub>J</sub>≤150°C

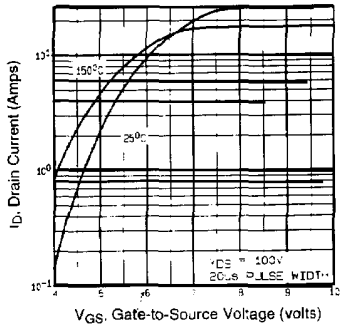
④ Pulse width ≤ 300 μs; duty cycle ≤2%



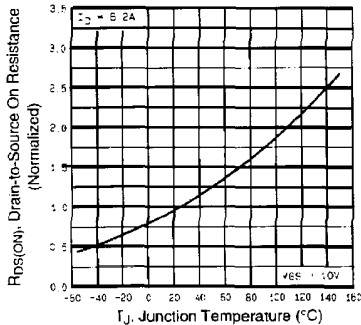
**Fig 1.** Typical Output Characteristics.  
 $T_C=25^\circ\text{C}$



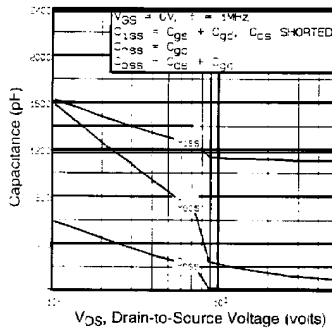
**Fig 2.** Typical Output Characteristics.  
 $T_C=150^\circ\text{C}$



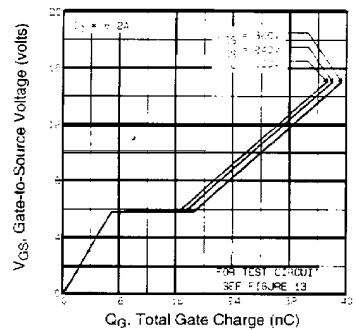
**Fig 3.** Typical Transfer Characteristics



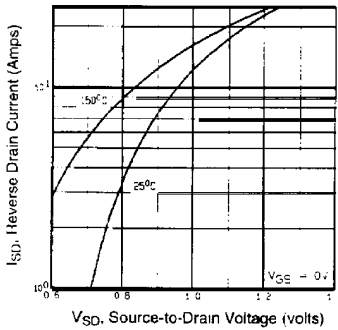
**Fig 4.** Normalized On-Resistance  
 Vs. Temperature



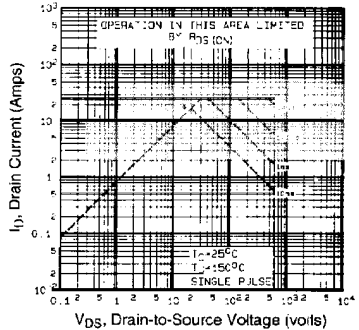
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



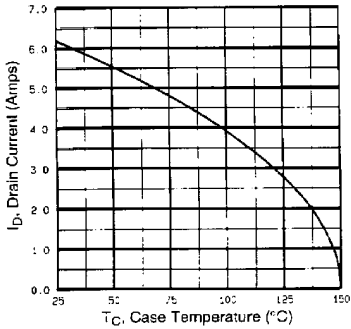
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



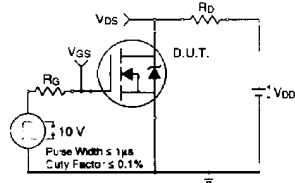
**Fig 7.** Typical Source-Drain Diode Forward Voltage



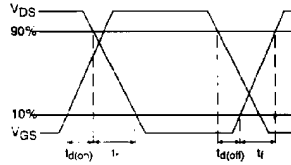
**Fig 8.** Maximum Safe Operating Area



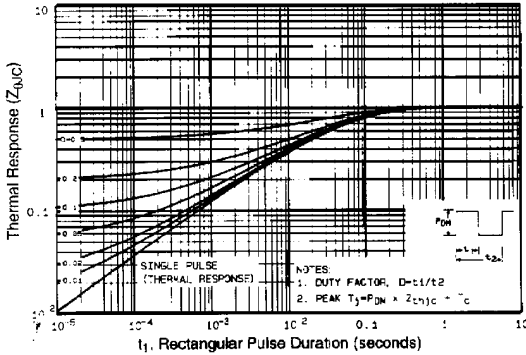
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

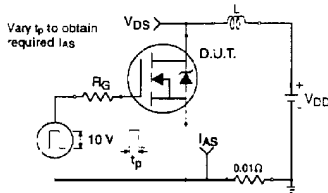


**Fig 10b.** Switching Time Waveforms

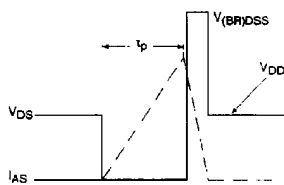


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

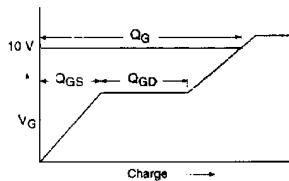
# IRFBC40LC



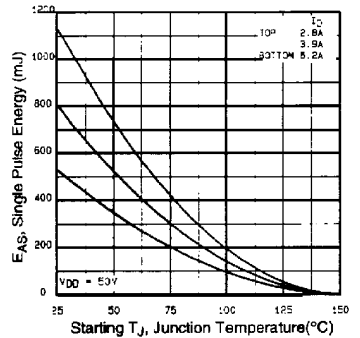
**Fig 12a.** Unclamped Inductive Test Circuit



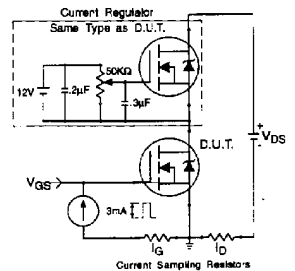
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

**Appendix A:** Figure 14, Peak Diode Recovery  $dv/dt$  Test Circuit

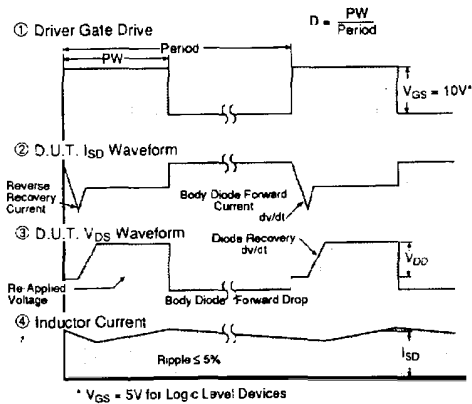
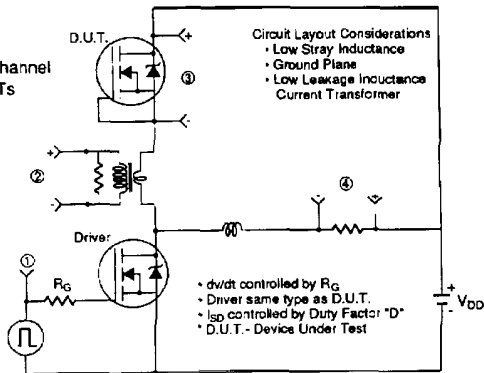
**Appendix B:** Package Outline Mechanical Drawing

**Appendix C:** Part Marking Information

# Appendix A

## Peak Diode Recovery $dv/dt$ Test Circuit

**Fig 14.** For N-Channel HEXFETs



# IRFBC40LC

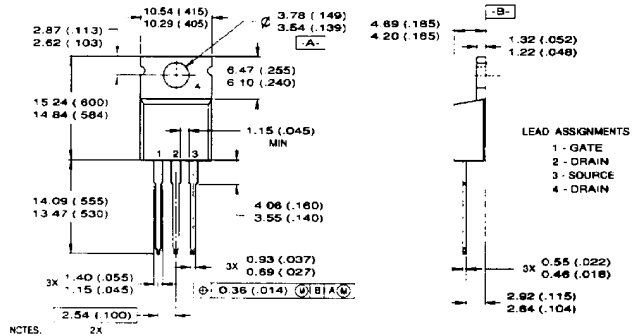


## Package Outline

## Appendix B

### TO-220AB Outline

Dimensions are shown in millimeters (inches)



- LEAD ASSIGNMENTS
- 1 - GATE
  - 2 - DRAIN
  - 3 - SOURCE
  - 4 - DRAIN

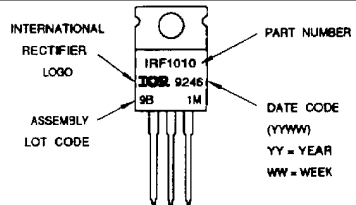
- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M 1982
  - 2 CONTROLLING DIMENSION INCH
  - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220-AB
  - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## Part Marking Information

## Appendix C

### TO-220AB

EXAMPLE: THIS IS AN IRF1010 WITH  
ASSEMBLY LOT CODE 9B1M



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