International
IOR Rectifier

SMPS MOSFET

IRFBL3703

HEXFET® Power MOSFET

Applications

- Synchronous Rectification in High Power High Frequency DC/DC Converters

V_{DSS}	$R_{DS(on)}$ max	I_D
30V	**0.0025Ω**	**260A** ⑥

Benefits

- >1mm lower profile than D^2Pak
- Same footprint as D^2Pak
- Low Gate Impedance to Reduce Switching Losses
- Ultra Low On-Resistance
- Fully Avalanche Rated

Super-D^2Pak™

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	260 ⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	180 ⑥	
I_{DM}	Pulsed Drain Current ①	1000	
P_D @T_C = 25°C	Power Dissipation	300	W
P_D @T_A = 25°C	Power Dissipation	3.8	
	Linear Derating Factor	2.0	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Typical SMPS Topologies

- Forward and Bridge Converters with Synchronous Rectification for Telecom and Industrial Applications

Notes ① through ⑥ are on page 8

4/5/00

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.028	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	2.0	2.5	mΩ	V_{GS} = 10V, I_D = 76A ④
		——	2.5	3.6		V_{GS} = 7.0V, I_D = 76A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 24V, V_{GS} = 0V
		——	——	250		V_{DS} = 24V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -20V

Dynamic @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	150	——	——	S	V_{DS} = 24V, I_D = 76A
Q_g	Total Gate Charge	——	209	——	nC	I_D = 76A
Q_{gs}	Gate-to-Source Charge	——	62	——		V_{DS} = 24V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	42	——		V_{GS} = 10V, ④
$t_{d(on)}$	Turn-On Delay Time	——	18	——	ns	V_{DD} = 15V, V_{GS} = 10V
t_r	Rise Time	——	123	——		I_D = 76A
$t_{d(off)}$	Turn-Off Delay Time	——	53	——		R_G = 1.8Ω
t_f	Fall Time	——	24	——		V_{GS} = 10V ④
C_{iss}	Input Capacitance	——	8250	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	3000	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	290	——		f = 1.0MHz
C_{oss}	Output Capacitance	——	10360	——		V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz
C_{oss}	Output Capacitance	——	3060	——		V_{GS} = 0V, V_{DS} = 24V, f = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	——	2590	——		V_{GS} = 0V, V_{DS} = 0V to 24V ⑤

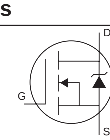
Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	1700	mJ
I_{AR}	Avalanche Current①	——	76	A
E_{AR}	Repetitive Avalanche Energy①	——	30	mJ

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.5	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	40	

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	260⑥	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	1000		
V_{SD}	Diode Forward Voltage	——	0.8	1.3	V	T_J = 25°C, I_S = 76A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	80	120	ns	T_J = 25°C, I_F = 76A, V_{DS} = 16V
Q_{rr}	Reverse RecoveryCharge	——	185	275	nC	di/dt = 100A/µs ④

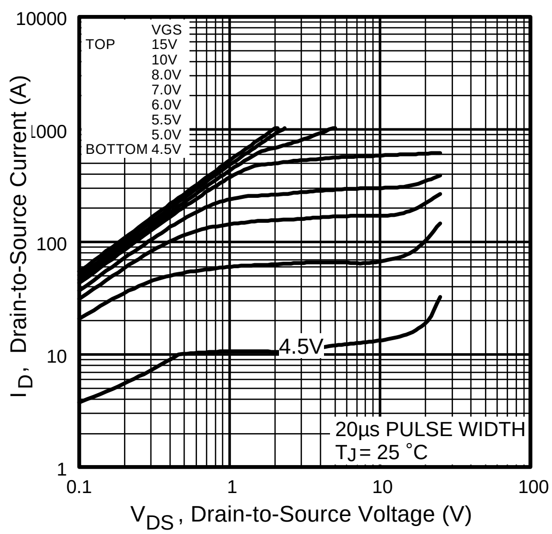


Fig 1. Typical Output Characteristics

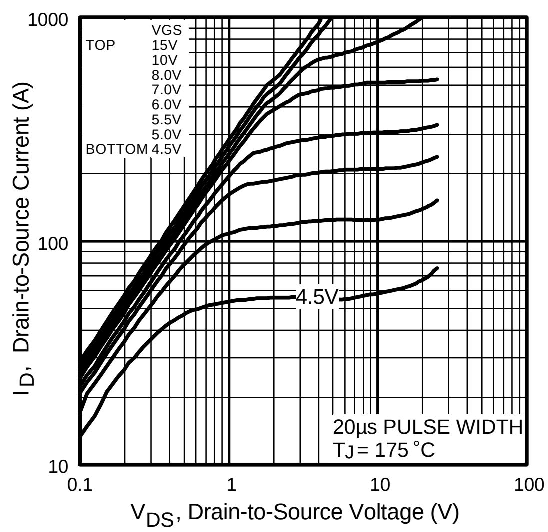


Fig 2. Typical Output Characteristics

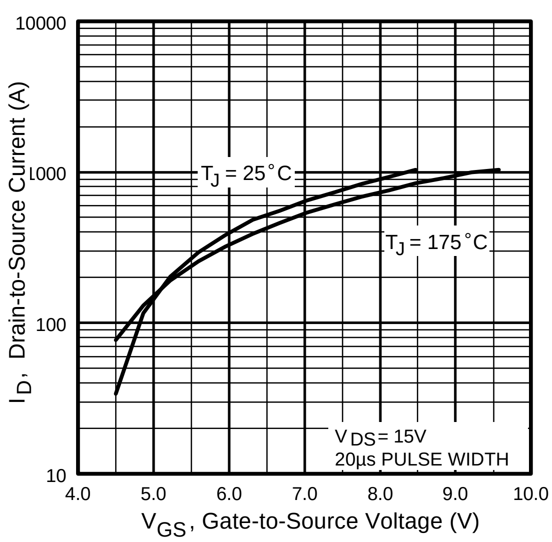


Fig 3. Typical Transfer Characteristics

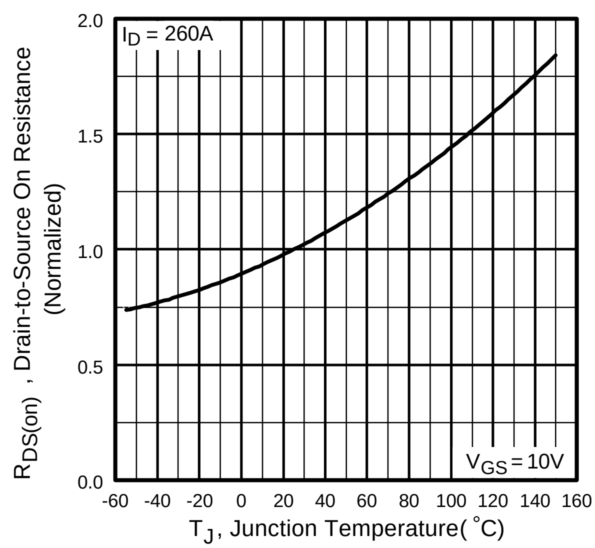


Fig 4. Normalized On-Resistance Vs. Temperature

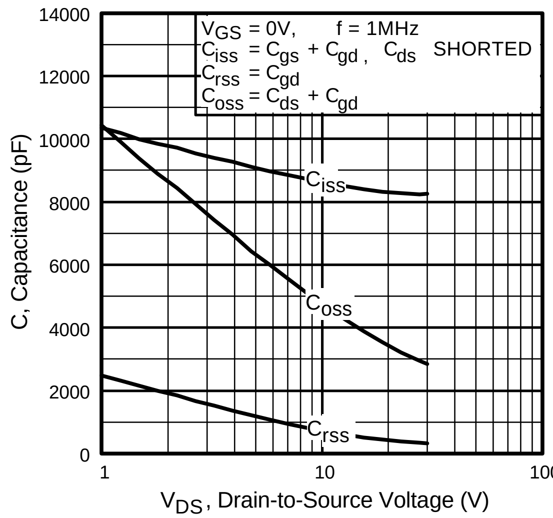


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

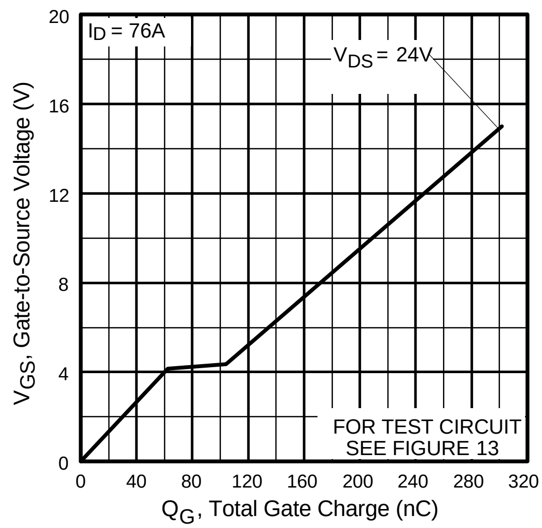


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

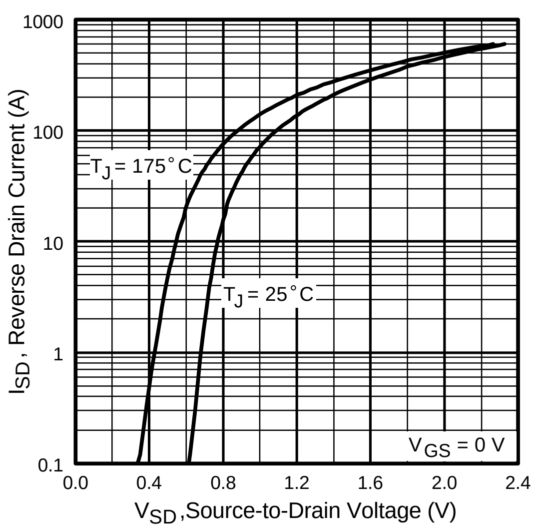


Fig 7. Typical Source-Drain Diode Forward Voltage

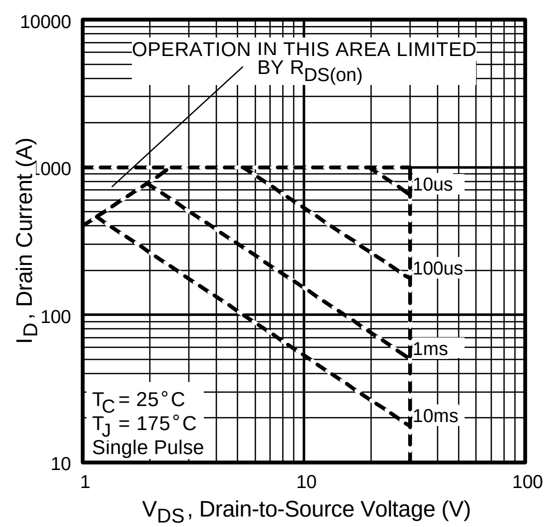


Fig 8. Maximum Safe Operating Area

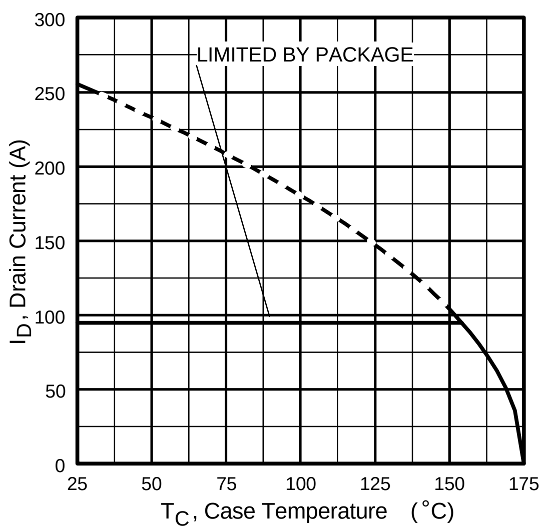


Fig 9. Maximum Drain Current Vs. Case Temperature

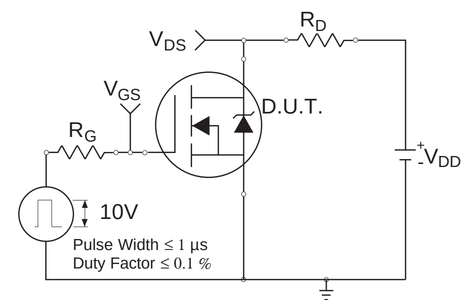


Fig 10a. Switching Time Test Circuit

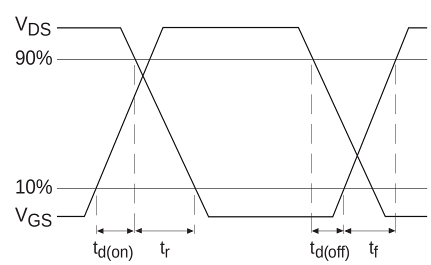


Fig 10b. Switching Time Waveforms

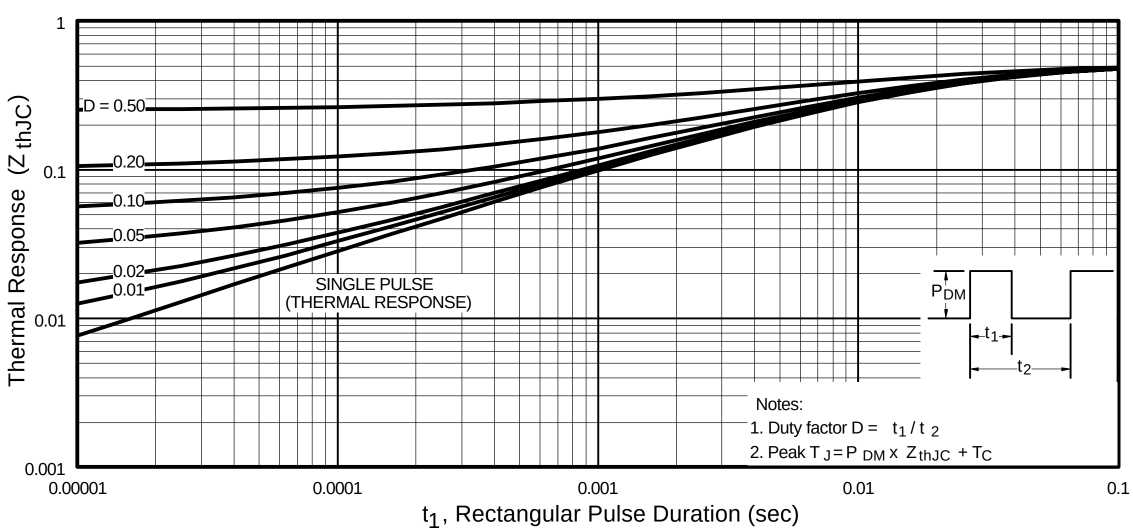


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

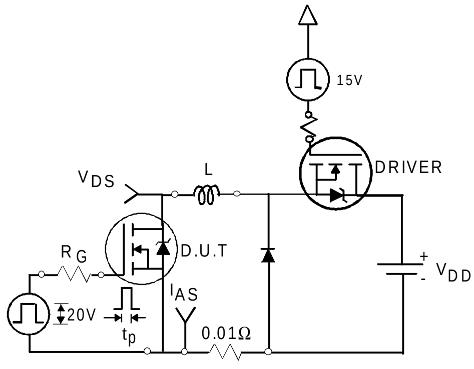


Fig 12a. Unclamped Inductive Test Circuit

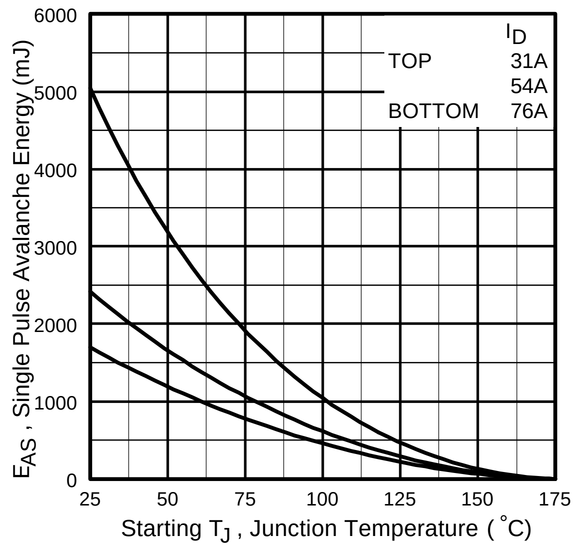


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

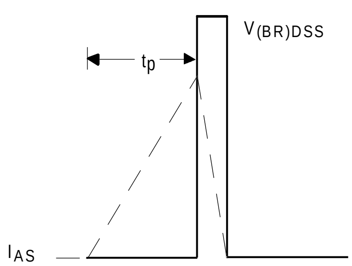


Fig 12b. Unclamped Inductive Waveforms

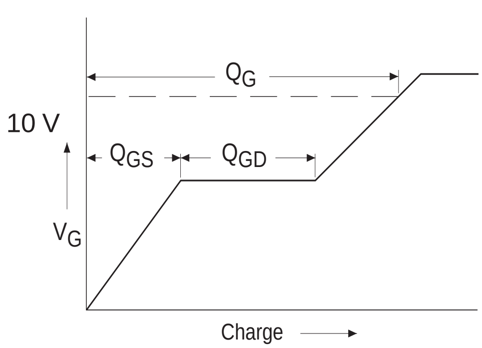


Fig 13a. Basic Gate Charge Waveform

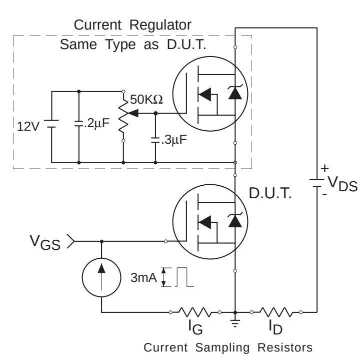
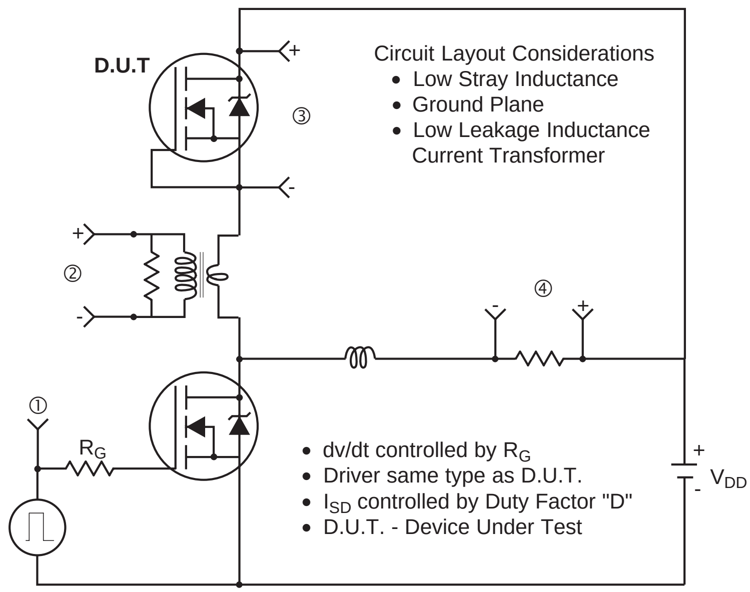
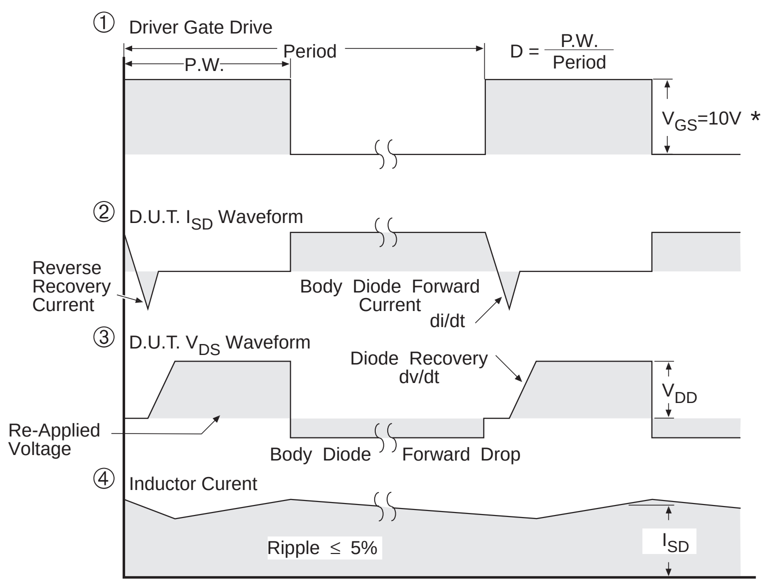


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



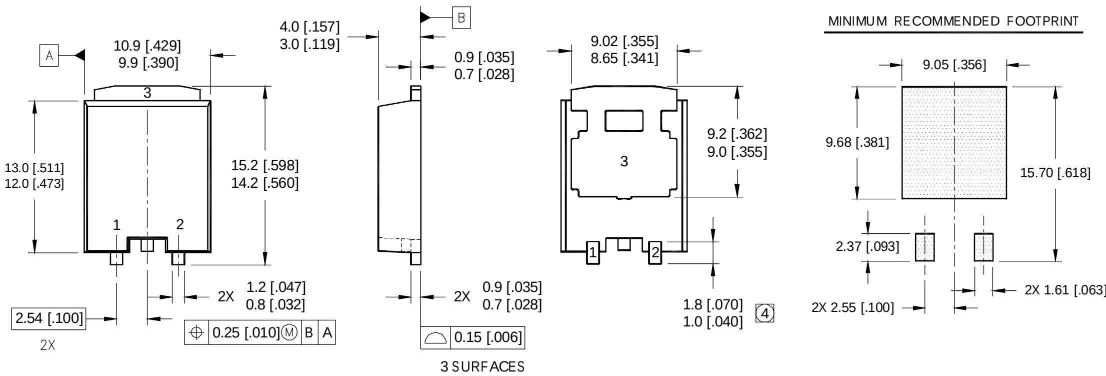


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFET

Super-D^{2}Pak^{TM} Package Outline

Dimensions are shown in millimeters (inches)



NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: MILLIMETER.
4. DIMENSION IS MEASURED AT FULL LEAD WIDTH.

LEAD ASSIGNMENTS

MOSFET	SCHOTTKY / FRED
1 = GATE	1 = ANODE 1
2 = SOURCE	2 = ANODE 2
3 = DRAIN	3 = COMMON CATHODE

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, L = 0.6mH $R_G = 25\Omega$, $I_{AS} = 76A$.

③ $I_{SD} \leq 76A$, di/dt $\leq$ 100A/µs, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 175°C$

④ Pulse width $\leq$ 300µs; duty cycle $\leq$ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}

⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A

International
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IR ITALY: Via Liguria 49, 10071 Borgaro, Torino Tel: ++ 39 011 451 0111
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