



TECHNICAL DATA SHEET

DATA SHEET NO. 1001A

August 1988

## High Voltage Power MOSFET Die

N-Channel Enhancement Mode High Ruggedness Series

The following device types use the IRFC150:

2N6764  
2N6763  
IRF150/IRFP150  
IRF151/IRFP151  
IRF152/IRFP152  
IRF153/IRFP153

### FEATURES:

- Fast switching times
- Low  $R_{DS(on)}$  HDMOS™ process
- Rugged polysilicon gate cell structure
- Excellent high voltage stability
- Low input capacitance
- Improved high temperature reliability

### APPLICATIONS:

- Switching power supplies
- Motor controls
- Audio Amplifiers
- Inverters
- Choppers

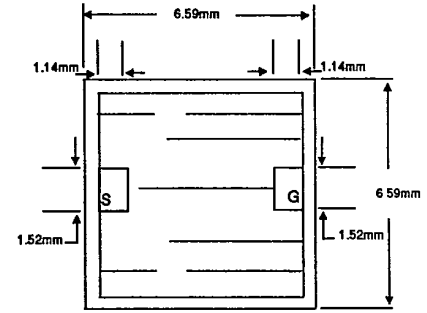
## IRFC150

$V_{(BR)DSS}$  ..... 100V  
 $R_{DS(on)}$  ..... 0.055 $\Omega$

## Die Topography

Notes:

1. Top Metal 3  $\mu$ m Aluminum
2. Back Metal Ni/V, with Au
3. Die thickness 420  $\pm$  10  $\mu$ m



### ELECTRICAL CHARACTERISTICS: (TA=25 °C unless otherwise specified)

| CHARACTERISTIC                    | TEST CONDITIONS  | SYMBOL        | MIN | TYP | MAX       | UNITS         |
|-----------------------------------|--|---------------|-----|-----|-----------|---------------|
| Drain-Source Breakdown Voltage    | $V_{GS} = 0\text{ V}$ , $I_D = 250\ \mu\text{A}$   | $V_{(BR)DSS}$ | 100 | —   | —         | V             |
| Gate Threshold Voltage            | $V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$   | $V_{GS(th)}$  | 2.0 | —   | 4.0       | V             |
| Gate-Source Leakage Current       | $V_{GS} = \pm 20\text{ V}_{DC}$  | $I_{GSS}$     | —   | —   | $\pm 100$ | nA            |
| Zero Gate Voltage Drain Current   | $V_{DS} = V_{(BR)DSS} \times 0.8$ , $V_{GS} = 0\text{ V}$<br>$T_C = 25^\circ\text{C}$<br>$T_C = 125^\circ\text{C}$ | $I_{DSS}$     | —   | —   | 250       | $\mu\text{A}$ |
|                                   |  | $I_{DSS}$     | —   | —   | 1000      | $\mu\text{A}$ |
| Static Drain-Source On-Resistance | $V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$   | $R_{DS(ON)}$  | —   | —   | 0.055     | $\Omega$      |
| Ciss Input Capacitance            | $V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$  | Ciss          | —   | —   | 3000      | pF            |
| Coss Output Capacitance           | Pulse Test: Pulse width $\leq 300\text{ms}$ , duty cycle $\leq 2\%$  | Coss          | —   | —   | 1500      | pF            |
| Crss Reverse Transfer Capacitance |  | Crss          | —   | —   | 500       | pF            |

### NOTES:

1.  $I_D$  based on  $R_{thJC} = 0.83\ ^\circ\text{C/W}$
2. ASSEMBLY RECOMMENDATIONS:
  - a) 10 mil Gate and 15 mil Source wires
  - b) Drain mounted with 92.5/5/2.5% Lead/Indium/Silver solder, or 95/5% Lead/tin solder
3. Devices shipped in ESD protected waffle packs with a maximum of 25 die per waffle pack.
4. Die should be handled and assembled in clean room environment.
5. Die should be stored in inert atmosphere (1 atmosphere  $\text{N}_2$ )

IXYS Corporation reserves the right to change limits, test conditions, and dimensions without notice.

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