



# High Voltage Power MOSFET Die

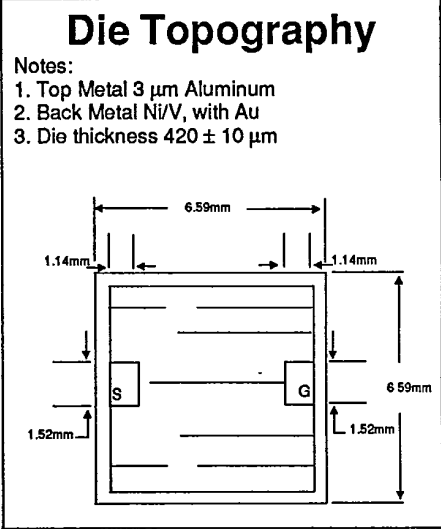
N-Channel Enhancement Mode High Ruggedness Series

IRFC250

$V_{(BR)DSS}$  ..... 200V  
 $R_{DS(on)}$  ..... 0.085 $\Omega$

**The following device types use the IRFC250:**

- |                |                |
|----------------|----------------|
| 2N6766         | IRF254/IRFP254 |
| 2N6765         |                |
| IRF250/IRFP250 |                |
| IRF251/IRFP251 |                |
| IRF252/IRFP252 |                |
| IRF253/IRFP253 |                |



**FEATURES:**

**APPLICATIONS:**

- |  |   |
|--|---|
| <ul style="list-style-type: none"> <li>• Fast switching times</li> <li>• Low <math>R_{DS(on)}</math> HDMOS™ process</li> <li>• Rugged polysilicon gate cell structure</li> <li>• Excellent high voltage stability</li> <li>• Low input capacitance</li> <li>• Improved high temperature reliability</li> </ul> | <ul style="list-style-type: none"> <li>• Switching power supplies</li> <li>• Motor controls</li> <li>• Audio Amplifiers</li> <li>• Inverters</li> <li>• Choppers</li> </ul> |
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**ELECTRICAL CHARACTERISTICS:** (TA=25 °C unless otherwise specified)

CHARACTERISTIC	TEST CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Drain-Source Breakdown Voltage	$V_{GS} = 0 V, I_D = 250 \mu A$	$V_{(BR)DSS}$	200	---	---	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	$V_{GS(th)}$	2.0	---	4.0	V
Gate-Source Leakage Current	$V_{GS} = \pm 20 V_{bc}$	$I_{GSS}$	---	---	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS} = V_{(BR)DSS} \times 0.8, V_{GS} = 0 V$	$T_C = 25^\circ C$	---	---	250	$\mu A$
		$T_C = 125^\circ C$	---	---	1000	$\mu A$
Static Drain-Source On-Resistance	$V_{GS} = 10 V, I_D = 15 A$	$R_{DS(ON)}$	---	---	0.085	$\Omega$
Ciss Input Capacitance	$V_{GS} = 0V, V_{DS} = 25 V, f = 1.0 MHz$	Ciss	---	---	3000	pF
Coss Output Capacitance	Pulse Test: Pulse width $\leq 300ms$ , duty cycle $\leq 2\%$	Coss	---	---	650	pF
Crss Reverse Transfer Capacitance		Crss	---	---	300	pF

**NOTES:**

1.  $I_D$  based on  $R_{thJC} = 0.83 \text{ }^\circ C/W$
2. ASSEMBLY RECOMMENDATIONS:
  - a) 10 mil Gate and 15 mil Source wires
  - b) Drain mounted with 92.5/5/2.5% Lead/Indium/Silver solder, or 95/5% Lead/tin solder
3. Devices shipped in ESD protected waffle packs with a maximum of 25 die per waffle pack.
4. Die should be handled and assembled in clean room environment.
5. Die should be stored in inert atmosphere (1 atmosphere N<sub>2</sub>)

IXYS Corporation reserves the right to change limits, test conditions, and dimensions without notice.