PD - 93857B

International
IOR Rectifier

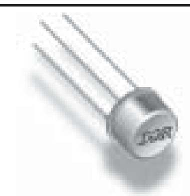
IRHF57230SE
JANSR2N7498T2

RADIATION HARDENED POWER MOSFET THRU-HOLE (TO-39)

200V, N CHANNEL
REF:MIL-PRF-19500/706
R5[TM] TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D	QPL Part Number
IRHF57230SE	100K Rads (Si)	0.24Ω	7.0A	JANSR2N7498T2


TO-39

International Rectifier's R5[TM] technology provides high performance power MOSFETs for space applications. These devices have been characterized for Single Event Effects (SEE) with useful performance up to an LET of 80 (MeV/(mg/cm^2)). The combination of low $R_{DS(on)}$ and low gate charge reduces the power losses in switching applications such as DC to DC converters and motor control. These devices retain all of the well established advantages of MOSFETs such as voltage control, fast switching, ease of paralleling and temperature stability of electrical parameters.

Features:
- Single Event Effect (SEE) Hardened
- Ultra Low $R_{DS(on)}$
- Neutron Tolerant
- Identical Pre- and Post-Electrical Test Conditions
- Repetitive Avalanche Ratings
- Dynamic dv/dt Ratings
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 12V, T_C = 25°C	Continuous Drain Current	7.0	A
I_D @ V_{GS} = 12V, T_C = 100°C	Continuous Drain Current	4.5	
I_{DM}	Pulsed Drain Current ①	28	
P_D @ T_C = 25°C	Max. Power Dissipation	25	W
	Linear Derating Factor	0.2	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	130	mJ
I_{AR}	Avalanche Current ①	7.0	A
E_{AR}	Repetitive Avalanche Energy ①	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	4.2	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.063 in./1.6mm from case for 10s)	
	Weight	0.98 (Typical)	g

For footnotes refer to the last page

09/10/03

Electrical Characteristics @ Tj = 25°C (Unless Otherwise Specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	—	V	V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.26	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.24	Ω	V_{GS} = 12V, I_D = 4.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.5	—	4.5	V	$V_{DS} = V_{GS}$, I_D = 1.0mA
g_{fs}	Forward Transconductance	4.2	—	—	S (Ω)	V_{DS} > 15V, I_{DS} = 4.5A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	10	µA	V_{DS}= 160V ,V_{GS}=0V
		—	—	25		V_{DS} = 160V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	47	nC	V_{GS} =12V, I_D = 7.0A
Q_{gs}	Gate-to-Source Charge	—	—	12		V_{DS} = 100V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	16		
$t_{d(on)}$	Turn-On Delay Time	—	—	25	ns	V_{DD} = 100V, I_D = 7.0A
t_r	Rise Time	—	—	100		V_{GS} =12V, R_G = 7.5Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		
t_f	Fall Time	—	—	40		
$L_S + L_D$	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm /0.25in. from package) to Source lead (6mm /0.25in. from package) with Source wires internally bonded from Source Pin to Drain Pad
C_{iss}	Input Capacitance	—	1014	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	182	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	8.8	—		

Source-Drain Diode Ratings and Characteristics

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	7.0	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	28		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_j = 25°C, I_S = 7.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	274	ns	T_j = 25°C, I_F = 7.0A, di/dt ≤ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	2.2	µC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJC}	Junction-to-Case	—	—	5.0	°C/W	
R_{thJA}	Junction-to-Ambient	—	175	—		Typical socket mount

Note: Corresponding Spice and Saber models are available on the Internationl Rectifier Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	100K Rads (Si) Min	Max	Units	Test Conditions ⑧
BV_{DSS}	Drain-to-Source Breakdown Voltage	200	—	V	V_{GS} = 0V, I_D = 1.0mA
$V_{GS(th)}$	Gate Threshold Voltage	2.0	4.5		$V_{GS} = V_{DS}$, I_D = 1.0mA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 20V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -20V
I_{DSS}	Zero Gate Voltage Drain Current	—	10	µA	V_{DS}= 160V, V_{GS}=0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-3)	—	0.222	Ω	V_{GS} = 12V, I_D = 4.5A
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.24	Ω	V_{GS} = 12V, I_D = 4.5A
V_{SD}	Diode Forward Voltage ④	—	1.5	V	V_{GS} = 0V, I_D = 7.0A

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Single Event Effect Safe Operating Area

Ion	LET MeV/(mg/cm²))	Energy (MeV)	Range (µm)	V_{DS} (V) @V_{GS}=0V	@V_{GS}=-5V	@V_{GS}=-10V	@V_{GS}=-15V	@V_{GS}=-20V
Br	36.7	309	39.5	200	200	200	200	200
I	59.8	341	32.5	200	200	200	185	120
Au	82.3	350	28.4	200	200	150	50	25

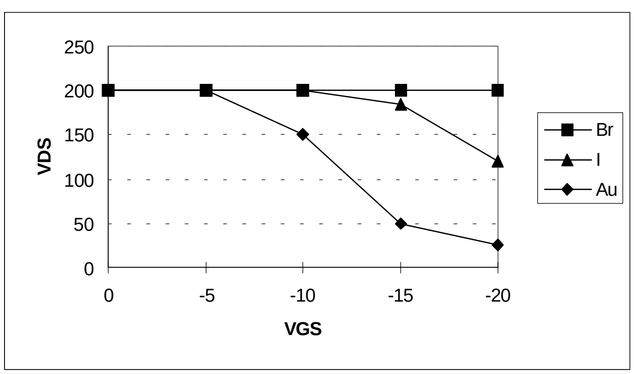


Fig a. Single Event Effect, Safe Operating Area

For footnotes refer to the last page

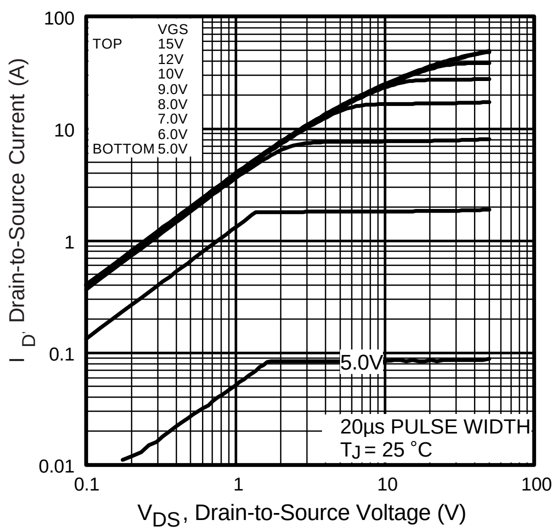


Fig 1. Typical Output Characteristics

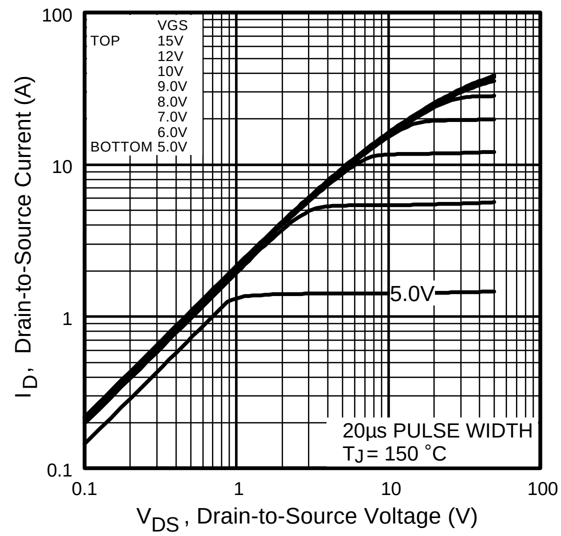


Fig 2. Typical Output Characteristics

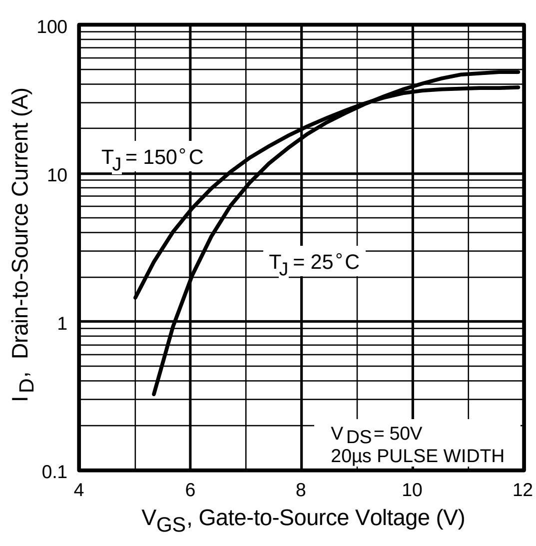


Fig 3. Typical Transfer Characteristics

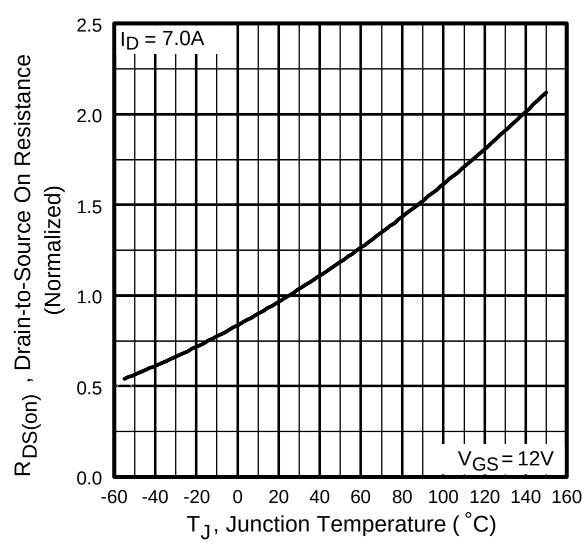


Fig 4. Normalized On-Resistance Vs. Temperature

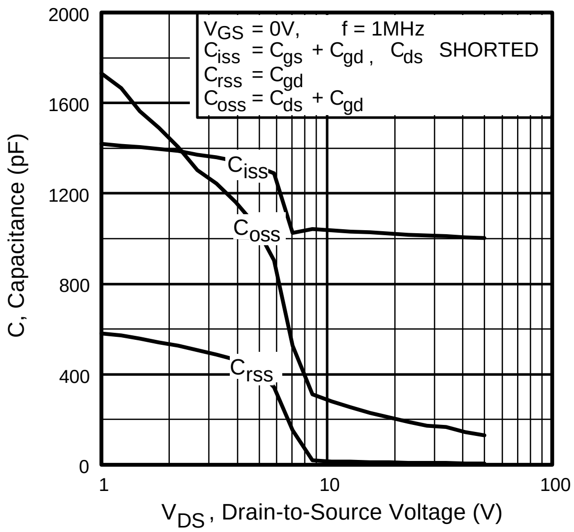


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

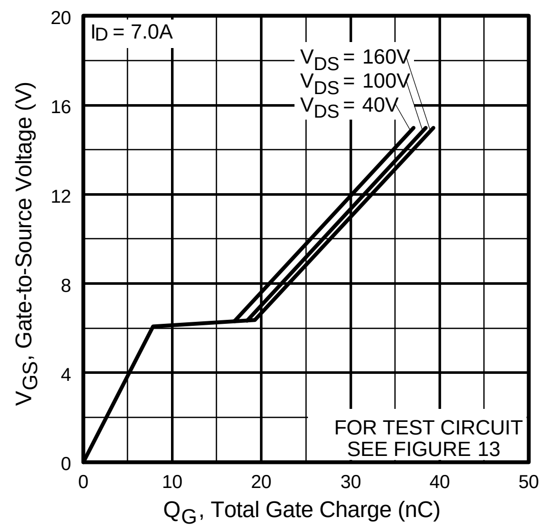


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

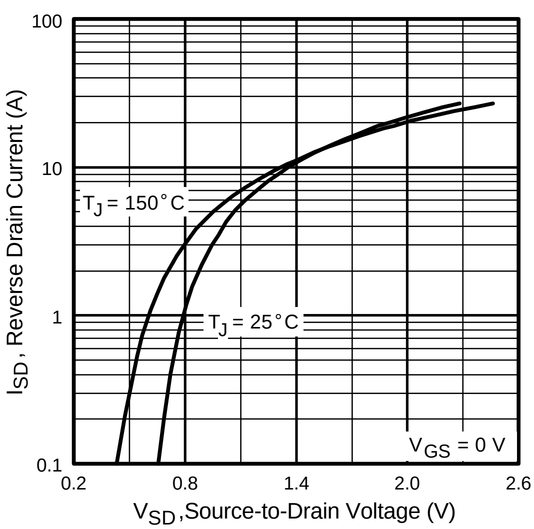


Fig 7. Typical Source-Drain Diode Forward Voltage

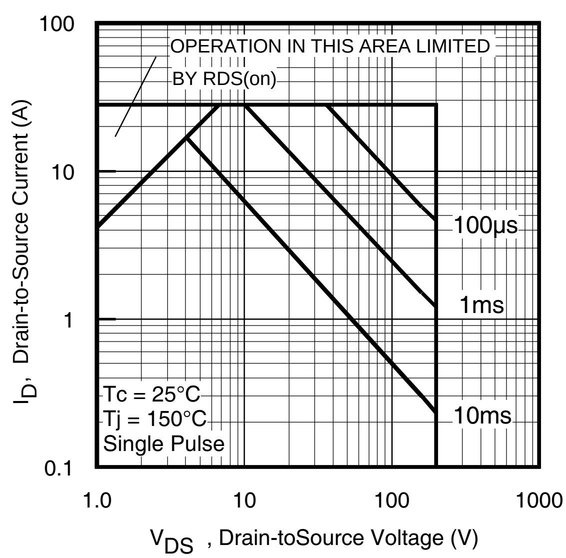


Fig 8. Maximum Safe Operating Area

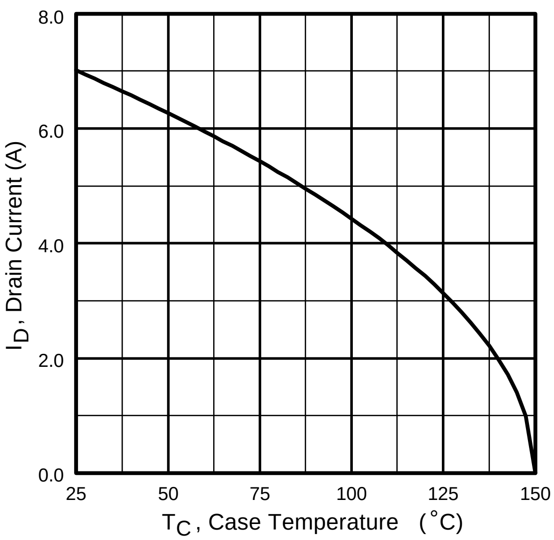


Fig 9. Maximum Drain Current Vs. Case Temperature

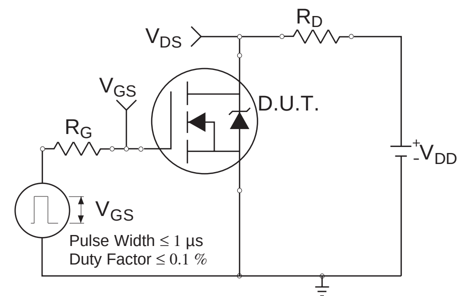


Fig 10a. Switching Time Test Circuit

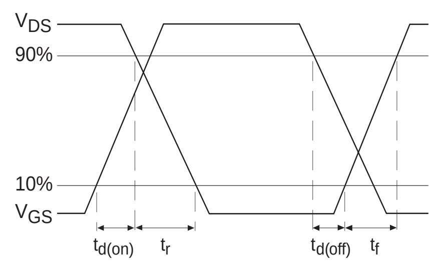


Fig 10b. Switching Time Waveforms

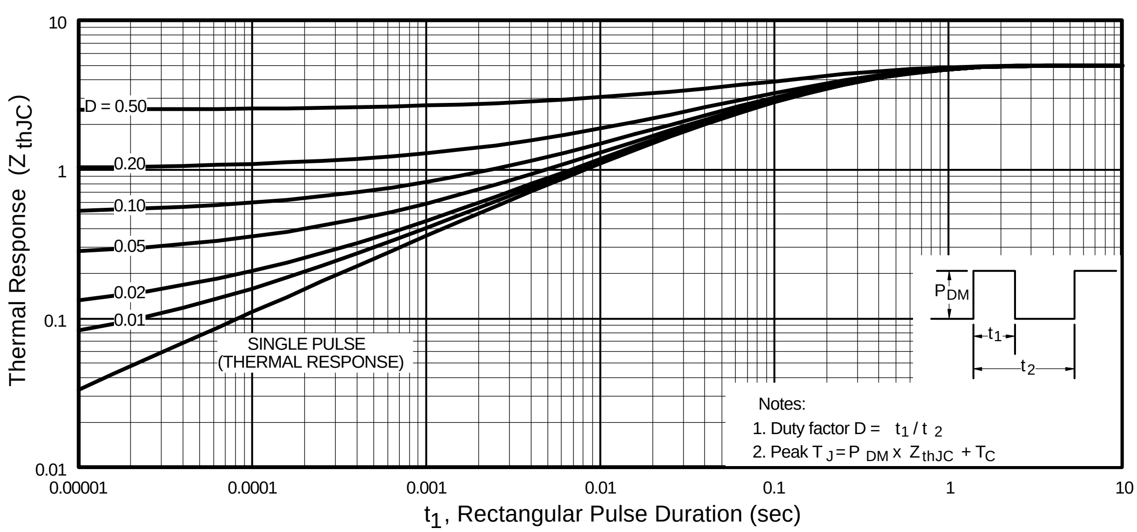


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

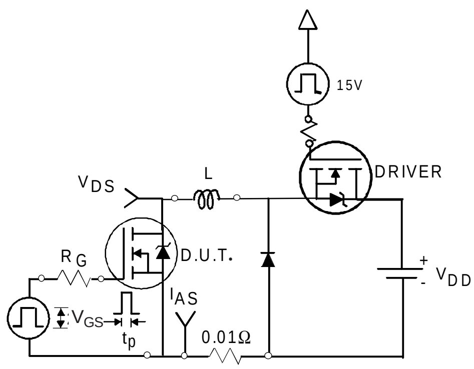


Fig 12a. Unclamped Inductive Test Circuit

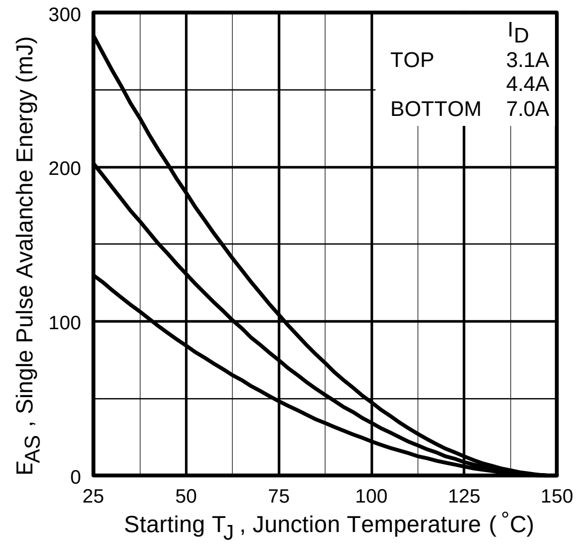


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

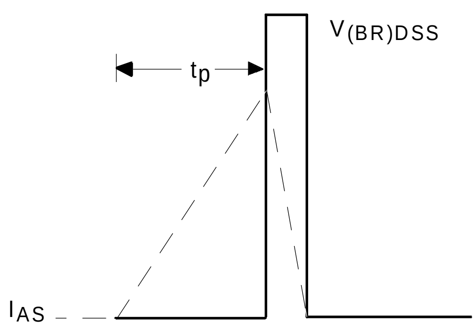


Fig 12b. Unclamped Inductive Waveforms

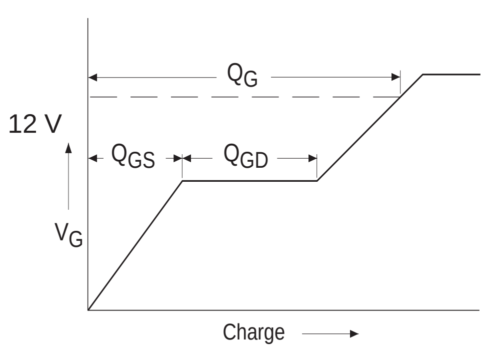


Fig 13a. Basic Gate Charge Waveform

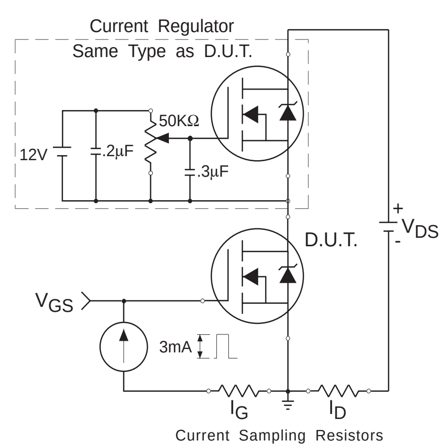


Fig 13b. Gate Charge Test Circuit

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 50V, starting T_J = 25°C, L= 5.3mH Peak I_L = 7.0A, V_{GS} = 12V

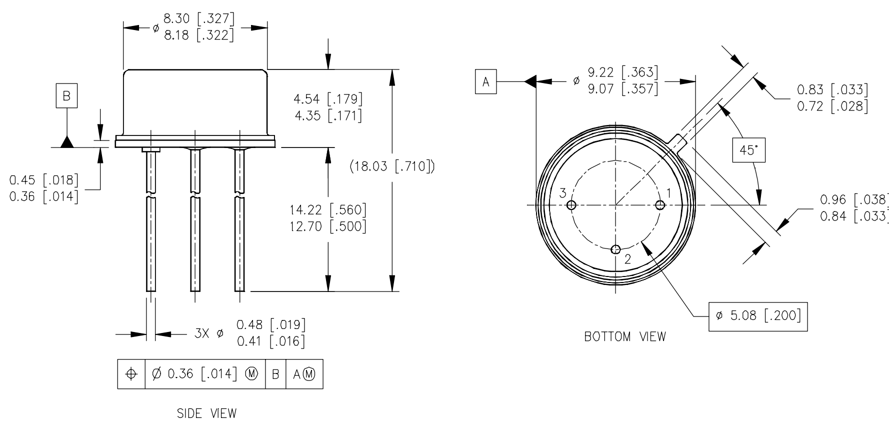
③ $I_{SD} \le 7.0A$, di/dt ≤ 219A/μs, $V_{DD} \le 200V$, $T_J \le 150°C$

④ Pulse width ≤ 300 μs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 12 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

⑥ **Total Dose Irradiation with V_{DS} Bias.** 160 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — TO-205AF (Modified TO-39)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME 14.5M–1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. CONTROLLING DIMENSION: INCH.
4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND
1- SOURCE
2- GATE
3- DRAIN

International
IOR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR LEOMINSTER : 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.

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