


**RADIATION HARDENED  
 LOGIC LEVEL POWER MOSFET  
 THRU-HOLE (TO-39)**

**IRHLF6970Z4  
 60V, P-CHANNEL  
 TECHNOLOGY**

**Product Summary**

Part Number	Radiation Level	RDS(on)	ID
IRHLF6970Z4	100K Rads (Si)	1.2Ω	-1.6A
IRHLF6930Z4	300K Rads (Si)	1.2Ω	-1.6A

International Rectifier's R6™ Logic Level Power Mosfets provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.



**TO-39**

**Features:**

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary N-Channel Available - IRHLF670Z4

**Absolute Maximum Ratings**

**Pre-Irradiation**

	Parameter		Units
I <sub>D</sub> @ V <sub>GS</sub> = -4.5V, T <sub>C</sub> = 25°C	Continuous Drain Current	-1.6	A
I <sub>D</sub> @ V <sub>GS</sub> = -4.5V, T <sub>C</sub> = 100°C	Continuous Drain Current	-1.0	
I <sub>DM</sub>	Pulsed Drain Current ①	-6.4	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Max. Power Dissipation	5.0	W
	Linear Derating Factor	0.04	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	10	mJ
I <sub>AR</sub>	Avalanche Current ①	-1.6	A
EAR	Repetitive Avalanche Energy ①	0.5	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-4.0	V/ns
T <sub>J</sub>	Operating Junction	-55 to 150	°C
T <sub>STG</sub>	Storage Temperature Range		
	Lead Temperature	300 (0.063in/1.6mm from case for 10s)	
	Weight	0.98 ( Typical )	g

For footnotes refer to the last page

**Electrical Characteristics @ T<sub>j</sub> = 25°C (Unless Otherwise Specified)**

	Parameter	Min	Typ	Max	Units	Test Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-60	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Temperature Coefficient of Breakdown Voltage	—	-0.06	—	V/°C	Reference to 25°C, I <sub>D</sub> = -1.0mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-State Resistance	—	—	1.2	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1.0A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0	—	-2.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250μA
g <sub>fs</sub>	Forward Transconductance	1.0	—	—	S (r <sub>o</sub> )	V <sub>DS</sub> = -10V, I <sub>DS</sub> = -1.0A ④
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	—	-1.0	μA	V <sub>DS</sub> = -48V, V <sub>GS</sub> = 0V
		—	—	-10		V <sub>DS</sub> = -48V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	—	-100	nA	V <sub>GS</sub> = -10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	—	100		V <sub>GS</sub> = 10V
Q <sub>g</sub>	Total Gate Charge	—	—	4.0	nC	V <sub>GS</sub> = -5.0V, I <sub>D</sub> = -1.6A V <sub>DS</sub> = -30V
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	1.5		
Q <sub>gd</sub>	Gate-to-Drain ('Miller') Charge	—	—	1.8		
t <sub>d(on)</sub>	Turn-On Delay Time	—	—	18	ns	V <sub>DD</sub> = -30V, I <sub>D</sub> = -1.6A, V <sub>GS</sub> = -5.0V, R <sub>G</sub> = 24Ω
t <sub>r</sub>	Rise Time	—	—	20		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	—	15		
t <sub>f</sub>	Fall Time	—	—	25		
L <sub>S</sub> + L <sub>D</sub>	Total Inductance	—	7.0	—	nH	Measured from Drain lead (6mm/0.25in from package) to Source lead(6mm/0.25in from package)with Source wire internally bonded from Source pin to Drain pad
C <sub>iss</sub>	Input Capacitance	—	177	—	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	—	40	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	8.0	—		
R <sub>g</sub>	Gate Resistance	—	28	—	Ω	f = 5.0MHz, open drain

**Source-Drain Diode Ratings and Characteristics**

	Parameter	Min	Typ	Max	Units	Test Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	-1.6	A	
I <sub>SM</sub>	Pulse Source Current (Body Diode) ①	—	—	-6.4		
V <sub>SD</sub>	Diode Forward Voltage	—	—	-5.0	V	T <sub>j</sub> = 25°C, I <sub>S</sub> = -1.6A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	—	50	ns	T <sub>j</sub> = 25°C, I <sub>F</sub> = -1.6A, di/dt ≤ -100A/μs
Q <sub>RR</sub>	Reverse Recovery Charge	—	—	50	nC	V <sub>DD</sub> ≤ -25V ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L <sub>S</sub> + L <sub>D</sub> .				

**Thermal Resistance**

	Parameter	Min	Typ	Max	Units	Test Conditions
R <sub>thJC</sub>	Junction-to-Case	—	—	25	°C/W	

**Note:** Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

## Radiation Characteristics

IRHLF6970Z4

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-3 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

**Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥**

	Parameter	100K Rads(Si) <sup>1</sup>		300KRads(Si) <sup>2</sup>		Units	Test Conditions
		Min	Max	Min	Max		
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-60	—	-60	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -250μA
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0	-2.0	-1.0	-2.0		V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -250μA
I <sub>GSS</sub>	Gate-to-Source Leakage Forward	—	-100	—	-100	nA	V <sub>GS</sub> = -10V
I <sub>GSS</sub>	Gate-to-Source Leakage Reverse	—	100	—	100		V <sub>GS</sub> = 10 V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	—	-1.0	—	-10	μA	V <sub>DS</sub> = -48V, V <sub>GS</sub> = 0V
R <sub>DS(on)</sub>	Static Drain-to-Source <sup>④</sup> On-State Resistance (TO-39)	—	1.2	—	1.2	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -1.0A
V <sub>SD</sub>	Diode Forward Voltage <sup>④</sup>	—	-5.0	—	-5.0	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = -1.6A

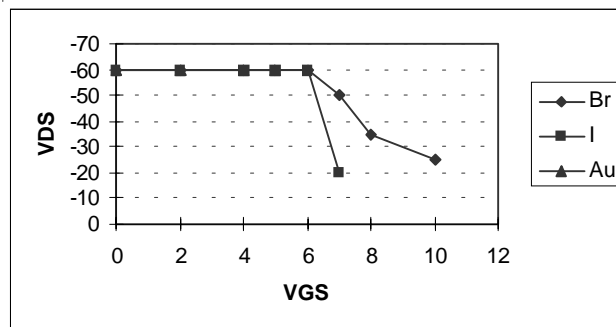
1. Part number IRHLF6970Z4

2. Part number IRHLF6930Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

**Table 2. Single Event Effect Safe Operating Area**

Ion	LET (MeV/(mg/cm <sup>2</sup> ))	Energy (MeV)	Range (μm)	VDS (V)							
				@VGS= 0V	@VGS= 2V	@VGS= 4V	@VGS= 5V	@VGS= 6V	@VGS= 7V	@VGS= 8V	@VGS= 10V
Br	37.9	285	36.8	-60	-60	-60	-60	-60	-50	-35	-25
I	59.9	345	32.7	-60	-60	-60	-60	-60	-20	-	-
Au	82.3	357	28.5	-60	-60	-60	-60	-	-	-	-



**Fig a. Single Event Effect, Safe Operating Area**

For footnotes refer to the last page

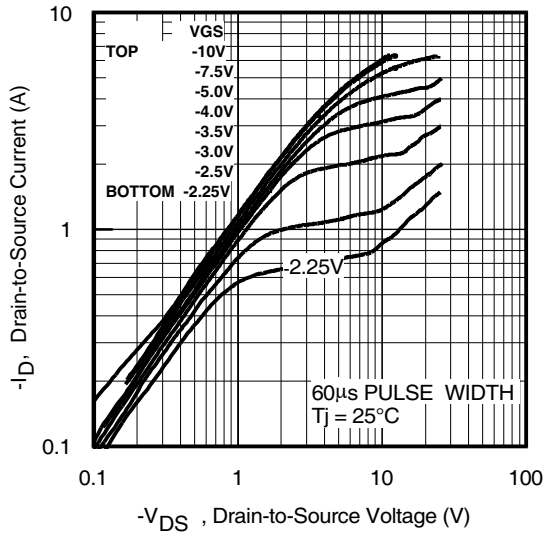


Fig 1. Typical Output Characteristics

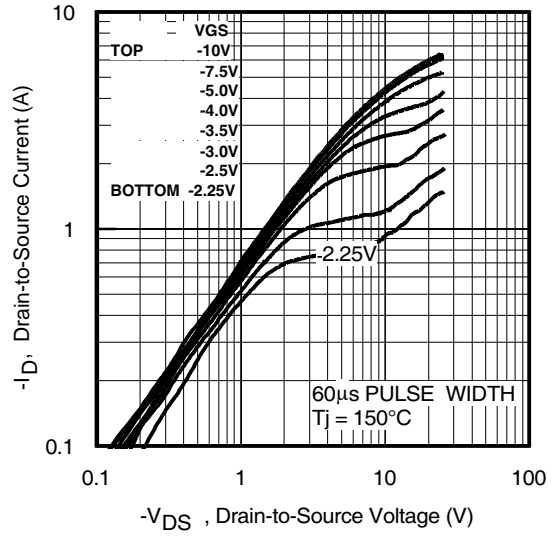


Fig 2. Typical Output Characteristics

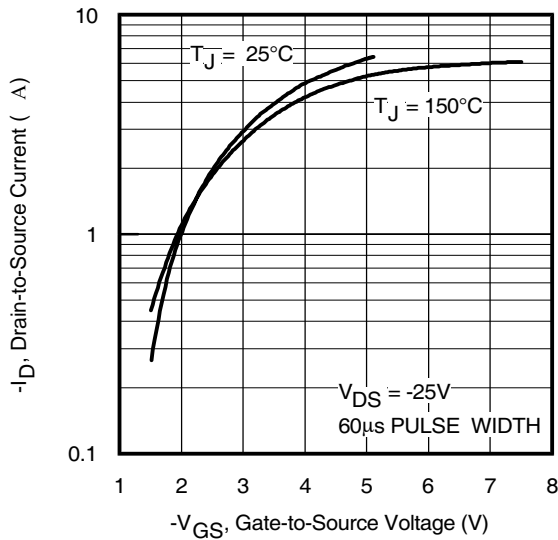


Fig 3. Typical Transfer Characteristics

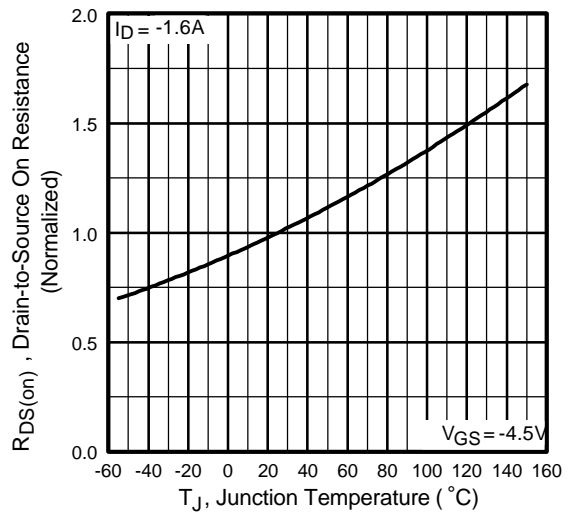
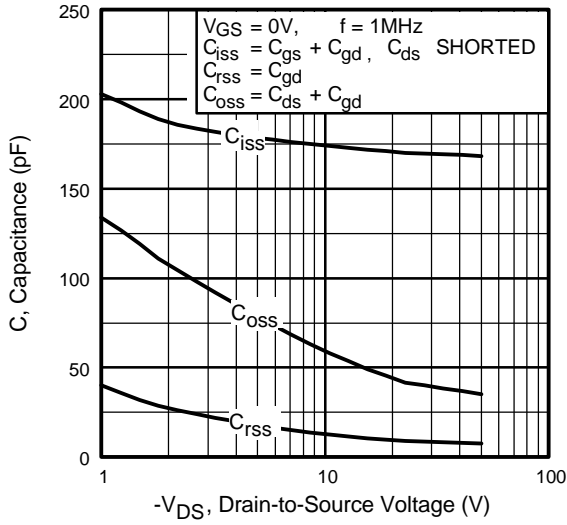
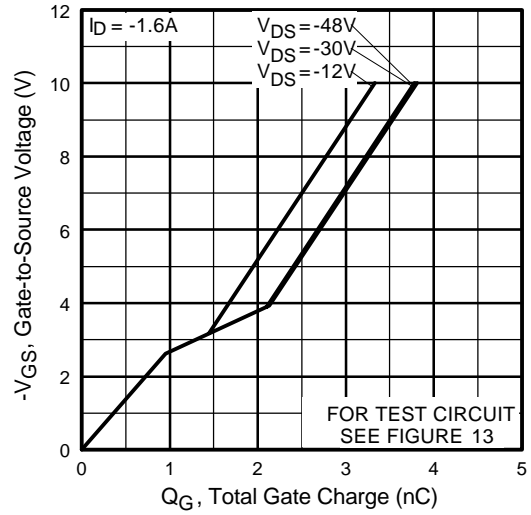


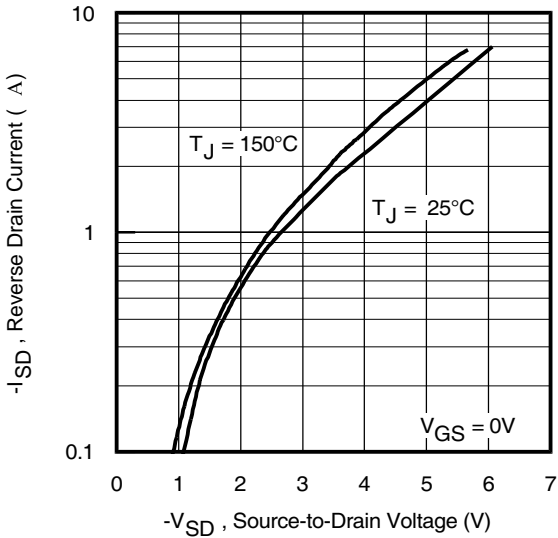
Fig 4. Normalized On-Resistance Vs. Temperature



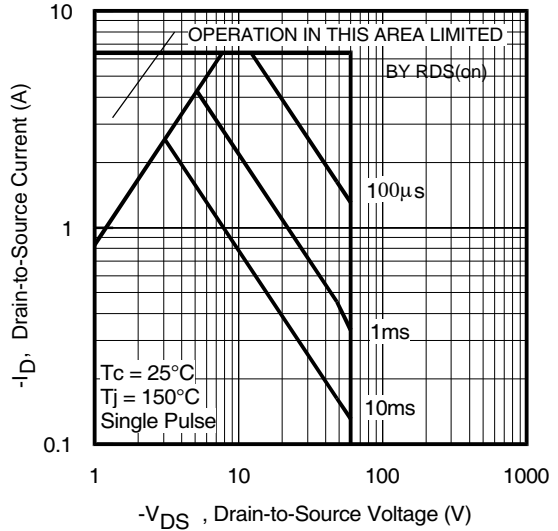
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

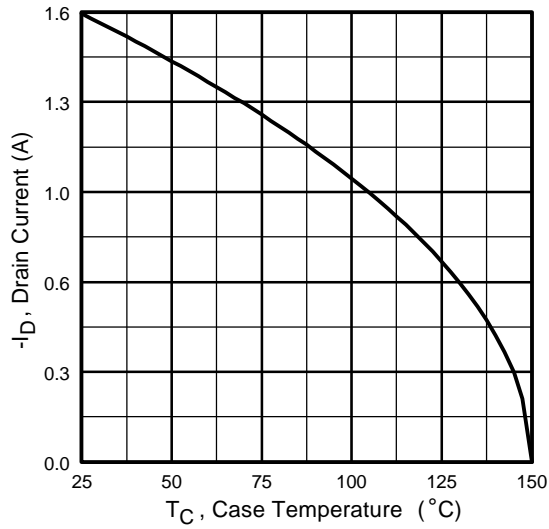


Fig 9. Maximum Drain Current Vs. Case Temperature

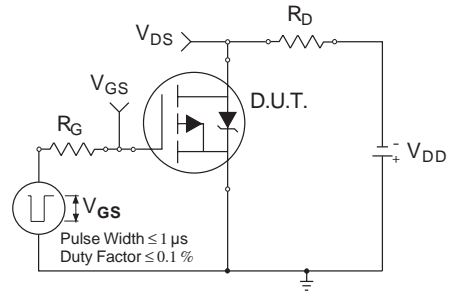


Fig 10a. Switching Time Test Circuit

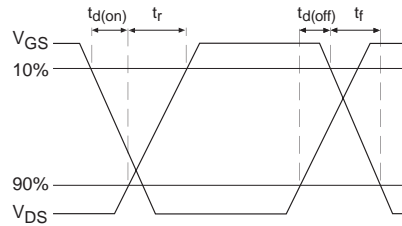


Fig 10b. Switching Time Waveforms

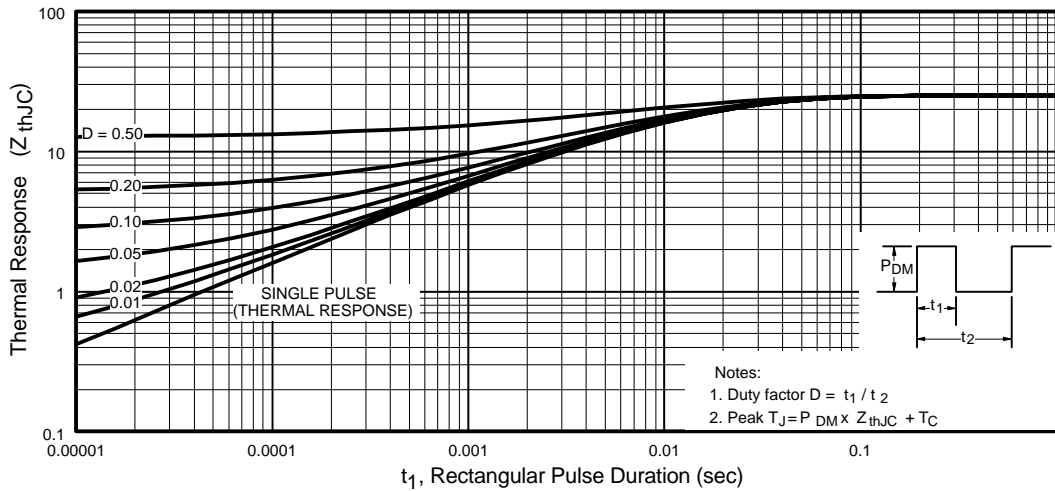


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

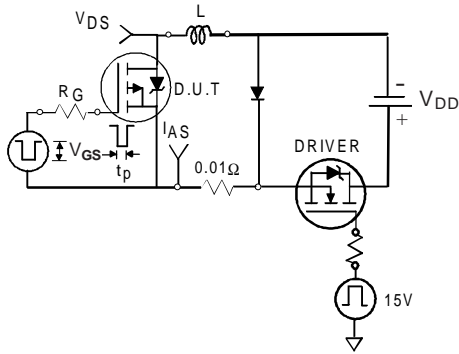


Fig 12a. Unclamped Inductive Test Circuit

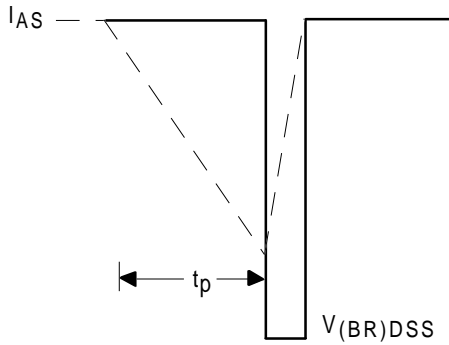


Fig 12b. Unclamped Inductive Waveforms

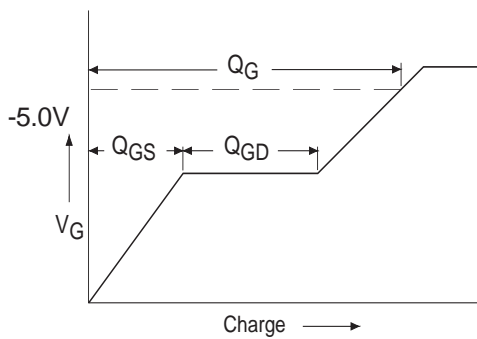


Fig 13a. Basic Gate Charge Waveform

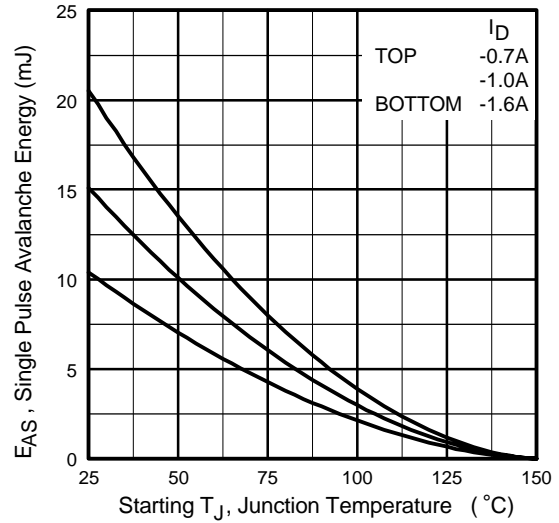


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

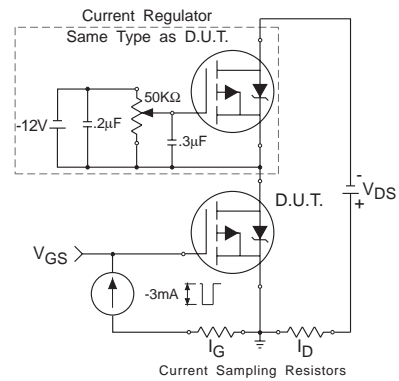
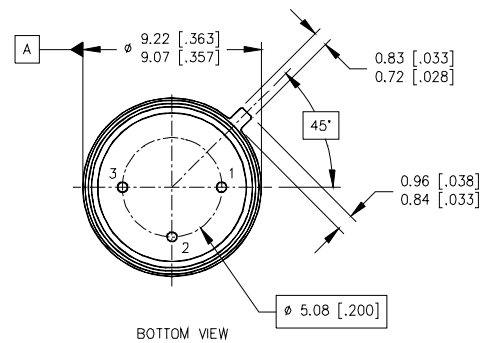
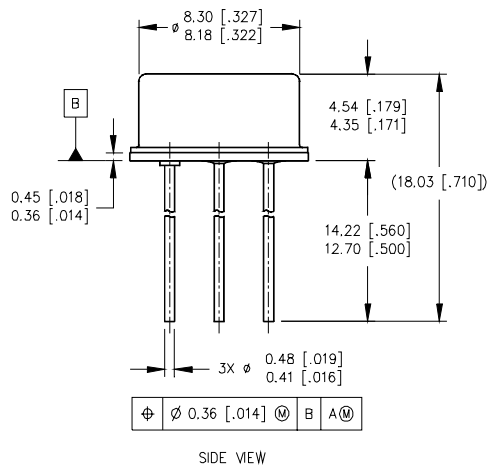


Fig 13b. Gate Charge Test Circuit

**Footnotes:**

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ②  $V_{DD} = -25V$ , starting  $T_J = 25^{\circ}C$ ,  $L = 8.0mH$   
Peak  $I_L = -1.6A$ ,  $V_{GS} = -12V$
- ③  $I_{SD} \leq -1.6A$ ,  $di/dt \leq -170A/\mu s$ ,  
 $V_{DD} \leq -60V$ ,  $T_J \leq 150^{\circ}C$
- ④ Pulse width  $\leq 300 \mu s$ ; Duty Cycle  $\leq 2\%$
- ⑤ **Total Dose Irradiation with  $V_{GS}$  Bias.**  
-10 volt  $V_{GS}$  applied and  $V_{DS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with  $V_{DS}$  Bias.**  
-48 volt  $V_{DS}$  applied and  $V_{GS} = 0$  during irradiation per MIL-STD-750, method 1019, condition A.

**Case Outline and Dimensions — TO-205AF (Modified TO-39)**



NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME 14.5M-1994.
- 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- 3. CONTROLLING DIMENSION: INCH.
- 4. CONFORMS TO JEDEC OUTLINE TO-205AF (TO-39).

LEGEND

- 1- SOURCE
- 2- GATE
- 3- DRAIN

International  
**IR** Rectifier

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Data and specifications subject to change without notice. 07/03