

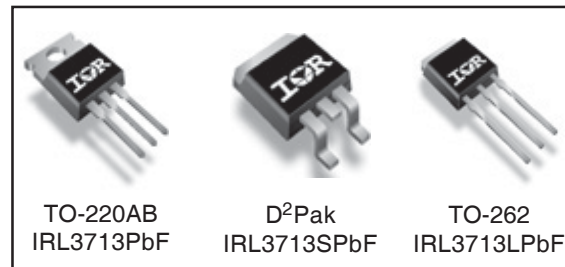
**Applications**

- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power
- 100% R<sub>G</sub> Tested
- Lead-Free

V <sub>DSS</sub>	R <sub>DS(on)</sub> max (mΩ)	I <sub>D</sub>
30V	3.0@V <sub>GS</sub> = 10V	260A <sup>Ⓞ</sup>

**Benefits**

- Ultra-Low Gate Impedance
- Very Low R<sub>DS(on)</sub> at 4.5V V<sub>GS</sub>
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

Symbol	Parameter	Max	Units
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	260 <sup>Ⓞ</sup>	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	180 <sup>Ⓞ</sup>	
I <sub>DM</sub>	Pulsed Drain Current <sup>①</sup>	1040 <sup>Ⓞ</sup>	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	330	W
P <sub>D</sub> @ T <sub>C</sub> = 100°C	Maximum Power Dissipation	170	
	Linear Derating Factor	2.2	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Junction and Storage Temperature Range	-55 to +175	°C

**Thermal Resistance**

Symbol	Parameter	Typ	Max	Units
R <sub>θJC</sub>	Junction-to-Case <sup>②</sup>	—	0.45*	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface <sup>④</sup>	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient <sup>④⑦</sup>	—	62	
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) <sup>⑤⑦</sup>	—	40	

\* R<sub>θJC</sub> (end of life) for D<sup>2</sup>Pak and TO-262 = 0.50°C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wearout of the die attach medium.

Notes <sup>①</sup> through <sup>⑦</sup> are on page 11

# IRL3713/S/LPbF

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## Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.027	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	2.6	3.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 38A ③
		—	3.3	4.0		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 30A ③
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	50	μA	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V
		—	—	20		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
		—	—	100		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-200		V <sub>GS</sub> = -20V

## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	76	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 30A
Q <sub>g</sub>	Total Gate Charge	—	75	110	nC	I <sub>D</sub> = 30A
Q <sub>gs</sub>	Gate-to-Source Charge	—	24	—		V <sub>DS</sub> = 15V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	37	—		V <sub>GS</sub> = 4.5V ④
Q <sub>oss</sub>	Output Gate Charge	—	61	92		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 15V
R <sub>G</sub>	Gate Resistance	0.5	—	3.4	Ω	
t <sub>d(on)</sub>	Turn-On Delay Time	—	16	—	ns	V <sub>DD</sub> = 15V
t <sub>r</sub>	Rise Time	—	160	—		I <sub>D</sub> = 30A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	40	—		R <sub>G</sub> = 1.8Ω
t <sub>f</sub>	Fall Time	—	57	—		V <sub>GS</sub> = 4.5V ④
C <sub>iss</sub>	Input Capacitance	—	5890	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	3130	—		V <sub>DS</sub> = 15V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	630	—		f = 1.0MHz

## Avalanche Characteristics

Symbol	Parameter	Typ	Max	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy ②	—	1530	mJ
I <sub>AR</sub>	Avalanche Current ①	—	46	A

## Diode Characteristics

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	260 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①⑥	—	—	1040 ⑥		
V <sub>SD</sub>	Diode Forward Voltage	—	0.80	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 30A, V <sub>GS</sub> = 0V ③
		—	0.68	—		T <sub>J</sub> = 125°C, I <sub>S</sub> = 30A, V <sub>GS</sub> = 0V ③
t <sub>rr</sub>	Reverse Recovery Time	—	75	110	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 30A, V <sub>R</sub> = 0V
Q <sub>rr</sub>	Reverse Recovery Charge	—	140	210	nC	di/dt = 100A/μs ③
t <sub>rr</sub>	Reverse Recovery Time	—	78	120	ns	T <sub>J</sub> = 125°C, I <sub>F</sub> = 30A, V <sub>R</sub> = 20V
Q <sub>rr</sub>	Reverse Recovery Charge	—	160	240	nC	di/dt = 100A/μs ③

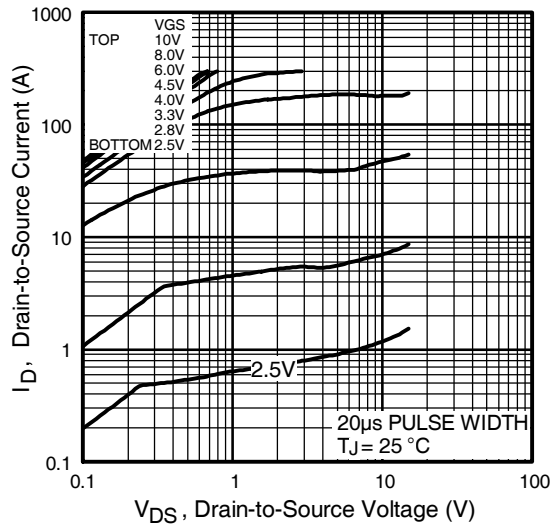


Fig 1. Typical Output Characteristics

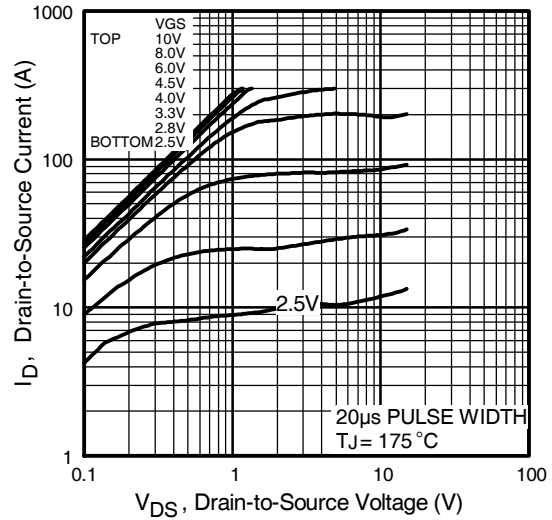


Fig 2. Typical Output Characteristics

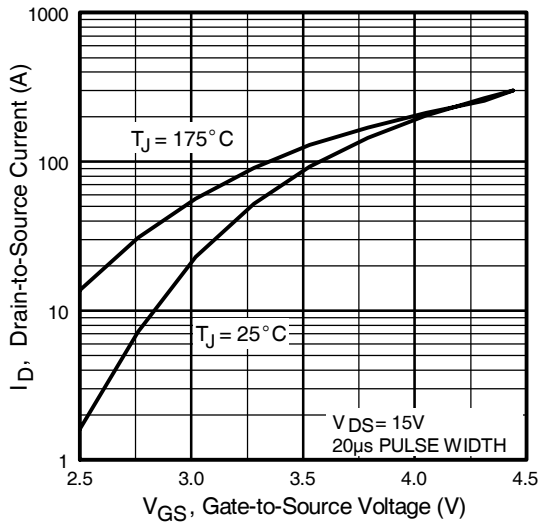


Fig 3. Typical Transfer Characteristics

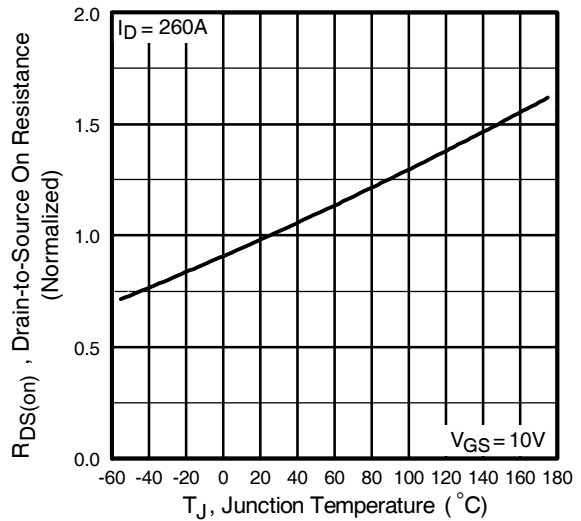
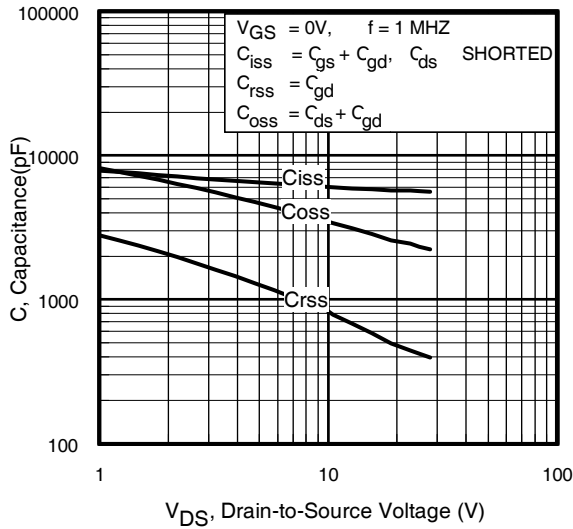
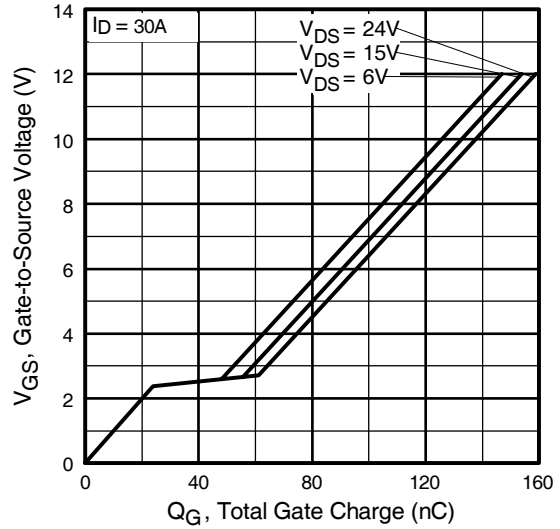


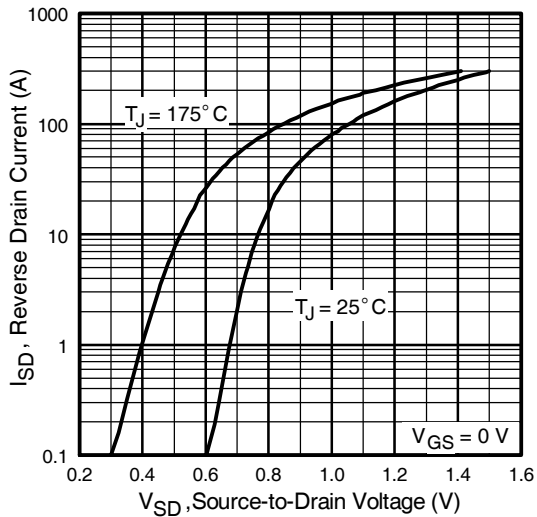
Fig 4. Normalized On-Resistance Vs. Temperature



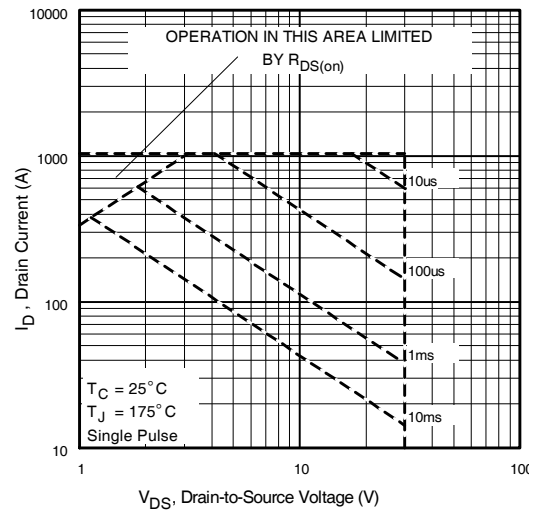
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area

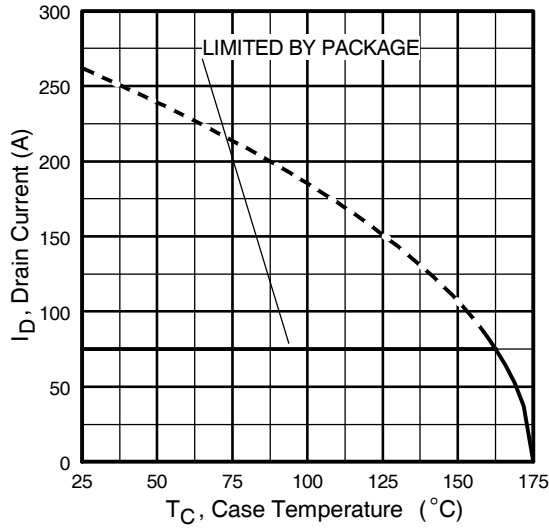


Fig 9. Maximum Drain Current Vs. Case Temperature

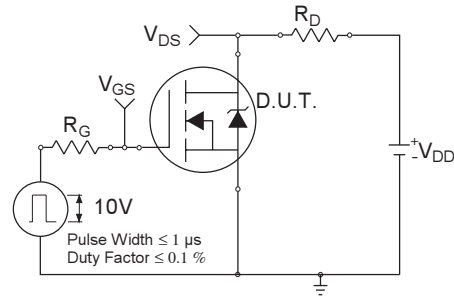


Fig 10a. Switching Time Test Circuit

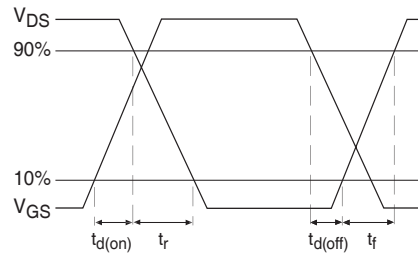


Fig 10b. Switching Time Waveforms

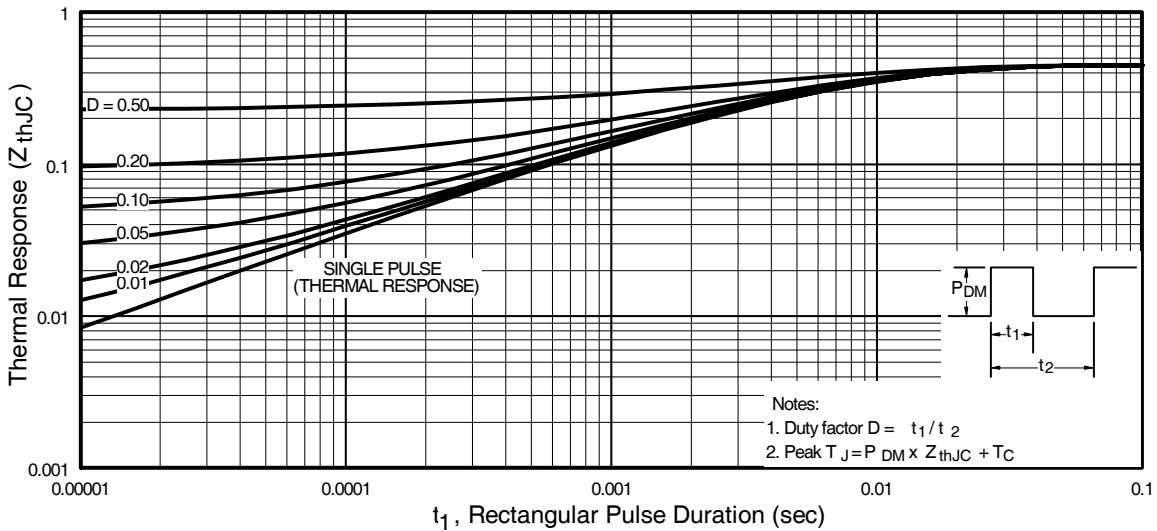
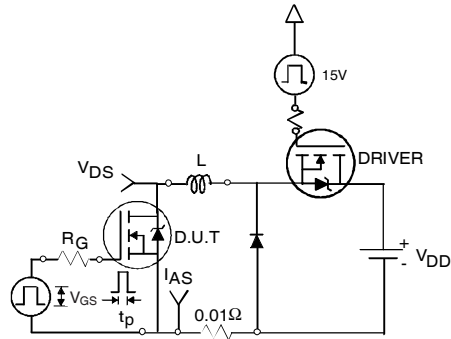


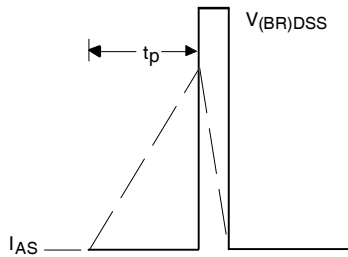
Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

# IRL3713/S/LPbF

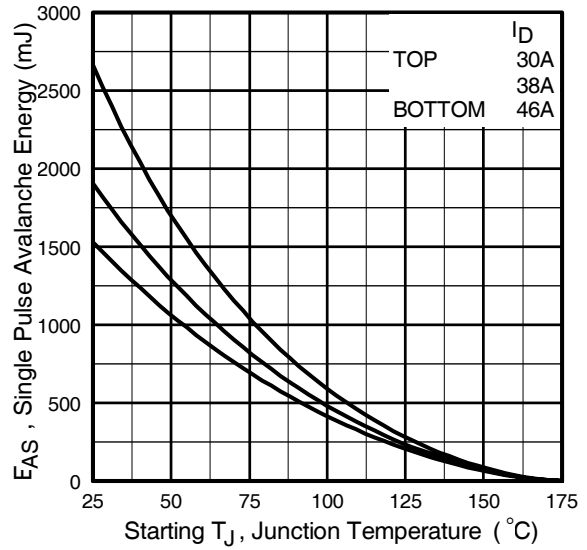
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**IR** Rectifier



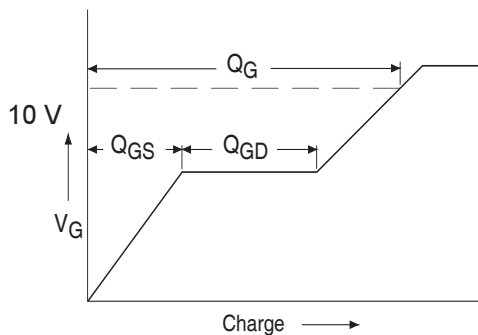
**Fig 12a.** Unclamped Inductive Test Circuit



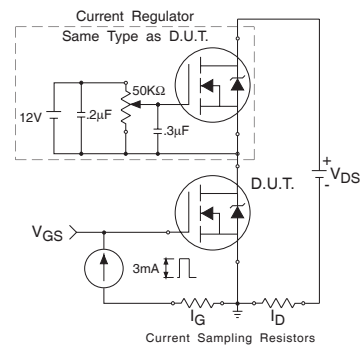
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

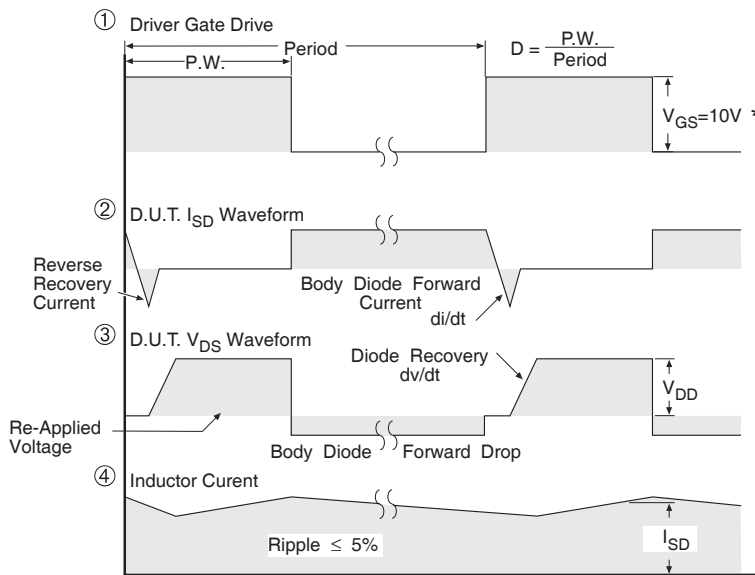
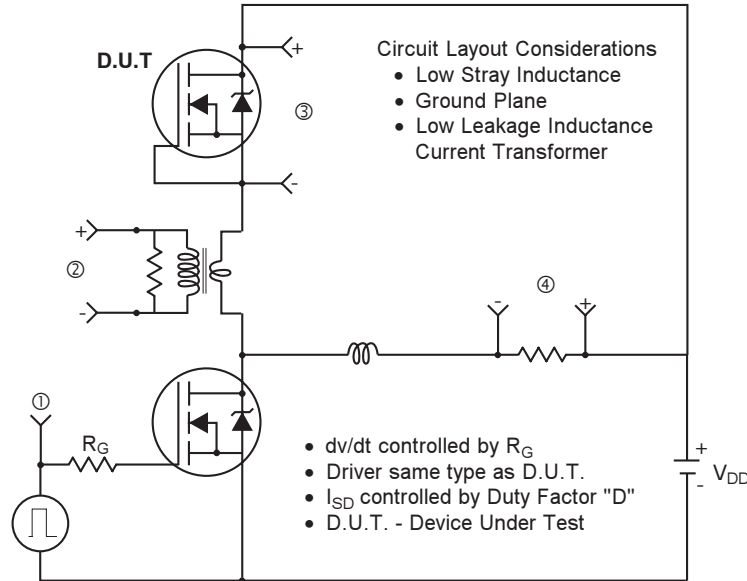


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**



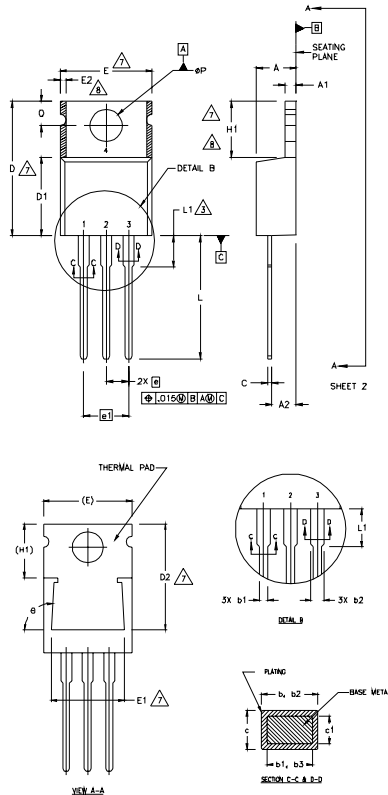
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

# IRL3713/S/LPbF

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
  - 2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY. DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
  - 5 CONTROLLING DIMENSION : INCHES.
  - 6 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
  - 7 DIMENSION E2 x H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

**LEAD ASSIGNMENTS**

- HEXLEET**
- 1 - GATE
  - 2 - DRAIN
  - 3 - SOURCE

**IRBLS CoPACK**

- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

**DIODES**

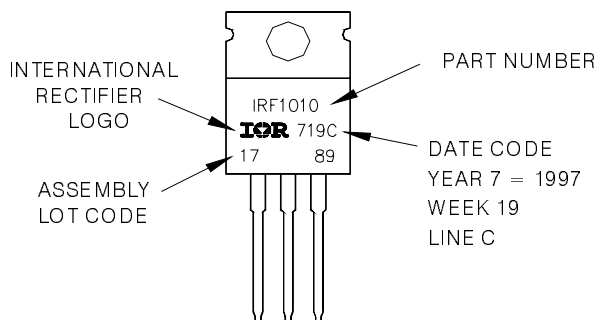
- 1 - ANODE/OPEN
- 2 - CATHODE
- 3 - ANODE

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	3.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	-	6.35	-	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°-93°		90°-93°		

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"

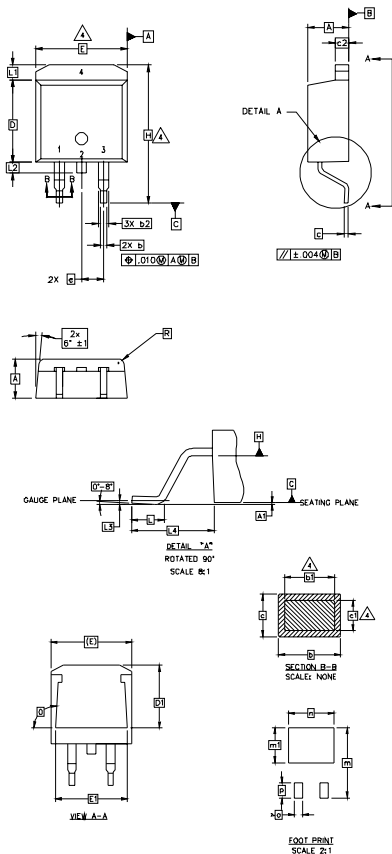
**Note:** "P" in assembly line position indicates "Lead-Free"





## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	4
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	4
c2	1.14	1.65	.045	.065	
D	8.51	9.65	.335	.380	3
D1	6.86		.270		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1		1.65		.065	
L2	1.27	1.78	.050	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
R	0.51	0.71	.020	.028	
θ	90°	93°	90°	93°	

LEAD ASSIGNMENTS

HEXFET

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

IGBTs, CoPACK

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

DIODES

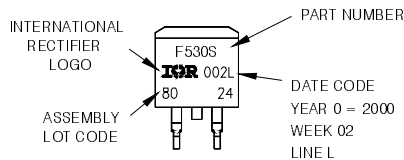
- 1.- ANODE \*
- 2, 4.- CATHODE
- 3.- ANODE

\* PART DEPENDENT.

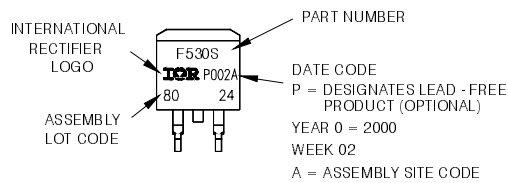
## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE 'L'

Note: "P" in assembly line position  
indicates "Lead - Free"



OR

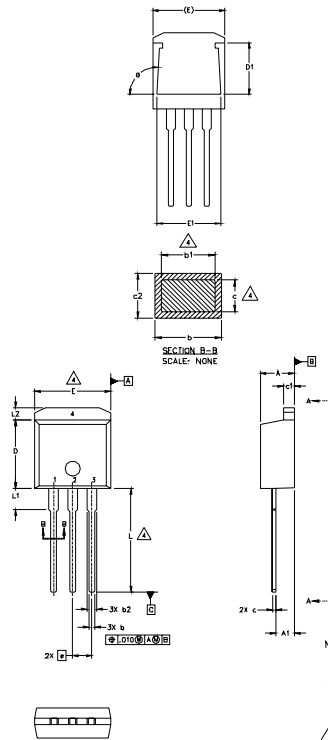


# IRL3713/S/LPbF

## TO-262 Package Outline

Dimensions are shown in millimeters (inches)

International  
**IR** Rectifier



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

### LEAD ASSIGNMENTS

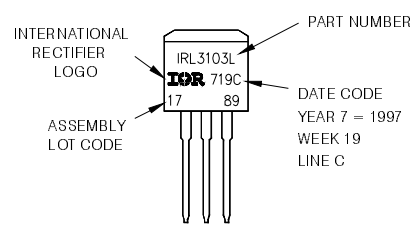
HEXFET	IGBT
1.- GATE	1 - GATE
2.- DRAIN	2 - COLLECTOR
3.- SOURCE	3 - EMITTER
4.- DRAIN	

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
  3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
  5. CONTROLLING DIMENSION: INCH.

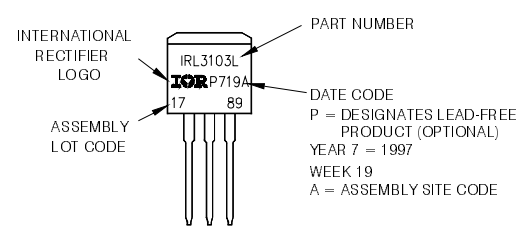
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE 'C'

Note: 'P' in assembly line position indicates 'Lead-Free'

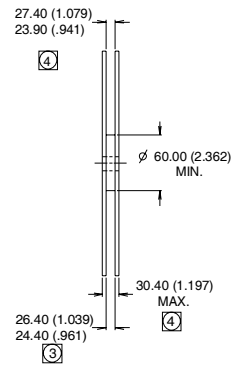
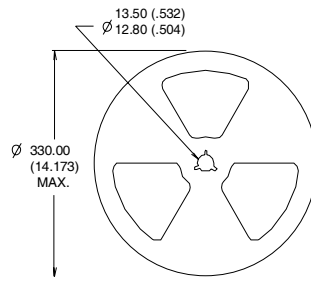
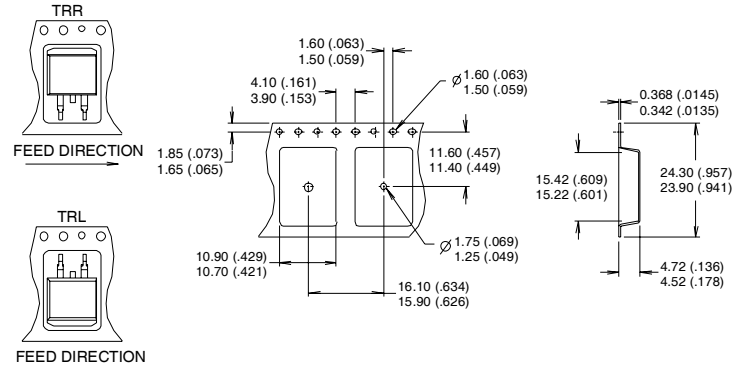


**OR**



## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



- NOTES:
1. COMFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION MEASURED @ HUB.
  4. INCLUDES FLANGE DISTORTION @ OUTER EDGE.

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.4\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 46\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ③ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ④ This is only applied to TO-220A package.
- ⑤ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.
- ⑦  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice.  
 This product has been designed and qualified for the Industrial market.  
 Qualification Standards can be found on IR's Web site.

International  
**IR** Rectifier

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