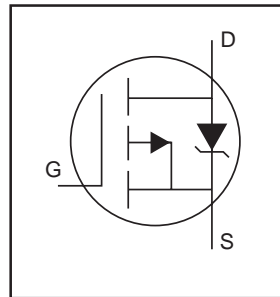


# IRLIB9343PbF

## Features

- Advanced Process Technology
- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low  $R_{DS(ON)}$  for Improved Efficiency
- Low  $Q_g$  and  $Q_{sw}$  for Better THD and Improved Efficiency
- Low  $Q_{rr}$  for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Repetitive Avalanche Capability for Robustness and Reliability
- Lead-Free

Key Parameters		
$V_{DS}$	-55	V
$R_{DS(ON)}$ typ. @ $V_{GS} = -10V$	93	mΩ
$R_{DS(ON)}$ typ. @ $V_{GS} = -4.5V$	150	mΩ
$Q_g$ typ.	31	nC
$T_J$ max	175	°C



## Description

This Digital Audio HEXFET<sup>®</sup> is specifically designed for Class-D audio amplifier applications. This MosFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MosFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MosFET a highly efficient, robust and reliable device for Class-D audio amplifier applications.

## Absolute Maximum Ratings

	Parameter	Max.	Units
$V_{DS}$	Drain-to-Source Voltage	-55	V
$V_{GS}$	Gate-to-Source Voltage	±20	
$I_D$ @ $T_C = 25^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V	-14	A
$I_D$ @ $T_C = 100^\circ C$	Continuous Drain Current, $V_{GS}$ @ -10V	-10	
$I_{DM}$	Pulsed Drain Current ①	-60	
$P_D$ @ $T_C = 25^\circ C$	Power Dissipation	33	W
$P_D$ @ $T_C = 100^\circ C$	Power Dissipation	20	
	Linear Derating Factor	0.26	W/°C
$T_J$	Operating Junction and	-40 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Mounting Torque, 6-32 or M3 screw	10 (1.1)	lbf•in (N•m)

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	—	3.84	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④	—	65	

Notes ① through ⑤ are on page 7

**Electrical Characteristics @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

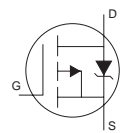
	Parameter	Min.	Typ.	Max.	Units	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	-55	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-52	—	mV/°C	Reference to $25^\circ\text{C}$ , $I_D = -1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	93	105	mΩ	$V_{GS} = -10V, I_D = -3.4A$ ③
		—	150	170		$V_{GS} = -4.5V, I_D = -2.7A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-3.7	—	mV/°C	
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-2.0	μA	$V_{DS} = -55V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -55V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
$g_{fs}$	Forward Transconductance	5.3	—	—	S	$V_{DS} = -25V, I_D = -14A$
$Q_g$	Total Gate Charge	—	31	47		$V_{DS} = -44V$
$Q_{gs}$	Pre-Vth Gate-to-Source Charge	—	7.1	—		$V_{GS} = -10V$
$Q_{gd}$	Gate-to-Drain Charge	—	8.5	—		$I_D = -14A$
$Q_{godr}$	Gate Charge Overdrive	—	15	—		See Fig. 6 and 19
$t_{d(on)}$	Turn-On Delay Time	—	9.5	—	ns	$V_{DD} = -28V, V_{GS} = -10V$ ③
$t_r$	Rise Time	—	24	—		$I_D = -14A$
$t_{d(off)}$	Turn-Off Delay Time	—	21	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	9.5	—		
$C_{iss}$	Input Capacitance	—	660	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	160	—		$V_{DS} = -50V$
$C_{rss}$	Reverse Transfer Capacitance	—	72	—		$f = 1.0\text{MHz}$ , See Fig.5
$C_{oss}$	Effective Output Capacitance	—	280	—		$V_{GS} = 0V, V_{DS} = 0V$ to $-44V$
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.)
$L_S$	Internal Source Inductance	—	7.5	—		from package and center of die contact

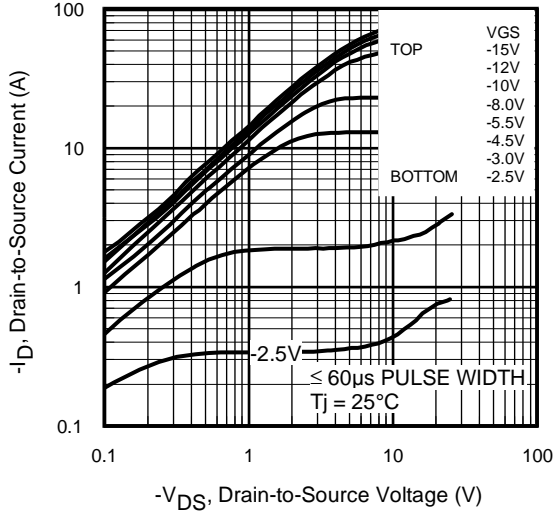
**Avalanche Characteristics**

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	190	mJ
$I_{AR}$	Avalanche Current ⑤	See Fig. 14, 15, 17a, 17b		A
$E_{AR}$	Repetitive Avalanche Energy ⑤			mJ

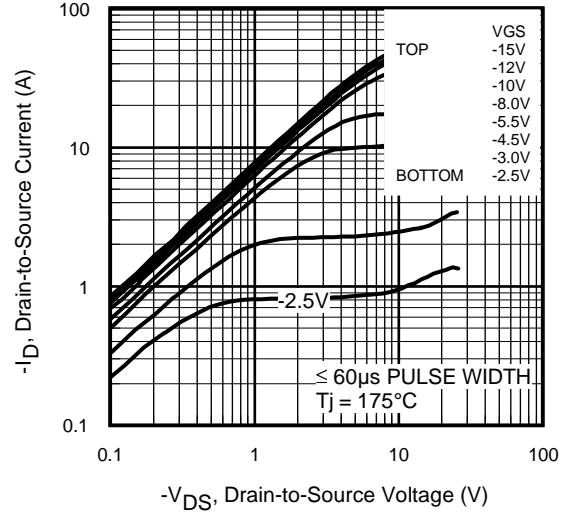
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S @ T_C = 25^\circ\text{C}$	Continuous Source Current (Body Diode)	—	—	-14	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-60		
$V_{SD}$	Diode Forward Voltage	—	—	-1.2	V	$T_J = 25^\circ\text{C}, I_S = -14A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	57	86	ns	$T_J = 25^\circ\text{C}, I_F = -14A$
$Q_{rr}$	Reverse Recovery Charge	—	120	180	nC	$di/dt = 100A/\mu s$ ③

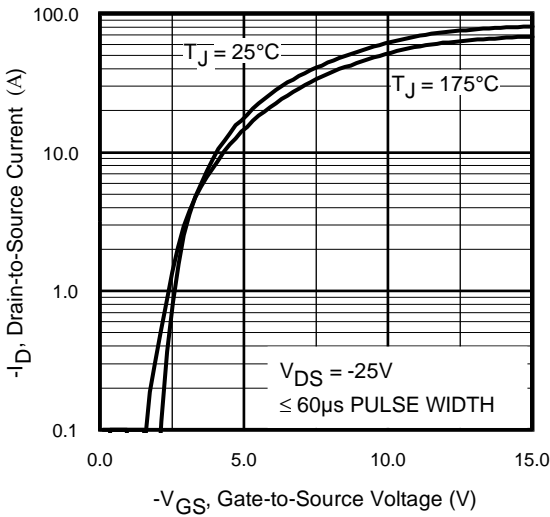




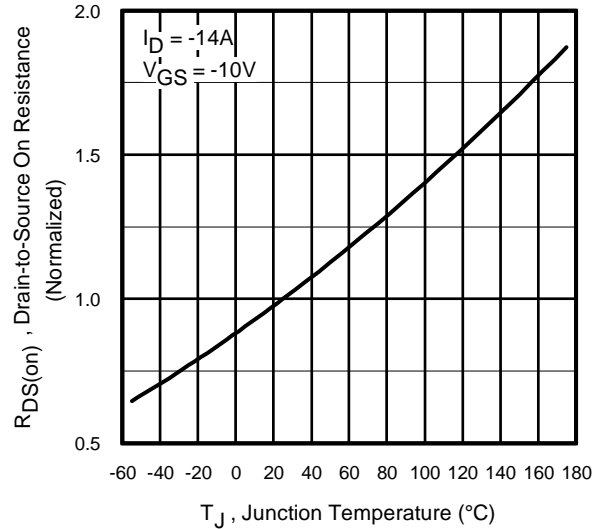
**Fig 1.** Typical Output Characteristics



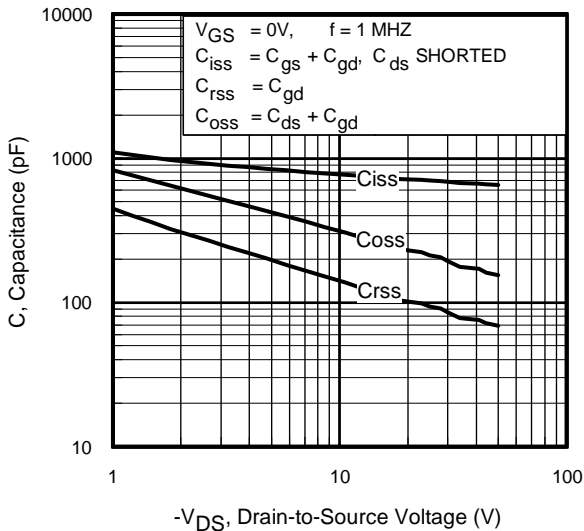
**Fig 2.** Typical Output Characteristics



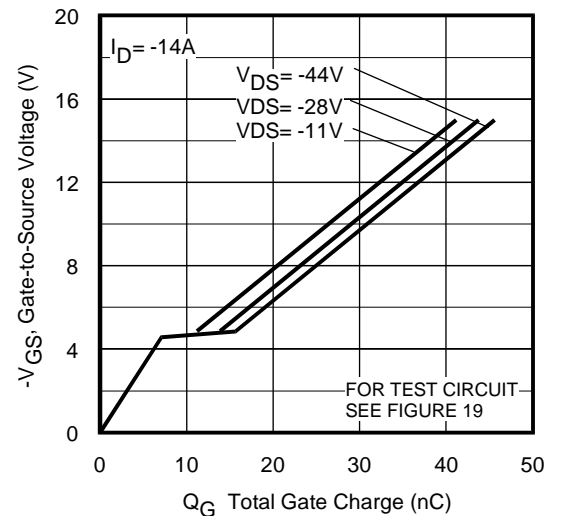
**Fig 3.** Typical Transfer Characteristics



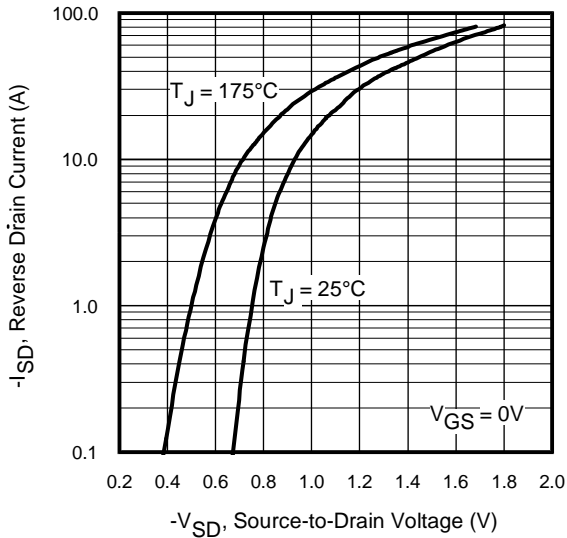
**Fig 4.** Normalized On-Resistance vs. Temperature



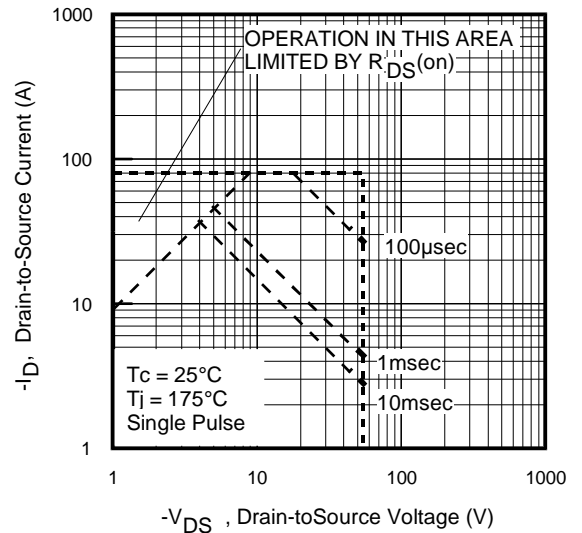
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage  
www.irf.com



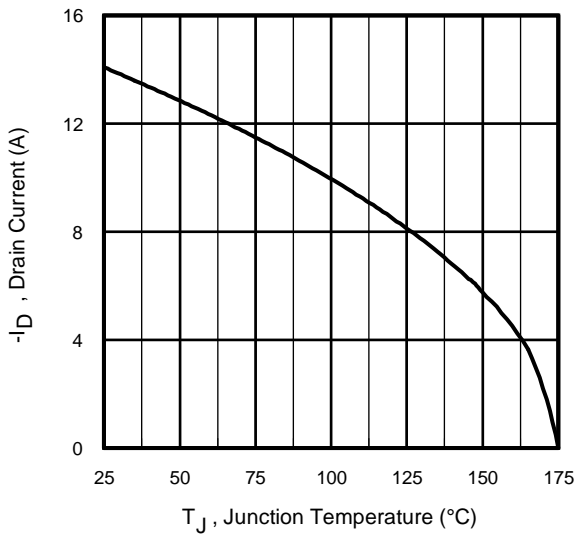
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage  
3



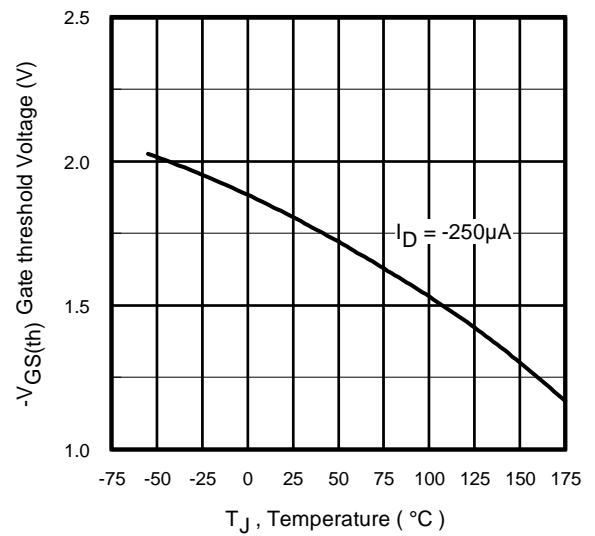
**Fig 7.** Typical Source-Drain Diode Forward Voltage



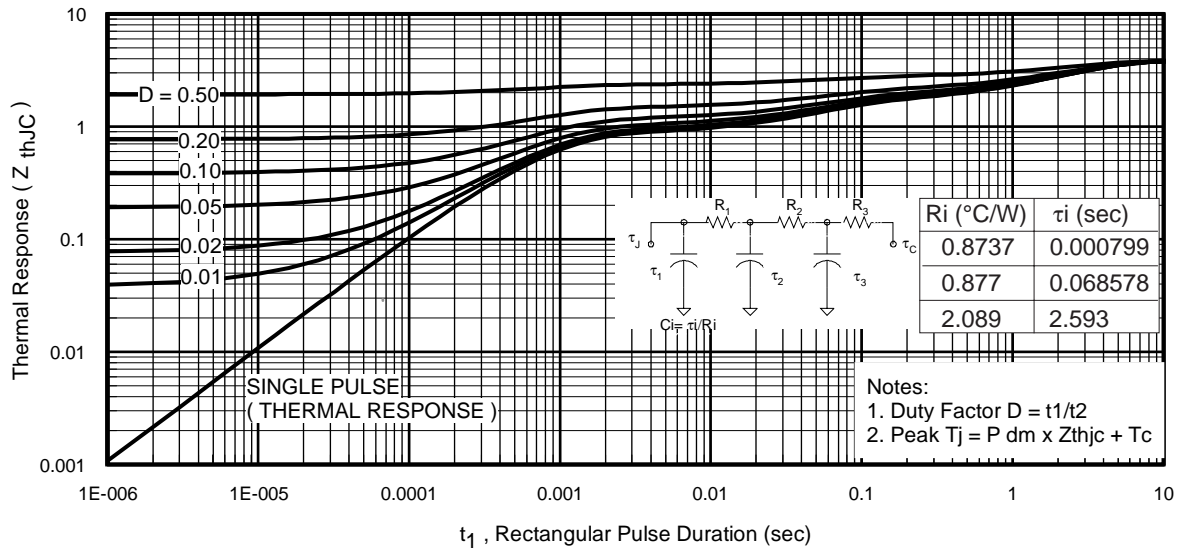
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Threshold Voltage vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

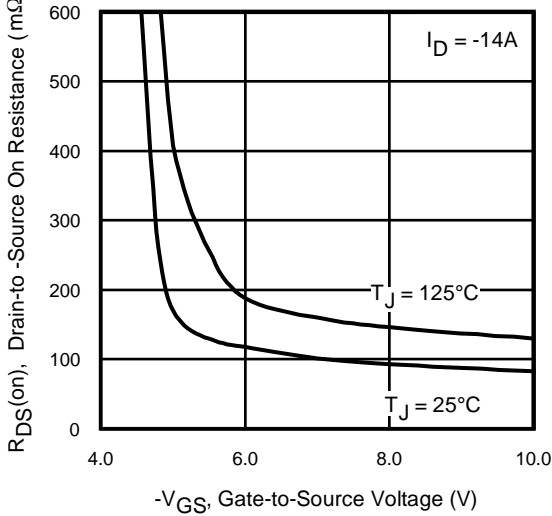


Fig 12. On-Resistance Vs. Gate Voltage

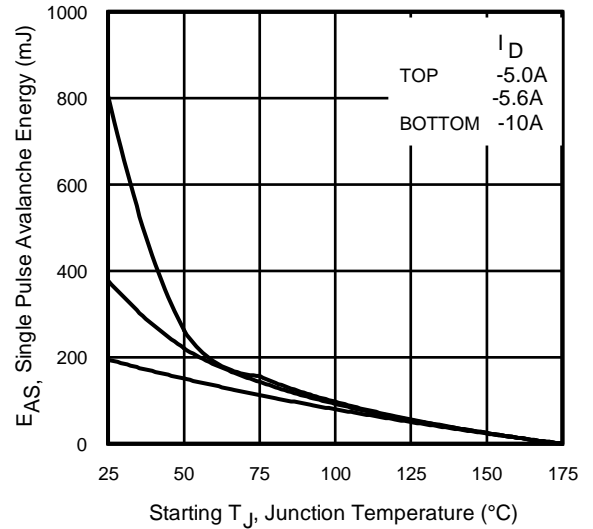


Fig 13. Maximum Avalanche Energy Vs. Drain Current

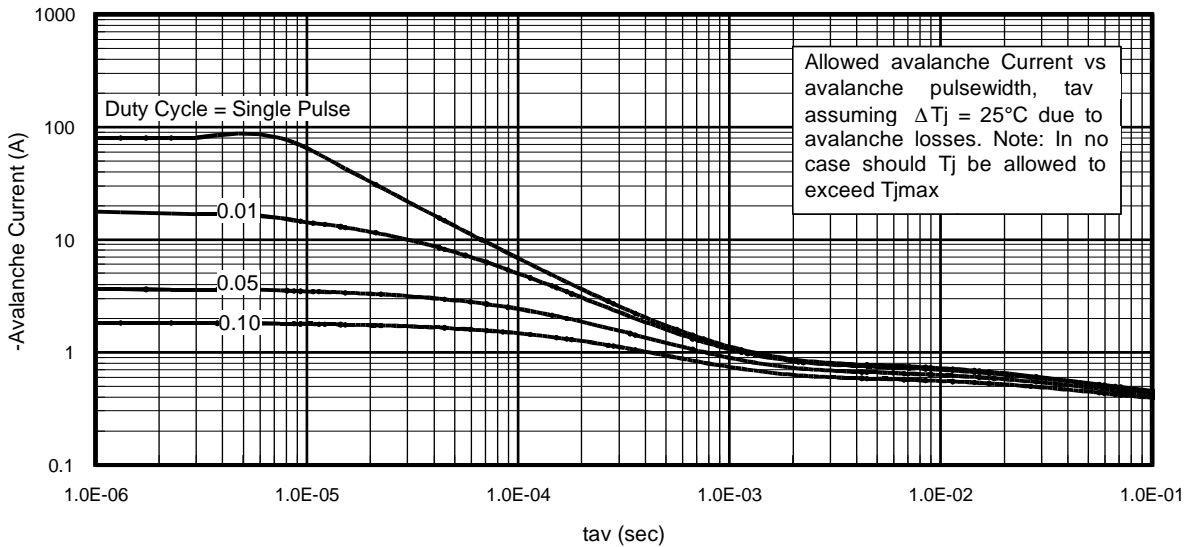


Fig 14. Typical Avalanche Current Vs. Pulsewidth

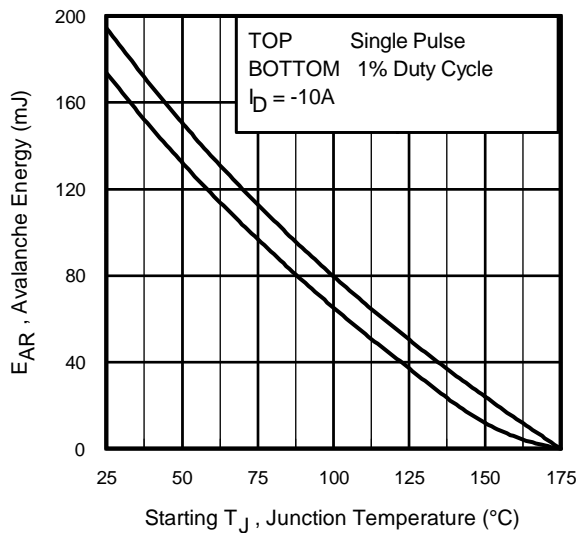


Fig 15. Maximum Avalanche Energy Vs. Temperature

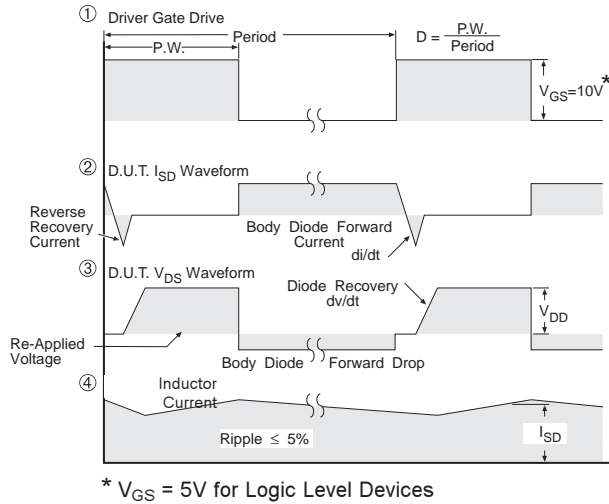
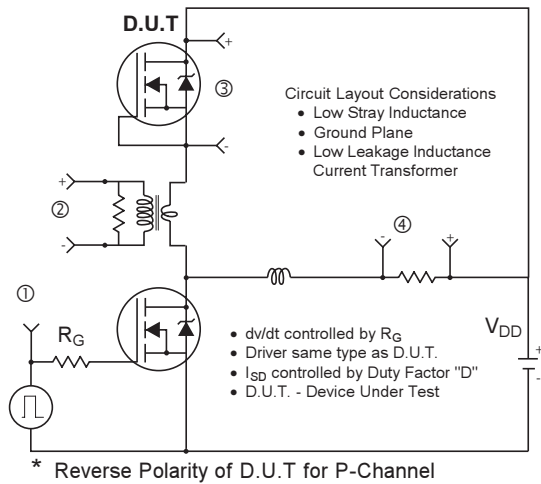
**Notes on Repetitive Avalanche Curves , Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 17a, 17b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

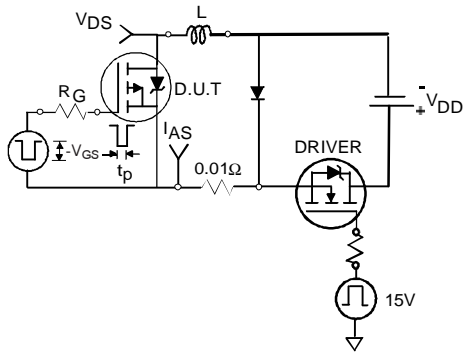
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{thJC} ]$$

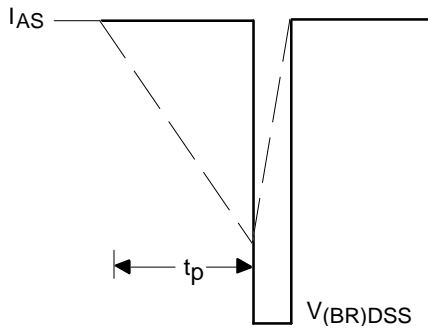
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



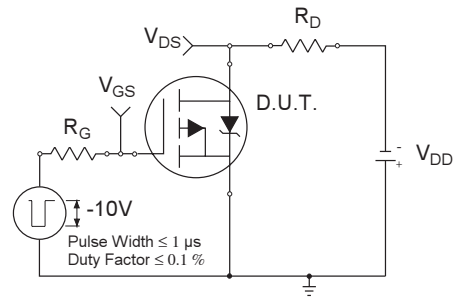
**Fig 16. Peak Diode Recovery  $dv/dt$  Test Circuit for P-Channel HEXFET<sup>®</sup> Power MOSFETs**



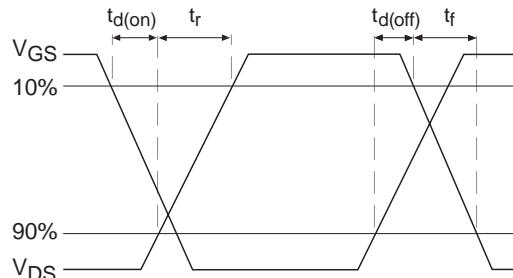
**Fig 17a. Unclamped Inductive Test Circuit**



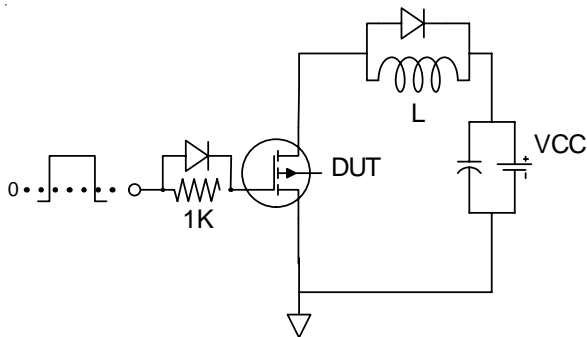
**Fig 17b. Unclamped Inductive Waveforms**



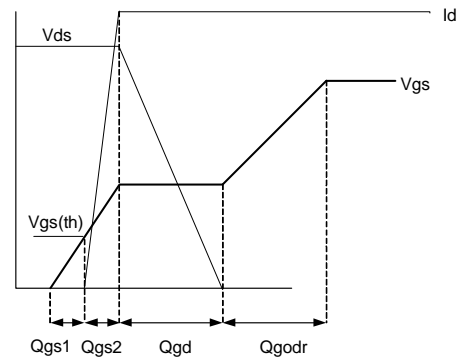
**Fig 18a. Switching Time Test Circuit**



**Fig 18b. Switching Time Waveforms**



**Fig 19a. Gate Charge Test Circuit**



**Fig 19b Gate Charge Waveform**

