1. General Description

The ISSC IS1002 is a highly integrated Bluetooth baseband controller providing capability for high data rate, short-range wireless communications in the 2.4 GHz ISM band. It is fully compliant with version 1.1 of Bluetooth specification and some important BT1.2 features. Specially engineered for low power consumption and cost effective solution, the ISSC IS1002 integrates a baseband controller, HCI controller, and Audio controller. It also integrates a Turbo 8051 processor with 160K mask ROM for program memory and 32K SRAM for data memory.

The ISSC IS1002 is also available with a Bluetooth compliant protocol stack, including hardware drivers, link manager (LM), and host controller interface (HCI).

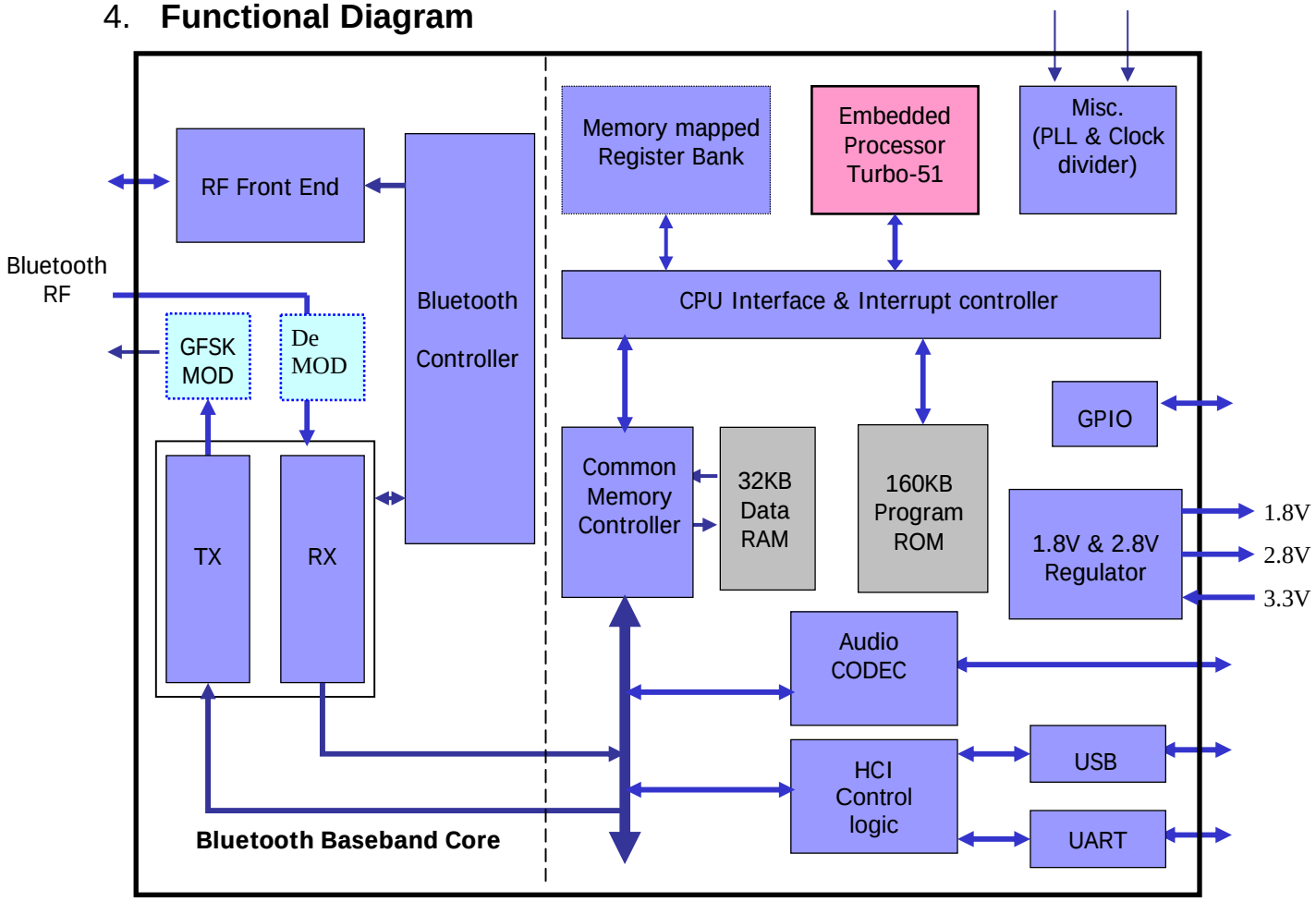
2. Features

- Compliant with Bluetooth Specification 1.1/1.2
- Full Bluetooth RF Interface & Lower Link Controller functions
- BlueRF Interfaces to leading Radio ICs
- Full-featured hardware link controller with low-power mode and efficient data movement architecture
- Hardware support for all Bluetooth 1.1 packet types including
    - Data packets: DM1, DM3, DM5; DH1, DH3, DH5; AUX, DV
    - Voice packets: HV1, HV2, HV3, DV
    - Link Control packets: ID, IQ, NULL, POLL, and FHS
- Flexible and robust voice CODEC algorithms (CVSD, A-law, μ-law), with 3 simultaneous SCO channels support.
- Baseband functions implemented in hardware such as Forward Error Correction (FEC), whitening, Header Error Check (HEC), Shorten Hamming Code, CRC generation/checking, and Encryption/De-encryption.
- Hardware permutation to speed up software Authentication.
- Point-to-multipoint support (Piconet).
- Scatternet support.
- BT1.2 Adaptive Frequency Hopping (AFH) supported.
- BT1.2 Fast Connection supported.
- Ultra-low low cost and power consumption features.
- Integrated Turbo 8051 processor.
- Integrated 32K bytes SRAM for common data buffer.
- Integrated 160K bytes Mask ROM for 8051 program memory.
- HCI universal connect interface provides access to other physical host interfaces (i.e. USB, UART.).
- Full-speed UART host interface.
- Selectable reference clock frequencies.
- Protocol Stack available, including drivers, link manager, and HCI.
- 48 QFN package

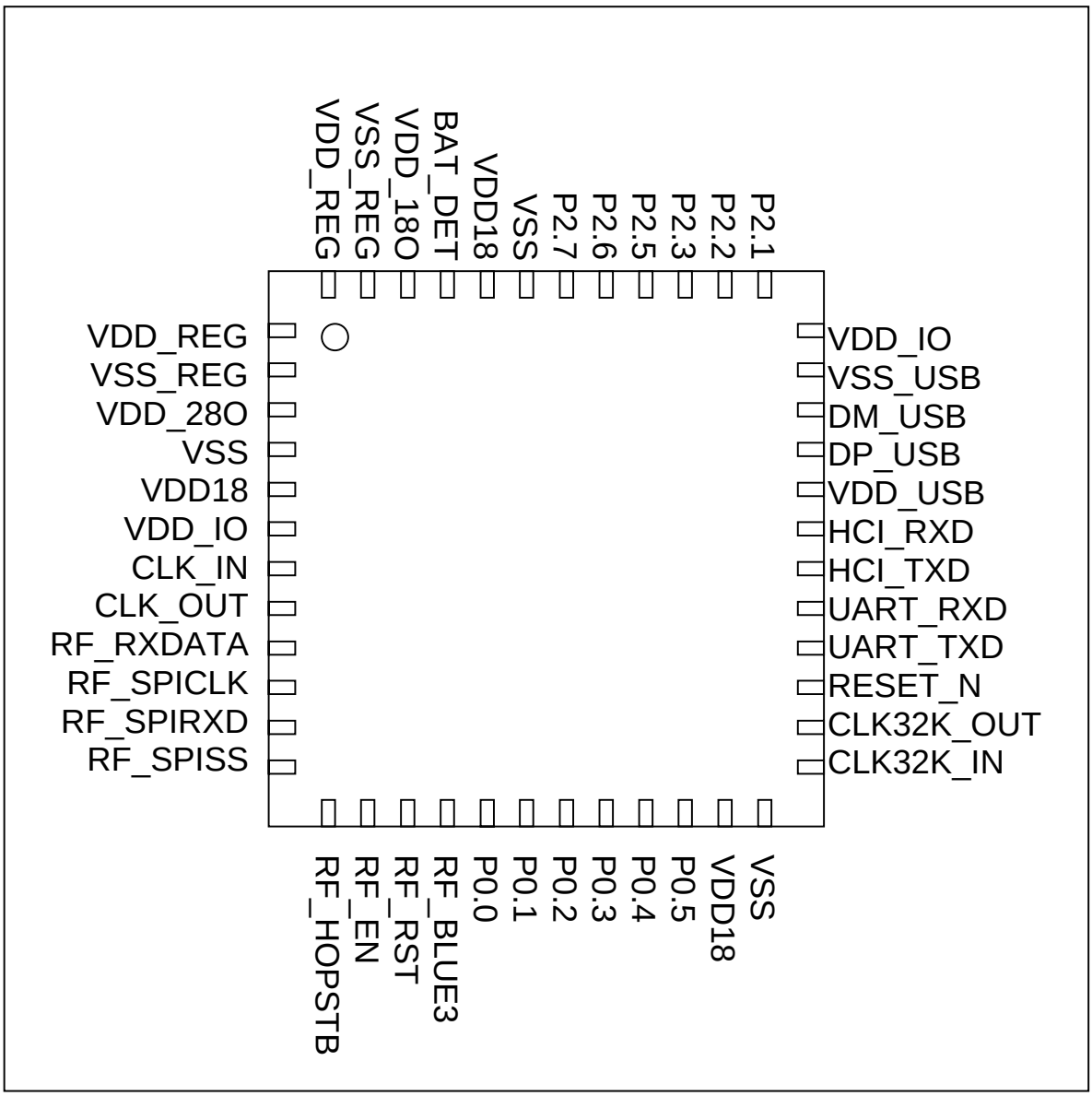
3. Applications

ISSC IS1002 can be applied to short-range wireless connectivity. Typical applications could include headsets, laptop and desktop computers, digital cameras, PDA's, and wireless computer peripherals such as printers and wireless LAN cards.

4. Functional Diagram



5. Pin Assignment



6. Pin Descriptions

Pin No.	I/O	Pin Name	Pin Descriptions
1	—	VDD_REG	Vdd input for regulator
2	—	VSS_REG	Regulator Vss
3	—	VDD28O	2.8V regulator output
4	—	VSS_IO_0	GND
5	—	SVDD18	1.8V Vdd
6	—	VDD_IO_0	3.3V Vdd
7	I	XTAL_I	Main crystal Input
8	O	XTAL_O	Main crystal output
9	I/O	bt_rf_rxdata	RF Control
10	O	bt_rf_spi_clk	RF Control
11	I/O	bt_rf_spi_rxd	RF Control
12	O	bt_rf_spi_ss	RF Control
13	O	bt_rf_hop_strb	RF Control
14	O	bt_rf_en	RF Control
15	O	bt_rf_rst	RF Control
16	O	bt_rf_blue3	RF Control
17	I/O	P0.0	8051 General Purpose I/O Port 0 bit 0
18	I/O	P0.1	8051 General Purpose I/O Port 0 bit 1
19	I/O	P0.2	8051 General Purpose I/O Port 0 bit 2
20	I/O	P0.3	8051 General Purpose I/O Port 0 bit 3
21	I/O	P0.4	8051 General Purpose I/O Port 0 bit 4
22	I/O	P0.5	8051 General Purpose I/O Port 0 bit 5
23	—	VDD_CORE	1.8Vdd
24	—	VSS_IO	Vss
25	I	CLK32K_I	32KHz crystal input
26	O	CLK32K_O	32KHz crystal input
27	I	RESET_n	External low reset
28	O	UART_TXD	UART Tx data
29	I	UART_RXD	UART Rx data
30	O	HCI_TXD	HCI UART Tx data
31	I	HCI_RXD	HCI UART Rx data
32	—	VDD_USB	3.3V Vdd for USB
33	I/O	DP_USB	
34	I/O	DM_USB	
35	—	VSS_USB	Vss for USB
36	—	VDD_IO	3.3V Vdd
37	I/O	P2.1	8051 General Purpose I/O Port 2 bit 1
38	I/O	P2.2	8051 General Purpose I/O Port 2 bit 2
39	I/O	P2.3	8051 General Purpose I/O Port 2 bit 3
40	I/O	P2.5	8051 General Purpose I/O Port 2 bit 5
41	I/O	P2.6	8051 General Purpose I/O Port 2 bit 6
42	I/O	P2.7	8051 General Purpose I/O Port 2 bit 7
43	—	VSS	GND

Pin No.	I/O	Pin Name	Pin Descriptions
44	—	VDD18	1.8V Vdd
45	I	Battery_in	Battery detection input
46	—	VDD18O	1.8V regulator output
47	—	VSS_REG	Vss for regulator
48	—	VDD_REG	Vdd for regulator

7. Functional Description

7.1 Overall Architecture

The ISSC IS1090 integrates an enhanced Bluetooth core, HCI controller, Audio controller and an embedded Turbo 8051 processor with 160K mask ROM for program memory and 32K SRAM for data memory. An innovative interconnection structure called the *Common-Memory Architecture* (*CMA*) is designed to provide a fast and flexible data movement scheme between the embedded processor, Bluetooth core, and peripheral hardware.

7.2 Embedded Processor

The embedded processor is the Turbo 8051 CPU. The embedded processor will be referred to as simply the *processor* or *8051* throughout the remainder of this document.

7.3 Common Memory Bus Architecture (CMA)

The functional diagram describing the CMA is shown in figure 1. A single-port synchronous interface is provided to memory. From this single port, the bandwidth is divided among the 6 interface busses described below:

- Embedded processor bus
- Baseband TX bus
- Baseband RX bus
- HCI TX bus
- HCI RX bus
- Audio bus

In addition, attached to the embedded processor bus are a register bank, a dedicated single-port memory (data segment 1), and flash memory (program segment). The processor coordinates all link control procedures and data movement using a set of pointer registers. For example, when an HCI packet (from the host via USB or UART) is received into the HCI buffer, the processor is interrupted. The processor can then read a status register to determine the HCI packet type and determine whether to set up the Baseband pointer registers for this memory region for RF-retransmission, or to otherwise directly perform packet processing with the CPU.

7.4 Memory Modules

The following list summarizes the available memory modules and the method by which they are controlled.

Memory Modules	Size in KBytes	Control method
processor program memory	160	controlled by processor
processor data memory	16/32	controlled by processor
common memory	16	controlled by AGU and CPU

7.5 Bluetooth Baseband Core

The following modules implemented in hardware constitute the Bluetooth baseband core.

7.5.1 Adaptive Frequency Hopping sequence generator

The adaptive frequency hopping sequence generator produces the correct hop frequency control sequence based on the Bluetooth clock, Bluetooth device address, and the current operating mode.

7.5.2 Access Code generation

The access code generates the access code based on the Lower Address Part (LAP) of the Bluetooth device address.

7.5.3 Access code Correlator

The access code is comprised of the preamble, sync word and trailer bits. The detection of the access code uses correlation to detect a valid access code.

7.5.4 Forward Error Correction (FEC)

Bluetooth uses two types of FEC: 1/3 repetition code and (15,10) shorten Hamming code respectively. The former basically repeats each transmitted bit three times while the latter has 15 bits of codeword which contains 5 parity bits. The code has capability of correction of all single-bit errors in each codeword.

7.5.5 Header Error Checking (HEC)

The purpose of HEC is to protect the header bits. Dedicated header error code generator calculates the HEC bits in the header of a transmitted packet. While on the receiver side, HEC detects corrupted headers.

7.5.6 Cyclic Redundancy Check (CRC)

A 16-bit CRC is adopted to protect payload data transmitted using certain types of Bluetooth packets.

7.5.7 Encryption/Decryption core

Information confidentiality can be protected by encryption of the packet payload. Dedicated encryption/decryption hardware is designed into the baseband core.

7.5.8 Authentication

The authentication in Bluetooth is based on SAFER+ algorithms. Effective architecture is implemented in hardware.

7.5.9 Received Signal Strength Indicator (RSSI) metric

The RSSI value is provided to the baseband processing hardware through an eight bit ADC (analog to digital converter).

7.5.10 Available Operating Clock Frequencies

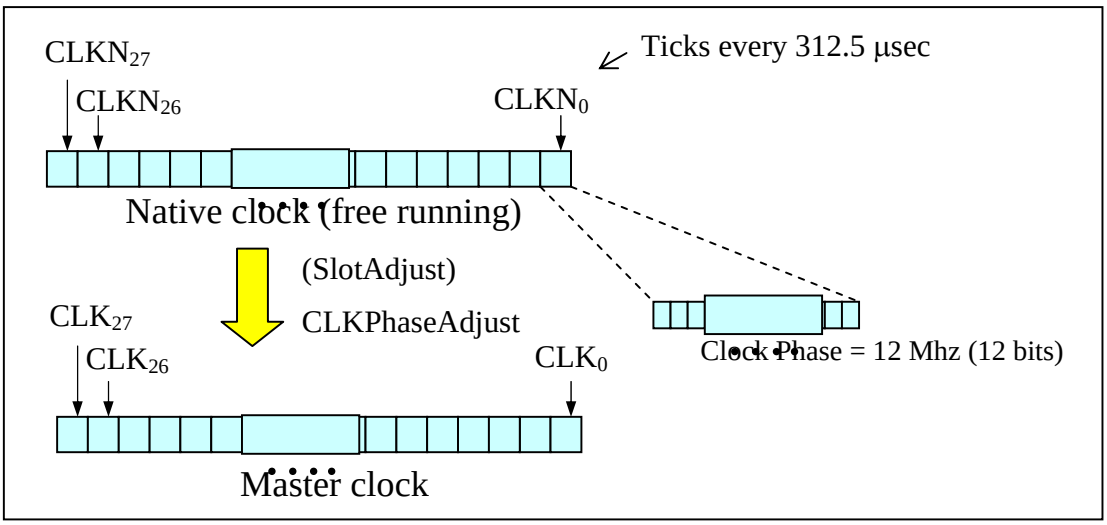
The ISSC IS1090 chip is capable of operating at the following frequencies: 48 MHz, 36 MHz, and 24 MHz. The following table shows the correct configuration for each frequency.

Rate_select1	Rate_select0	System Operation Frequency (MHz)
0	0	48
0	1	36
1	0	24
1	1	Reserved

7.6 Bluetooth Clock and Internal Timers

A Bluetooth standard 28-bit counter running at 3.2 kHz implements the native clock defined by Bluetooth specification. This clock provides the transmission and receiving timing of a half time slot (312.5 us). Another finer counter implemented in 12 bits is also provided as the phase of a half time slot. This phase information is very helpful when a Bluetooth slave wants to adapt to its master's clock. It is running at 12MHz. The counter is pre-scalable for the purpose of power saving operations. Figure 7.6.1 describes a standard Bluetooth native clock and master clock. The clock signal is also used as a slot boundary signal to trigger a baseband packet transmission or receipt. See appendix A for more information of the implementation.

Figure 7.6.1 Bluetooth Clocks



There are four timers provided by the system; two timers for TX/RX and general purpose use, and the other two for general purpose use. See definition of registers for task handler for details.

7.7 Task Handler:

The powerful pre-scheduling functions for the transceiver are realized by two sets of programmable timers, namely Task0Slot/PhaseTimer and Task1Slot/PhaseTimer. Each set of timers is associated with the task of transmission or receiving. When the timer is configured by firmware, it will automatically execute the TX or RX task at a specific time.

Sub-tasks and timing for a TX task remain to be defined.

Two additional timers for general purpose use are also provided.

7.8 HCI Control Logic for USB/UART:

A hardwired control logic is presented in front of the USB and UART devices for HCI protocol handling and packet buffering. This control logic is part of the HCI controller defined in Bluetooth specification. This logic is partially responsible for the HCI protocol handling to/from the host and it also maps the registers of the USB and UART devices indirectly to the 8051 such that the system can receive or send a HCI packet to/from the respective host interface. Major functions of this logic include:

- HCI packet formatter and de-formatter (identifying the packet type)
- Frame boundary determination, segmentation and reassembly of HCI packets.
- HCI packet transmission, receiving, and buffering (using common memory HCI buffer).
- Independent receive / transmit channels
- Universal device interface

7.9 Embedded UART:

An embedded UART (Universal Asynchronous Receiver Transmitter) is included in this design. In order to reduce gate count, only the functions required for the HCI logic are included. These include the following:

- Full-Duplex operation
- Programmable BAUD rate (using 16-bit input clock divider to obtain Baud Rate x16 clock base)
- 7 or 8 Data bits
- 1 or 2 Stop bits
- Even / Odd / Mark / Space / None Parity configurations
- Break Generation / Detection
- Maskable individual interrupts to CPU and combined Error interrupt to HCI
- Selectable Direct CPU interface or interface to HCI module

7.10 Voice CODEC

On the Bluetooth Specification, either a 64 kb/s log PCM format (A-Law or μ-Law) is used, or a CVSD (Continuous Variable Slope Delta Modulation) is used. ISSC IS1090 supports all coding schemes with conversion capabilities. In addition, the ISSC IS1090 Audio handling section also supports simultaneous 3-SCO channel operation. An external Codec must be added to perform the A/D and D/A functions.

7.11 Processor Memory Map[1]

The addressable memory space of the 8051 Turbo processor consists of a 64 kByte program space and a 64 kByte data space. The 64 kByte program space is mapped onto two pages in a larger 128 kByte memory space. This 128 kByte space may be physically implemented in a Flash or ROM device. The 64 kByte data space contains a single-port RAM, and the register bank. The maximum size of each memory component is as follows.

Memory Component	Physical Device	Maximum Size	Address range
program memory	Flash or ROM	128 kBytes	page 0: 0000h – ffffh page 1: 0000h – ffffh
data segment 1	single port RAM	32 kBytes	0000h – 7fffh
register segment	register bank	16 kBytes	8000h – bfffh
data segment 2	Common memory	13 kBytes	c000h – f3ffh
reserved			f400h – ffffh

7.12 Miscellaneous (Watchdog Timer, PLL, and Clock Divider)

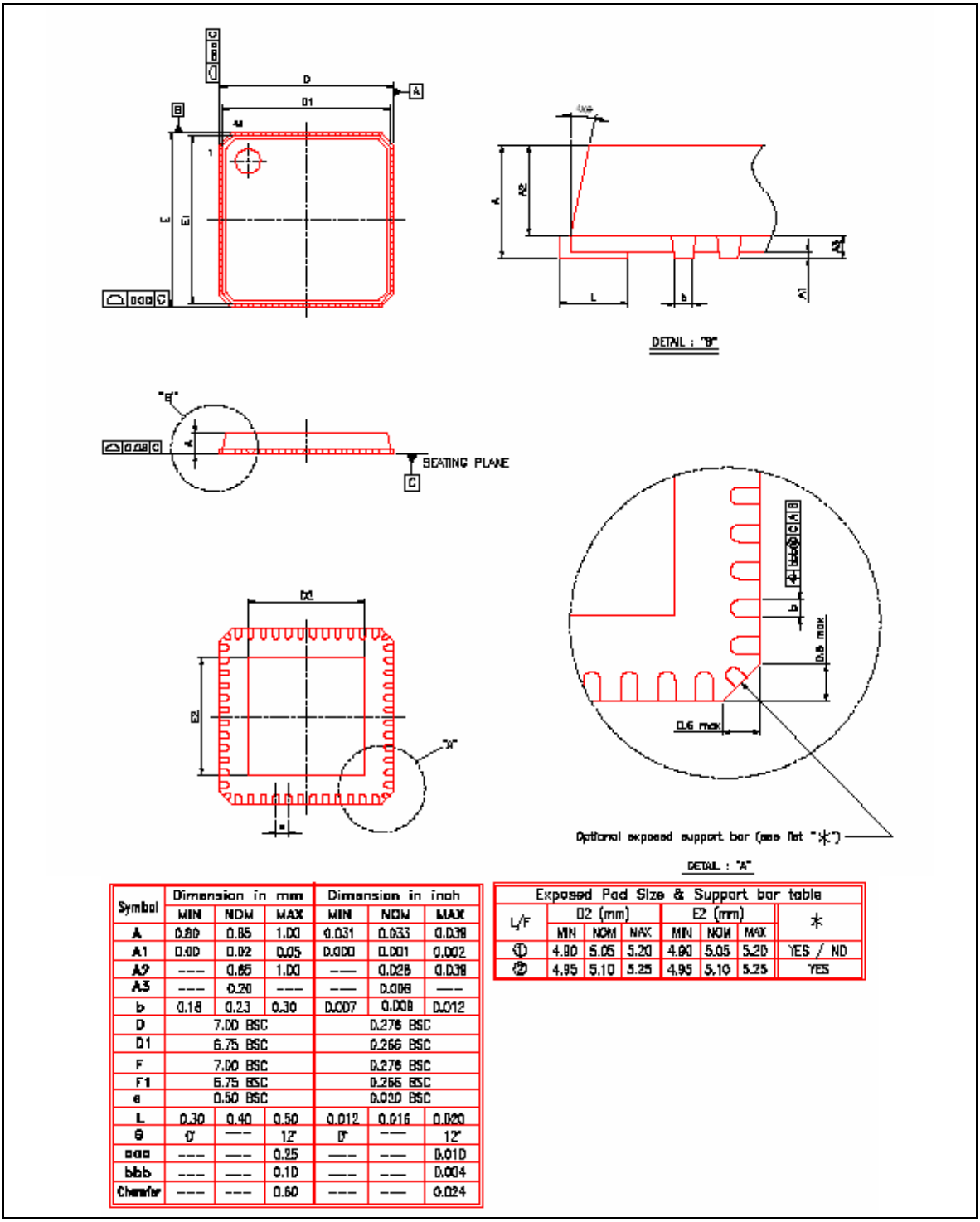
System related functions such as watchdog timer, Endian control, and interrupt vectors are also provided.

The purpose of the watchdog timer is to provide a reset to CPU in case when the CPU fails to service the watchdog timer in a pre-defined (programmable) period. In this situation, the CPU will be reset, and a flag will be set to indicate that the reset was due to a watchdog "timeout". In addition, it also provides resets to the other modules in Bluetooth baseband.

The build in PLL circuit will generate the required system clock of 48MHz, 36MHz or 24MHz from the oscillator clock. The clock divider will provide fixed frequencies of 12 MHz, 8KHz…for Bluetooth core and other peripheral hardware based on the input system clock of 48MHz, 36MHz, or 24MHz. All system clocks are 50% duty cycle.

[1] Additional memory spaces such as TX/RX buffer, USB/UART buffer are not addressable by 8051. Those special memory modules are controlled indirectly by 8051 via data router.

8. Package Information



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.000	0.001	0.002
A2	---	0.65	1.00	---	0.026	0.039
A3	---	0.20	---	---	0.008	---
b	0.18	0.23	0.30	0.007	0.009	0.012
D	7.00 BSC			0.276 BSC		
D1	6.75 BSC			0.266 BSC		
E	7.00 BSC			0.276 BSC		
E1	6.75 BSC			0.266 BSC		
e	0.50 BSC			0.020 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020
θ	0°	---	12°	0°	---	12°
aaa	---	---	0.25	---	---	0.010
bbb	---	---	0.10	---	---	0.004
Chamfer	---	---	0.60	---	---	0.024

Exposed Pad Size & Support bar table							
L/F	D2 (mm)			E2 (mm)			*
	MIN	NOM	MAX	MIN	NOM	MAX	
①	4.80	5.05	5.20	4.80	5.05	5.20	YES / NO
②	4.95	5.10	5.25	4.95	5.10	5.25	YES

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