IS41LV32256

256K x 32 (8-Mbit) EDO DYNAMIC RAM 3.3V, 100/83/66 MHz

SEPTEMBER 2000

FEATURES

- 262,144-word by 32-bit organization
- Single +3.3V ± 0.3V power supply
- Four $\overline{CAS}$ inputs for Byte Write and Byte Read control
- Refresh modes: $\overline{RAS}$-Only, $\overline{CAS}$-Before-$\overline{RAS}$ (CBR), and Hidden
- 512-cycle refresh in 8 ms
- Fast Page Mode with Extended Data Out
- 100-pin PQFP, TQFP package

DESCRIPTION

The *ISSI* IS41LV32256 is organized in a 262,122 x 32-bit CMOS Dynamic Random Access Memory. Four $\overline{CAS}$ signals facilitate execution of Byte Read and Byte Write operations. A very fast EDO cycle time of 10 ns allows an operating frequency of 100 MHz and makes the IS41LV32256 an ideal frame buffer memory for graphics applications.

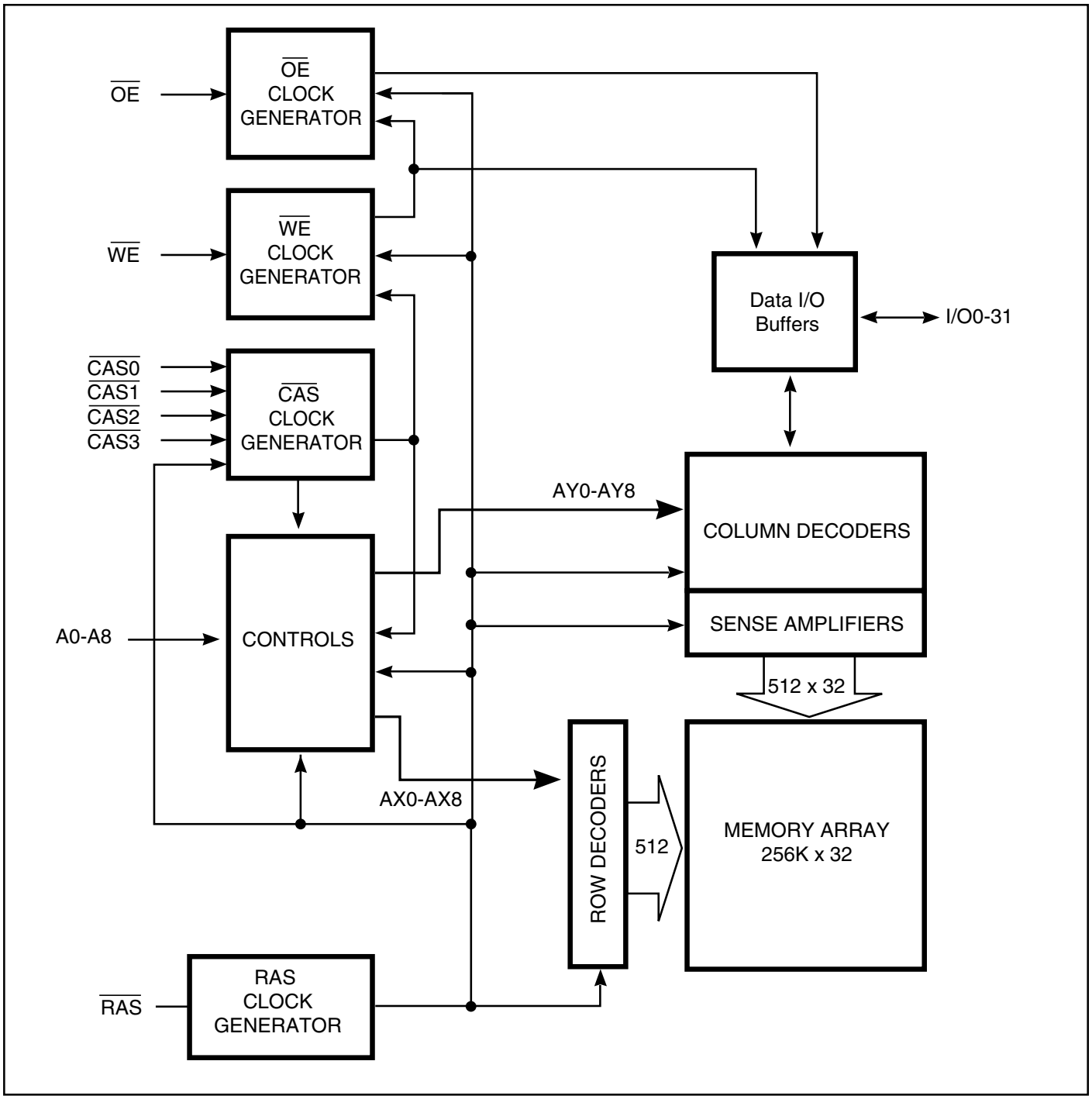
The IS41LV32256 is compatible with JEDEC standard SGRAMs. This 8-Mbit EDO memory offers a significantly lower latency and a faster memory cycle than the SGRAM. *ISSI*'s IS41LV32256 3.3V 256K x 32 device is pin/voltage compatible with all standard SGRAM parts.

The IS41LV32256 is available in a 100-pin PQFP and TQFP package.

KEY TIMING PARAMETERS

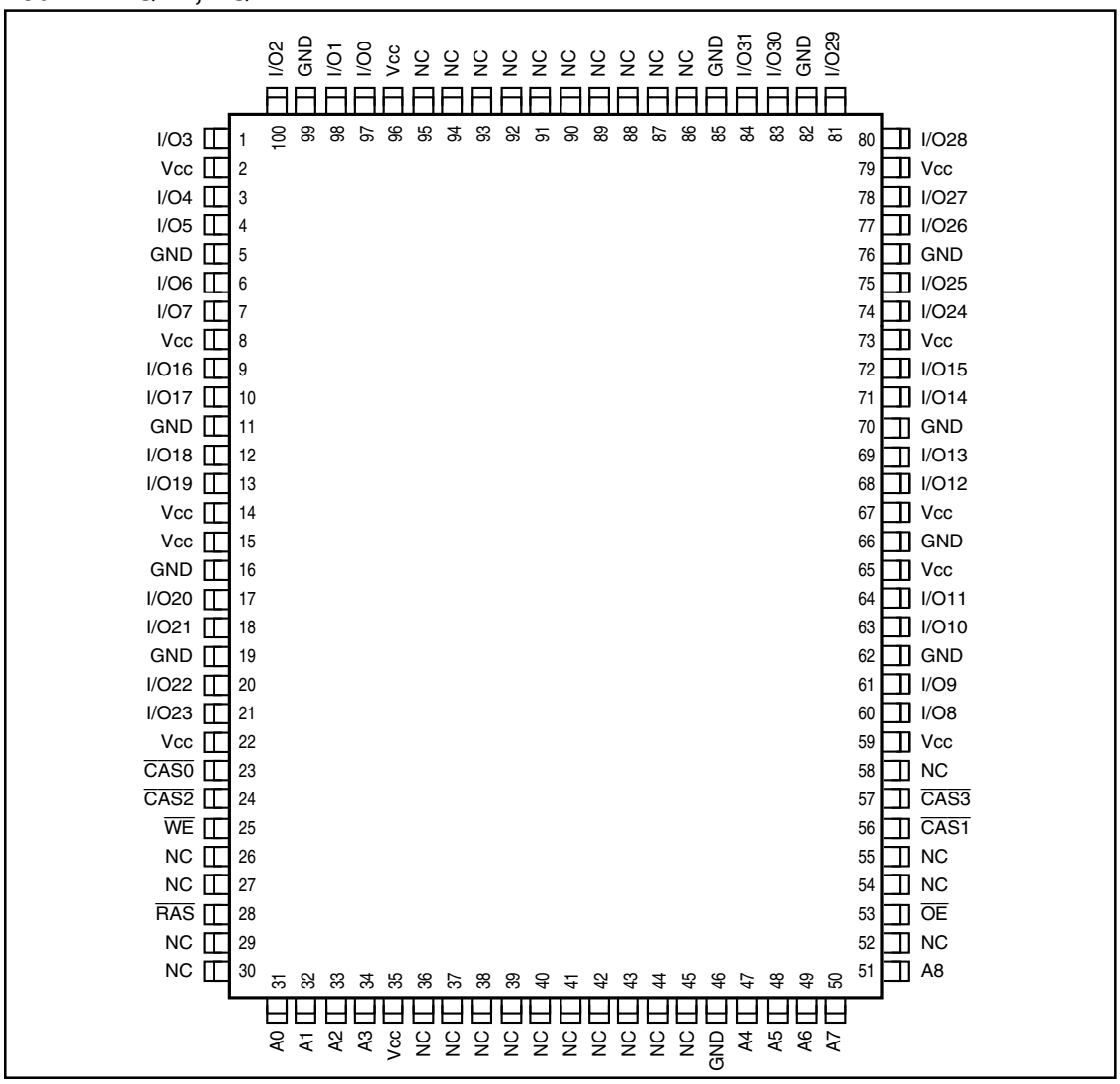
Parameter	-28	-30	-35	Unit
Max. $\overline{RAS}$ Access Time (t_{RAC})	28	30	35	ns
Max. $\overline{CAS}$ Access Time (t_{CAC})	9	9	10	ns
Max. Column Address Access Time (t_{AA})	15	16	18	ns
Max. $\overline{OE}$ Access Time (t_{OE})	9	9	10	ns
Min. Read/Write Cycle Time (t_{RC})	48	53	60	ns
Min. EDO Cycle Time (t_{PC})	12	12	15	ns

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

100-Pin PQFP, TQFP



PIN DESCRIPTIONS

A0-A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS0}$	Column Address Strobe for First Byte (I/O0-I/O7)
$\overline{CAS1}$	Column Address Strobe for Second Byte (I/O8-I/O15)
$\overline{CAS2}$	Column Address Strobe for Third Byte (I/O16-I/O23)
$\overline{CAS3}$	Column Address Strobe for Fourth Byte (I/O24-I/O31)
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O0-I/O31	Data Inputs/Outputs
Vcc	+3.3V Supply
GND	Ground
NC	No Connection: This pin should be left unconnected or tied to ground.

TRUTH TABLE

Function	$\overline{RAS}$	$\overline{CAS0}$	$\overline{CAS1}$	$\overline{CAS2}$	$\overline{CAS3}$	$\overline{WE}$	$\overline{OE}$	Address	I/O
Standby	H	H	H	H	H	X	X	X	High-Z
Read: Double Word	L	L	L	L	L	H	L	ROW/COL	DOUT
Read: 1st Byte	L	L	H	H	H	H	L	ROW/COL	I/O0-7=DOUT; I/O8-31=High-Z
Read: 2nd Byte	L	H	L	H	H	H	L	ROW/COL	I/O0-7=High-Z; I/O8-15=DOUT; I/O16-31=High-Z
Read: 3rd Byte	L	H	H	L	H	H	L	ROW/COL	I/O0-15=High-Z; I/O16-23=DOUT; I/O24-31=High-Z
Read: 4th Byte	L	H	H	H	L	H	L	ROW/COL	I/O0-23=High-Z; I/O24-31=DOUT
Write: Double Word (Early)	L	L	L	L	L	L	X	ROW/COL	DIN
Write: 1st Byte (Early)	L	L	H	H	H	L	X	ROW/COL	I/O0-7=DIN; I/O8-31=X
Write: 2nd Byte (Early)	L	H	L	H	H	L	X	ROW/COL	I/O0-8=X; I/O8-15=DIN; I/O16-31=X
Write: 3rd Byte (Early)	L	H	H	L	H	L	X	ROW/COL	I/O0-15=X; I/O16-23=DIN; I/O24-31=X
Write: 4th Byte (Early)	L	H	H	H	L	L	X	ROW/COL	I/O0-23=X; I/O24-31=DIN
Read-Write[1,2]	L	L	L	L	L	HØL	LØH	ROW/COL	DOUTØDIN
Fast-Page-Mode Read: EDO[2] 1st Cycle:	L	HØL	HØL	HØL	HØL	H	L	ROW/COL	DOUT
Subsequent Cycles:	L	HØL	HØL	HØL	HØL	H	L	COL	DOUT
Fast-Page-Mode Read: High-Z[2] 1st Cycle:	L	HØL	HØL	HØL	HØL	H	HØL	ROW/COL	DOUT
Subsequent Cycles:	L	HØL	HØL	HØL	HØL	H	HØL	COL	DOUT
Fast-Page-Mode Write: (Early)[1] 1st Cycle:	L	HØL	HØL	HØL	HØL	L	X	ROW/COL	DIN
Subsequent Cycles:	L	HØL	HØL	HØL	HØL	L	X	COL	DIN
Fast-Page-Mode Read-Write[1,2] 1st Cycle:	L	HØL	HØL	HØL	HØL	HØL	LØH	ROW/COL	DOUTØDIN
Subsequent Cycles:	L	HØL	HØL	HØL	HØL	HØL	LØH	COL	DOUTØDIN
Hidden Refresh Read[2]	LØHØL	L	L	L	L	H	L	ROW/COL	DOUT
Hidden Refresh Write[1]	LØHØL	L	L	L	L	L	X	ROW/COL	DINØHigh-Z
$\overline{RAS}$-Only Refresh	L	H	H	H	H	X	X	ROW	High-Z
CBR Refresh[3]	HØL	L	L	L	L	X	X	X	High-Z

Notes:
1. BYTE WRITE may be executed with $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$ or $\overline{CAS3}$ active.
2. BYTE READ may be executed with $\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$ or $\overline{CAS3}$ active.
3. Only one $\overline{CAS}$ signal ($\overline{CAS0}$, $\overline{CAS1}$, $\overline{CAS2}$ or $\overline{CAS3}$) must be active.

POWER-ON

The initial application of the V_{CC} supply requires a 200-µs wait followed by a minimum of any eight initialization cycles containing a $\overline{RAS}$ clock. During Power-On, the V_{CC} current is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} or be held at a valid V_{IH} during Power-On to avoid current surges.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Parameters	Rating	Unit
t_A	Ambient Temperature Under Bias	–1.0 to +80	°C
t_{STG}	Storage Temperature	–50 to +125	°C
V_T	Voltage Relative to GND	–1.0 to +5.5	V
I_{OUT}	Data Output Current	50	mA
P_D	Power Dissipation	1.0	W

Note:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS(1) (T_A = 0°C to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply	3.0	3.3	3.6	V
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	V
V_{IL}	Input Low Voltage	–0.5	—	0.4	V

Note:
1. Voltages are referenced to GND.

CAPACITANCE(1,2)

Symbol	Parameter	Max.	Unit
C_{IN}	Input Capacitance	5	pF
C_{IO}	Data Input/Output Capacitance	7	pF

Notes:
1. Capacitance is sampled and 100% tested.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V.

DC CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Condition	-28 Min.	-28 Max.	-30 Min.	-30 Max.	-35 Min.	-35 Max.	Units
V_{IH}	Input HIGH (Logic 1) Voltage, All Inputs	—	2.0	Vcc + 0.5	2.0	Vcc + 0.5	2.0	Vcc + 0.5	V
V_{IL}	Input LOW (Logic 1) Voltage, All Inputs	—	–0.5	0.8	–0.5	0.8	–0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OH} = –2 mA	2.4	Vcc	2.4	Vcc	2.4	Vcc	V
V_{OL}	Output LOW Voltage	I_{OL} = 2 mA	0	0.4	0	0.4	0	0.4	V
I_{LI}	Input Leakage Current	0V < V_{IN} < V_{CC}	–10	10	–10	10	–10	10	µA
I_{LO}	Output Leakage Current	0V < V_{OUT} < 3.6V; Output Disable	–10	10	–10	10	–10	10	µA
$I_{CC}1$	Average Power Supply Current (Operating)[2,3,15,16]	$\overline{RAS}$, $\overline{CAS}$ Cycling; t_{RC} = Min.	—	250	—	250	—	240	mA
$I_{CC}2$	Power Supply Current (Standby)	$\overline{RAS}$, $\overline{CAS}$ = V_{IH}	—	2.5	—	2.5	—	2.5	mA
Icc3	Average Power Supply Current ($\overline{RAS}$-Only Refresh)[2,3,15,16]	$\overline{RAS}$ = Cycling; $\overline{CAS}$ = V_{IH}; t_{RC} = Min.	—	250	—	250	—	240	mA
$I_{CC}4$	Average Power Supply Current (Fast Page Mode)[2,3,15,18]	$\overline{RAS}$ = V_{IL}; $\overline{CAS}$ = Cycling; t_{PC} = Min.	—	230	—	230	—	220	mA
$I_{CC}5$	Average Power Supply Current ($\overline{CAS}$-before-$\overline{RAS}$ Refresh)[2,3,15.16]	$\overline{RAS}$ = Cycling; $\overline{CAS}$-before-$\overline{RAS}$	—	250	—	250	—	240	mA
$I_{CC}6$	CMOS Standby Current	$\overline{RAS}$, $\overline{CAS}$ = V_{CC} –0.2V	—	600	—	600	—	600	µA

AC CHARACTERISTICS[1,2,3,4,5,6] (Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-28 Min.	-28 Max.	-30 Min.	-30 Max.	-35 Min.	-35 Max.	Units
t_{RC}	Random READ or WRITE Cycle Time	48	—	53	—	60	—	ns
t_{RAC}	Access Time from $\overline{RAS}$[6, 7]	—	28	—	30	—	35	ns
t_{CAC}	Access Time from $\overline{CAS}$[6, 8, 15]	—	9	—	9	—	10	ns
t_{AA}	Access Time from Column-Address[6]	—	15	—	16	—	18	ns
t_{RAS}	$\overline{RAS}$ Pulse Width	28	10K	30	10K	35	10K	ns
t_{RP}	$\overline{RAS}$ Precharge Time	17	—	18	—	20	—	ns
t_{CAS}	$\overline{CAS}$ Pulse Width[26]	5	10K	5	10K	6	10K	ns
t_{CP}	$\overline{CAS}$ Precharge Time[9, 25]	5	—	5	—	5	—	ns
t_{CSH}	$\overline{CAS}$ Hold Time [21]	28	—	30	—	35	—	ns
t_{RCD}	$\overline{RAS}$ to CAS Delay Time[10, 20]	10	19	10	21	11	28	ns
t_{ASR}	Row-Address Setup Time	0	—	0	—	0	—	ns
t_{RAH}	Row-Address Hold Time	6	—	6	—	7	—	ns
t_{ASC}	Column-Address Setup Time[20]	0	—	0	—	0	—	ns
t_{CAH}	Column-Address Hold Time[20]	5	—	5	—	6	—	ns
t_{AR}	Column-Address Hold Time (referenced to $\overline{RAS}$)	21	—	22	—	25	—	ns
t_{RAD}	$\overline{RAS}$ to Column-Address Delay Time[11]	8	13	8	15	9	16	ns
t_{RAL}	Column-Address to $\overline{RAS}$ Lead Time	15	—	16	—	18	—	ns
t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0	—	0	—	0	—	ns
t_{RSH}	$\overline{RAS}$ Hold Time[27]	7	—	7	—	8	—	ns

(Continued)

AC CHARACTERISTICS[1,2,3,4,5,6] (Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-28 Min.	-28 Max.	-30 Min.	-30 Max.	-35 Min.	-35 Max.	Units
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z[15, 29]	3	—	3	—	3	—	ns
t_{CRP}	$\overline{CAS}$ to RAS Precharge Time[21]	5	—	5	—	5	—	ns
t_{OD}	Output Disable Time[19, 28, 29]	3	15	3	15	3	15	ns
t_{OE}	Output Enable Time[15, 16]	—	9	—	9	—	10	ns
t_{OEHC}	$\overline{OE}$ HIGH Hold Time from $\overline{CAS}$ HIGH	10	—	10	—	10	—	ns
t_{OEP}	$\overline{OE}$ HIGH Pulse Width	10	—	10	—	10	—	ns
t_{OES}	$\overline{OE}$ LOW to $\overline{CAS}$ HIGH Setup Time	5	—	5	—	5	—	ns
t_{RCS}	Read Command Setup Time[17, 20]	0	—	0	—	0	—	ns
t_{RRH}	Read Command Hold Time (referenced to $\overline{RAS}$)[12]	0	—	0	—	0	—	ns
t_{RCH}	Read Command Hold Time (referenced to $\overline{CAS}$)[12, 17, 21]	0	—	0	—	0	—	ns
t_{WCH}	Write Command Hold Time[17, 27]	5	—	5	—	5	—	ns
t_{WCR}	Write Command Hold Time (referenced to $\overline{RAS}$)[17]	21	—	22	—	24	—	ns
t_{WP}	Write Command Pulse Width[17]	5	—	5	—	6	—	ns
t_{WPZ}	$\overline{WE}$ Pulse Widths to Disable Outputs	10	—	10	—	10	—	ns
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time[17]	7	—	7	—	8	—	ns
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time[17, 21]	5	—	5	—	8	—	ns
t_{WCS}	Write Command Setup Time[14, 17, 20]	0	—	0	—	0	—	ns
t_{DHR}	Data-in Hold Time (referenced to $\overline{RAS}$)	21	—	22	—	24	—	ns
t_{ACH}	Column-Address Setup Time to $\overline{CAS}$ Precharge during WRITE Cycle	15	—	15	—	15	—	ns
t_{OEH}	$\overline{OE}$ Hold Time from $\overline{WE}$ during READ-MODIFY-WRITE cycle[18]	5	—	5	—	6	—	ns
t_{DS}	Data-In Setup Time[15, 22]	0	—	0	—	0	—	ns
t_{DH}	Data-In Hold Time[15, 22]	5	—	5	—	6	—	ns
t_{RWC}	READ-MODIFY-WRITE Cycle Time	73	—	73	—	80	—	ns
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time during READ-MODIFY-WRITE Cycle[14]	40	—	40	—	45	—	ns
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time[14, 20]	18	—	18	—	20	—	ns
t_{AWD}	Column-Address to $\overline{WE}$ Delay Time[14]	24	—	25	—	30	—	ns
t_{PC}	EDO Page Mode READ or WRITE Cycle Time[24]	12	—	12	—	15	—	ns
t_{RASP}	$\overline{RAS}$ Pulse Width in EDO Page Mode	28	100K	30	100K	35	100K	ns
t_{CPA}	Access Time from $\overline{CAS}$ Precharge[15]	—	17	—	18	—	21	ns
t_{PRWC}	EDO Page Mode READ-WRITE Cycle Time[24]	34	—	35	—	40	—	ns
t_{CHO}	Data Output Hold after $\overline{CAS}$ LOW	3	—	3	—	3	—	ns
t_{OFF}	Output Buffer Turn-Off Delay from $\overline{CAS}$ or $\overline{RAS}$[13,15,19, 29]	3	7	3	7	3	15	ns
t_{WHZ}	Output Disable Delay from $\overline{WE}$	3	10	3	10	3	15	ns

(Continued)

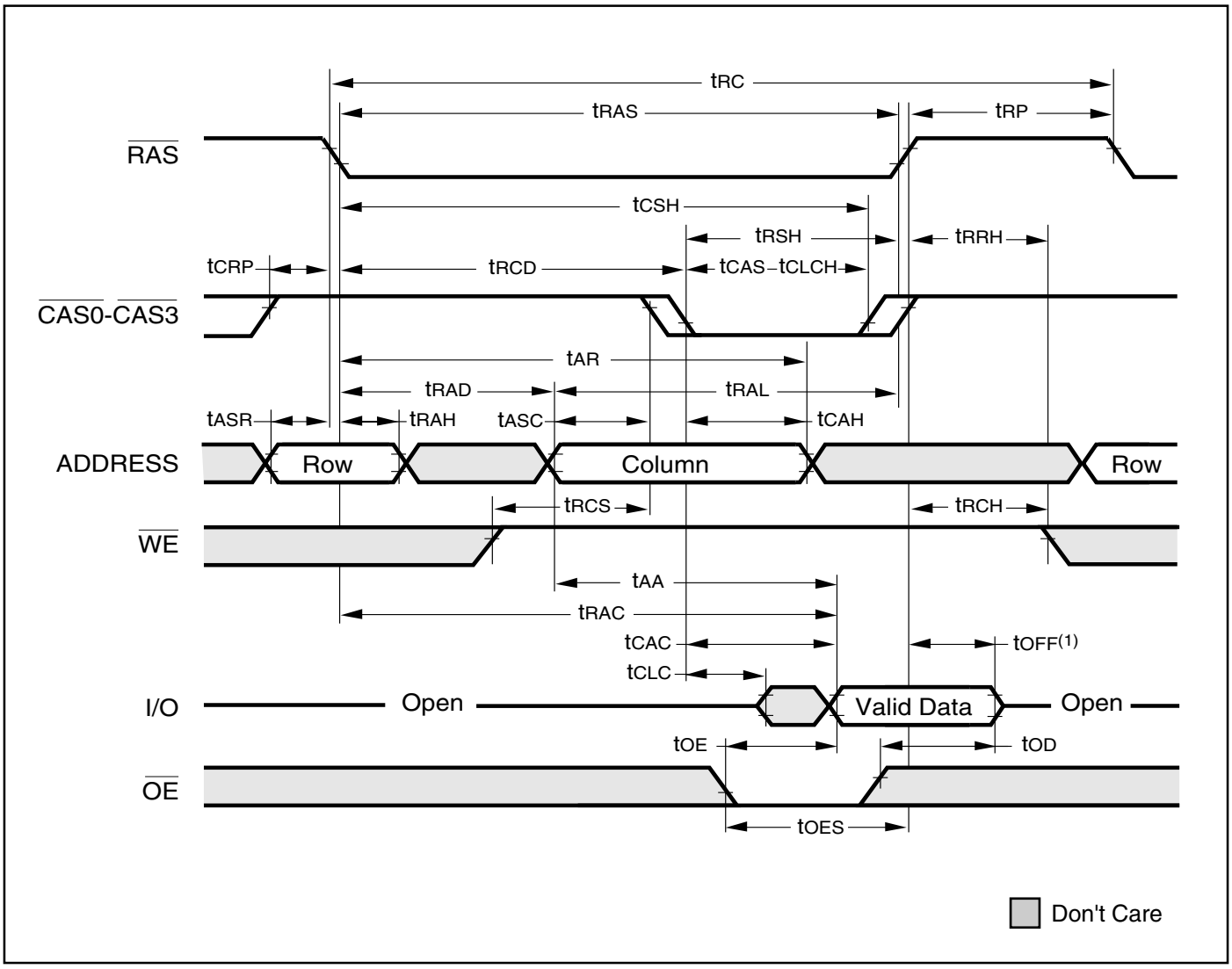
AC CHARACTERISTICS[1,2,3,4,5,6] (Recommended Operating Conditions unless otherwise noted.)

Symbol	Parameter	-28 Min.	-28 Max.	-30 Min.	-30 Max.	-35 Min.	-35 Max.	Units
t_{CLCH}	Last $\overline{CAS}$ going LOW to First $\overline{CAS}$ returning HIGH[23]	10	—	10	—	10	—	ns
t_{CSR}	$\overline{CAS}$ Setup Time (CBR REFRESH)[30, 20]	5	—	5	—	8	—	ns
t_{CHR}	$\overline{CAS}$ Hold Time (CBR REFRESH)[30, 21]	7	—	7	—	8	—	ns
t_{ORD}	$\overline{OE}$ Setup Time prior to $\overline{RAS}$ during HIDDEN REFRESH Cycle	0	—	0	—	0	—	ns
t_{REF}	Refresh Period (512 Cycles)	—	8	—	8	—	8	ms
t_T	Transition Time (Rise or Fall)[2, 3]	1	50	1	50	1	50	ns

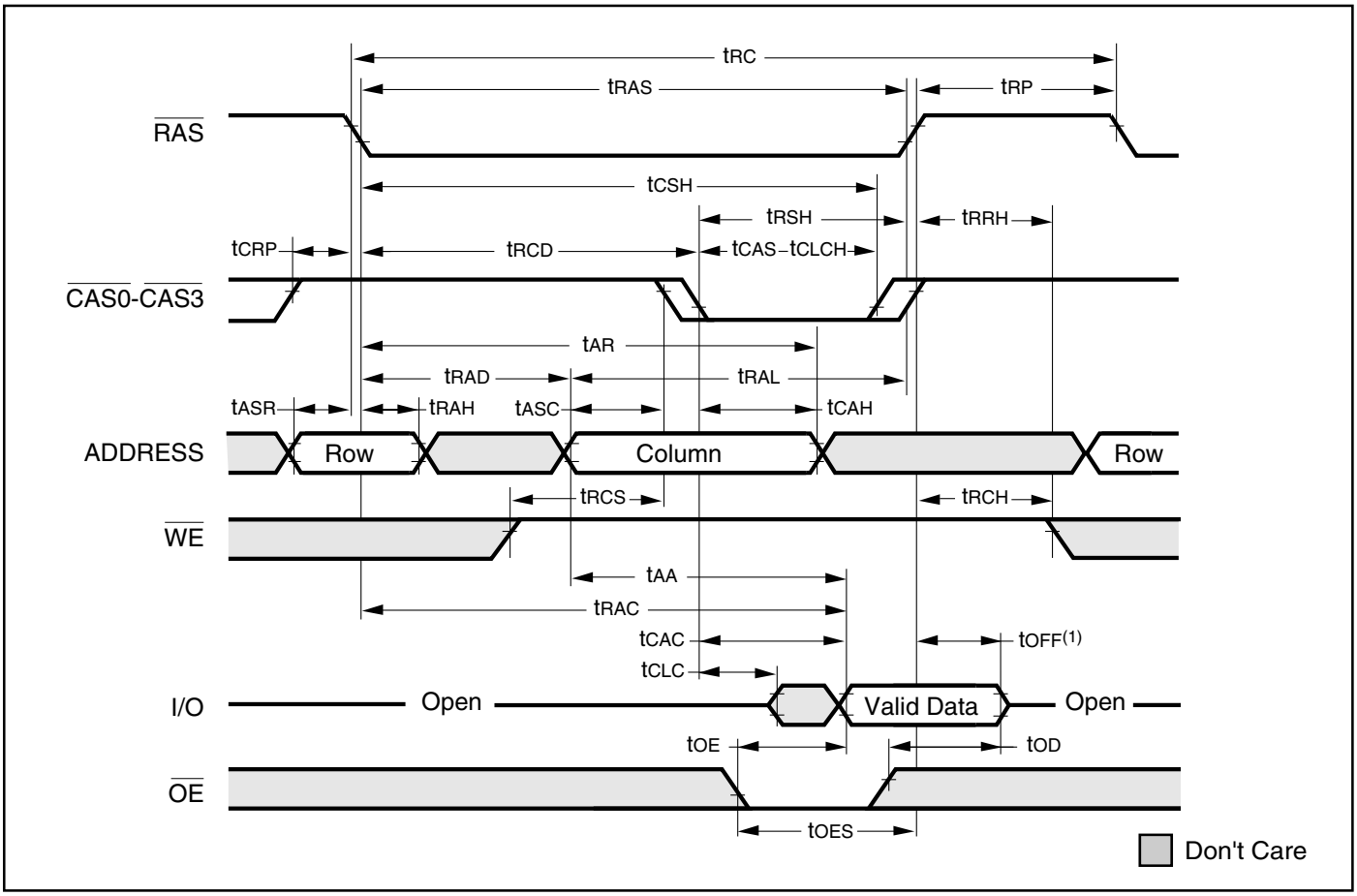
Notes:

1. An initial pause of 200 µs is required after power-up followed by eight $\overline{RAS}$ refresh cycle ($\overline{RAS}$-Only or CBR) before proper device operation is assured. The eight $\overline{RAS}$ cycles wake-up should be repeated any time the t_{REF} refresh requirement is exceeded.
2. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times, are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) and assume to be 1 ns for all inputs.
3. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. If $\overline{CAS}$ and $\overline{RAS}$ = V_{IH}, data output is High-Z.
5. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
6. Measured with a load equivalent to one TTL gate and 50 pF.
7. Assumes that t_{RCD} - t_{RCD} (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
8. Assumes that t_{RCD} • t_{RCD} (MAX).
9. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, data out will be maintained from the previous cycle. To initiate a new cycle and clear the data output buffer, $\overline{CAS}$ and $\overline{RAS}$ must be pulsed for t_{CP}.
10. Operation with the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, access time is controlled exclusively by t_{CAC}.
11. Operation within the t_{RAD} (MAX) limit ensures that t_{RCD} (MAX) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, access time is controlled exclusively by t_{AA}.
12. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
13. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
14. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If t_{WCS} • t_{WCS} (MIN), the cycle is an EARLY WRITE cycle and the data output will remain open circuit throughout the entire cycle. If t_{RWD} • t_{RWD} (MIN), t_{AWD} • t_{AWD} (MIN) and t_{CWD} • t_{CWD} (MIN), the cycle is a READ-WRITE cycle and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until $\overline{CAS}$ and $\overline{RAS}$ or $\overline{OE}$ go back to V_{IH}) is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW result in a LATE WRITE ($\overline{OE}$-controlled) cycle.
15. Output parameter (I/O) is referenced to corresponding $\overline{CAS}$ input, I/O0-I/O7 by $\overline{LCAS}$ and I/O8-I/O15 by $\overline{UCAS}$.
16. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, I/O goes open. If $\overline{OE}$ is tied permanently LOW, a LATE WRITE or READ-MODIFY-WRITE is not possible.
17. Write command is defined as $\overline{WE}$ going low.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The I/Os will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back to LOW after t_{OEH} is met.
19. The I/Os are in open during READ cycles once t_{OD} or t_{OFF} occur.
20. The first $\chi\overline{CAS}$ edge to transition LOW.
21. The last $\chi\overline{CAS}$ edge to transition HIGH.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY WRITE cycles and $\overline{WE}$ leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
23. Last falling $\chi\overline{CAS}$ edge to first rising $\chi\overline{CAS}$ edge.
24. Last rising $\chi\overline{CAS}$ edge to next cycle's last rising $\chi\overline{CAS}$ edge.
25. Last rising $\chi\overline{CAS}$ edge to first falling $\chi\overline{CAS}$ edge.
26. Each $\chi\overline{CAS}$ must meet minimum pulse width.
27. Last $\chi\overline{CAS}$ to go LOW.
28. I/Os controlled, regardless $\overline{UCAS}$ and $\overline{LCAS}$.
29. The 3 ns minimum is a parameter guaranteed by design.
30. Enables on-chip refresh and address counters.

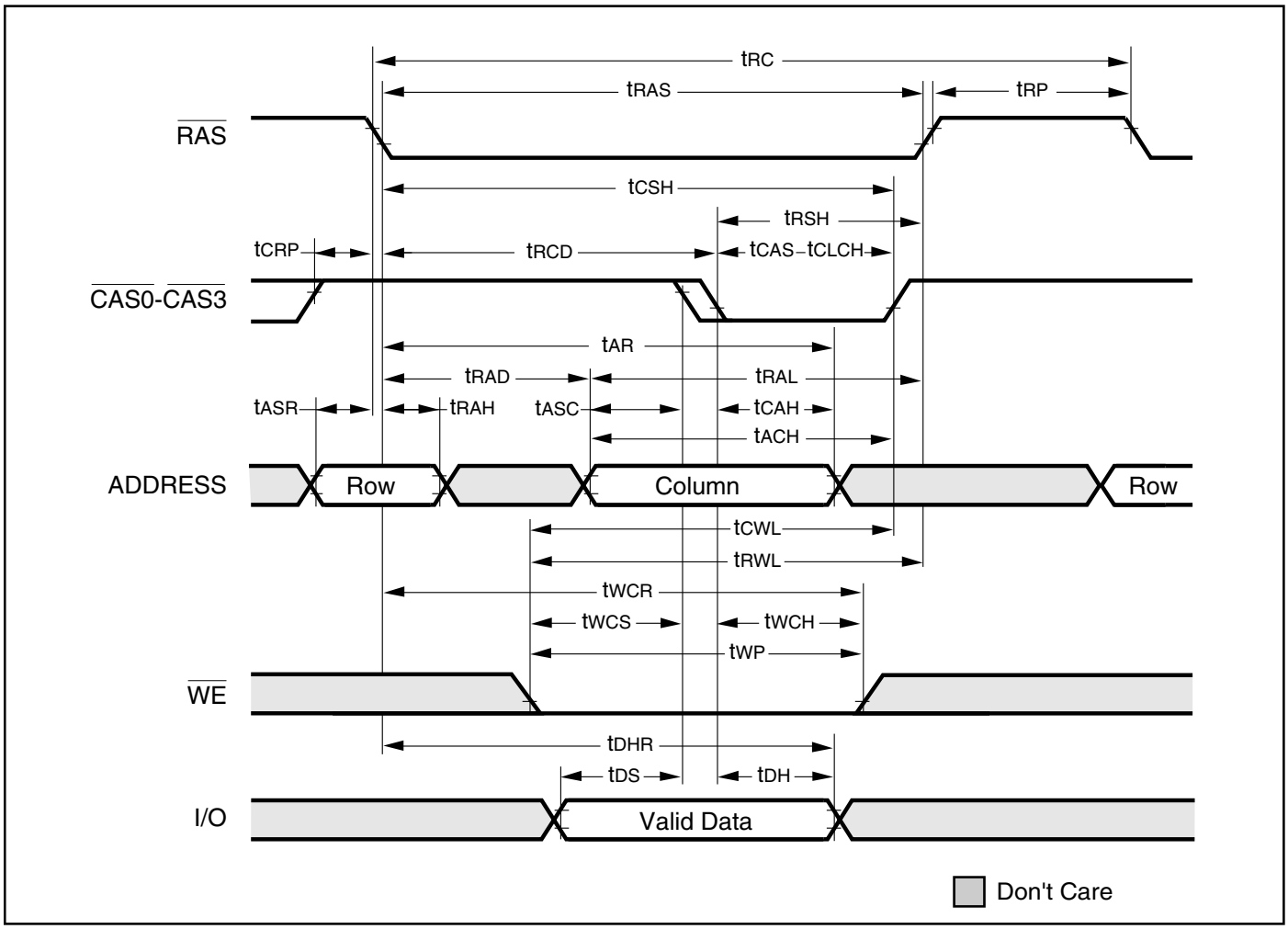
READ CYCLE (Outputs Controlled by $\overline{RAS}$)



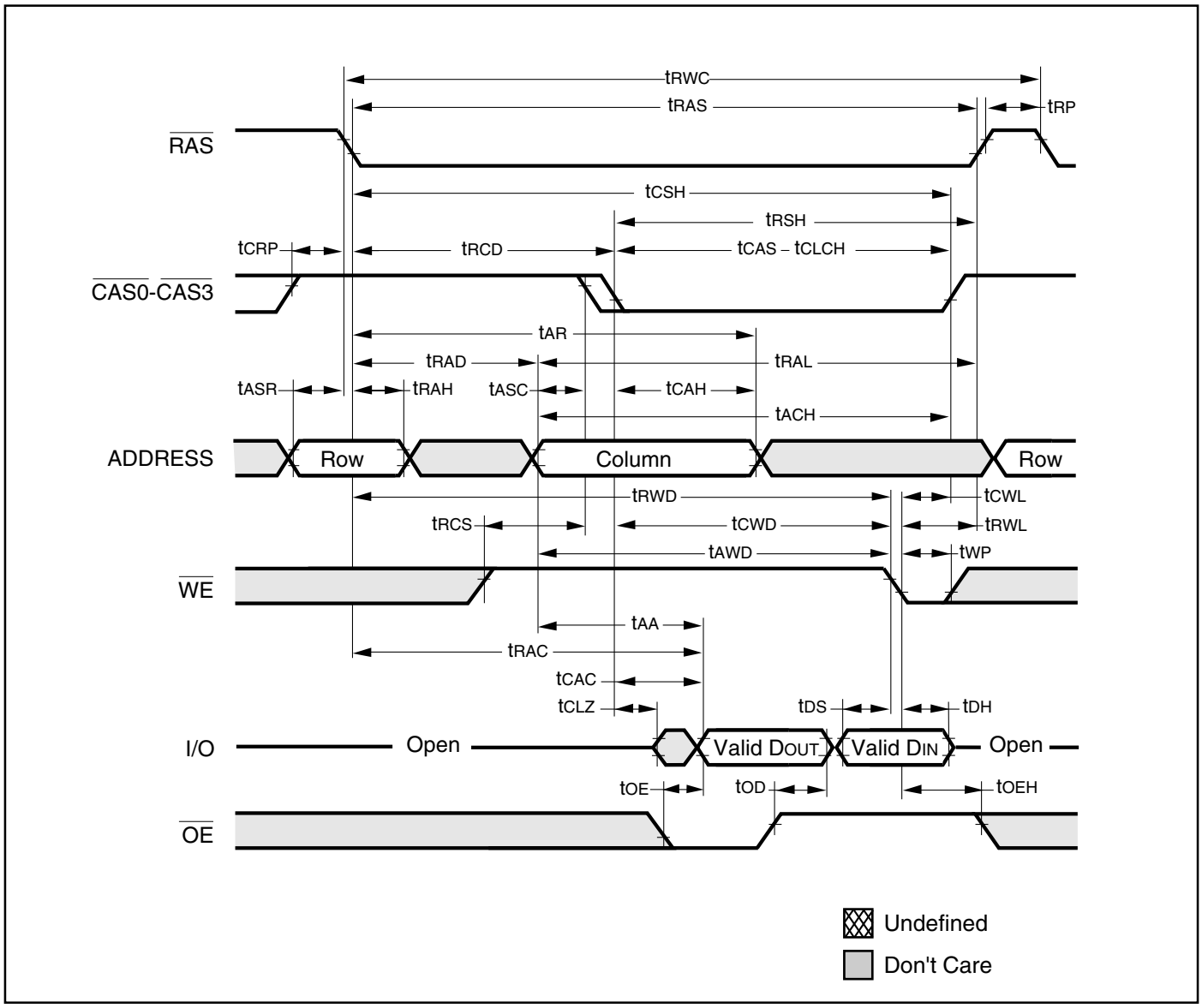
READ CYCLE (Outputs Controlled by $\overline{CAS}$)



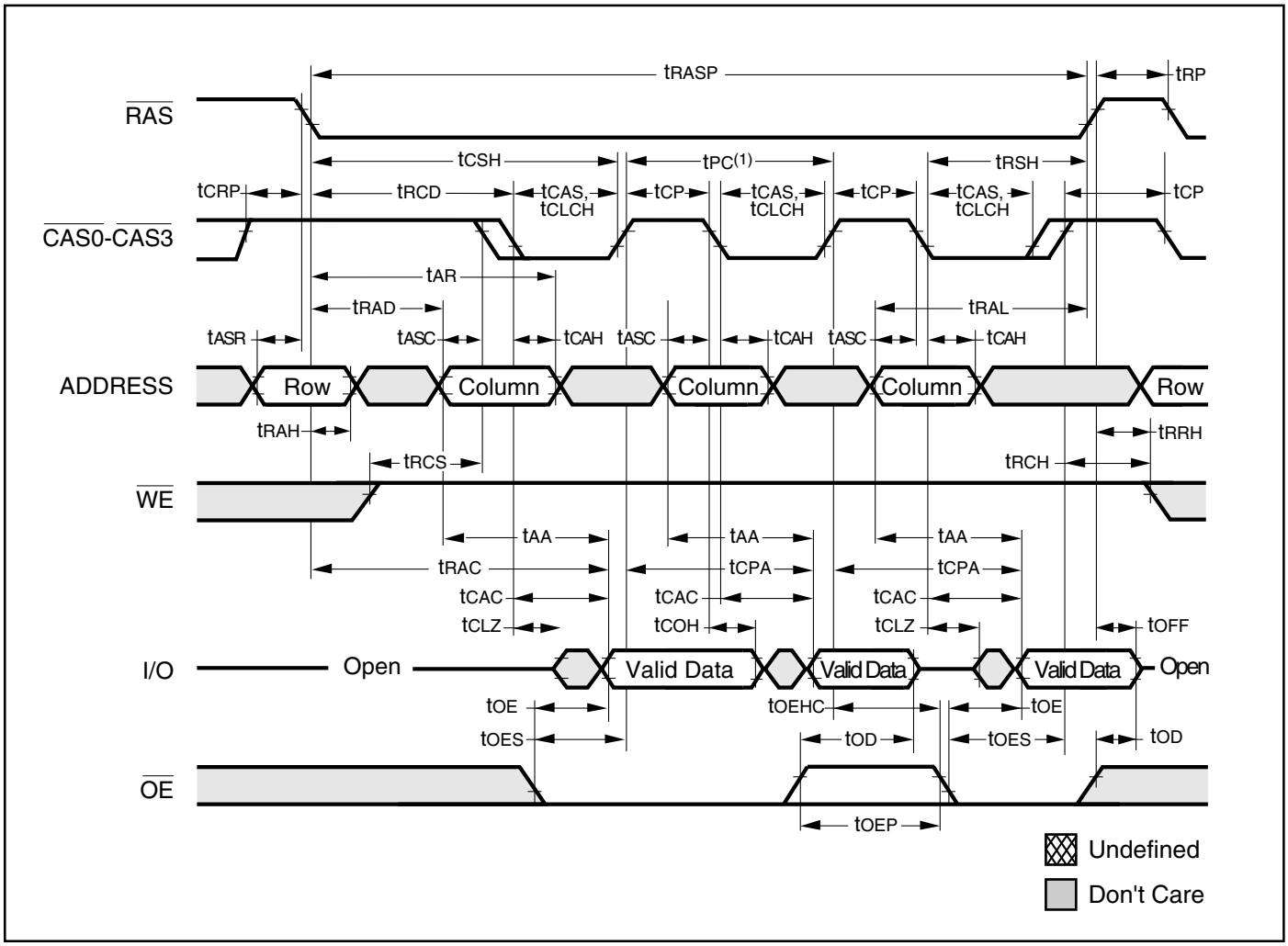
EARLY WRITE CYCLE ($\overline{OE}$ = DON'T CARE)



READ WRITE CYCLE (LATE WRITE and READ-MODIFY-WRITE Cycles)

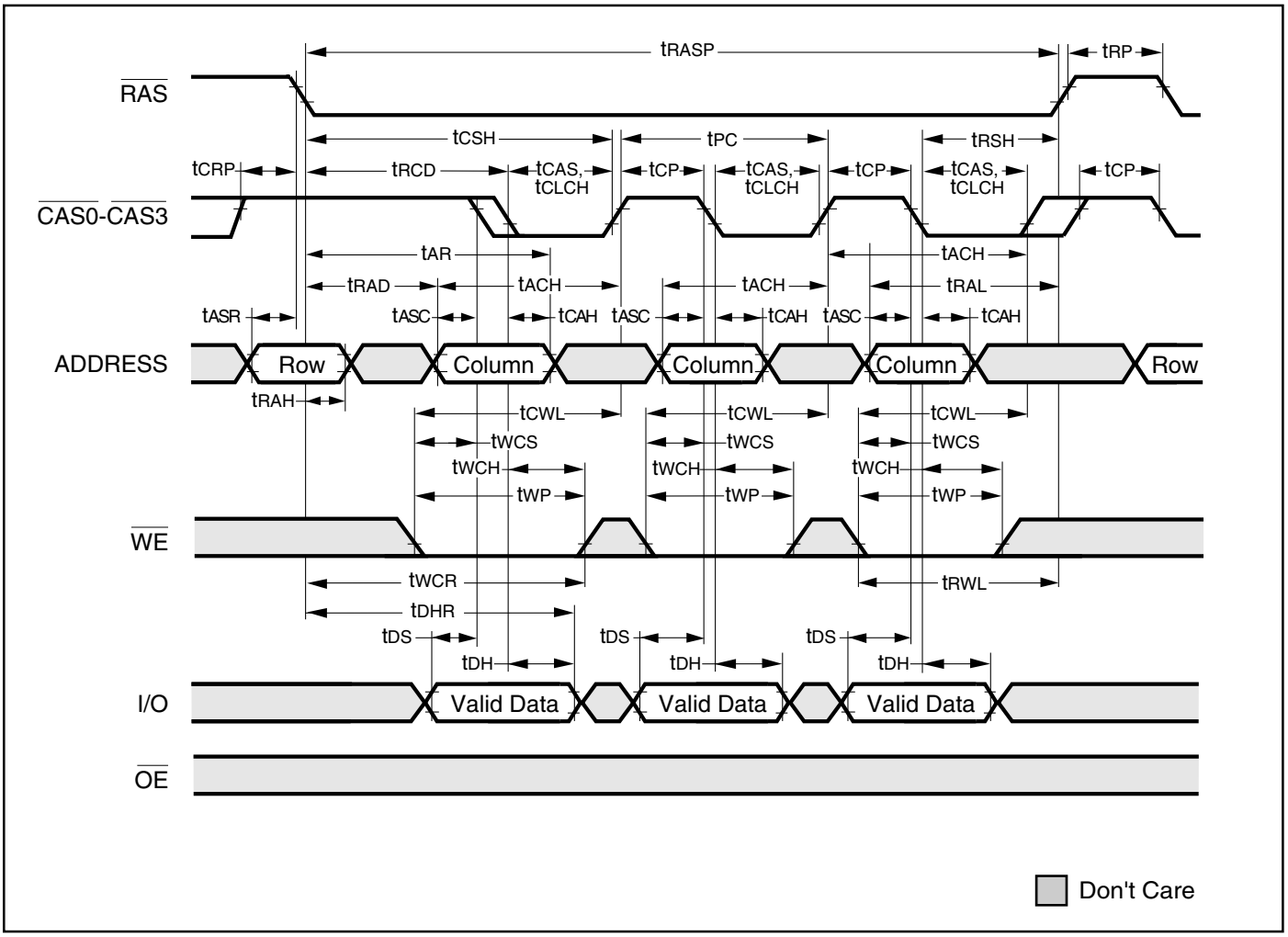


EDO-PAGE-MODE READ CYCLE

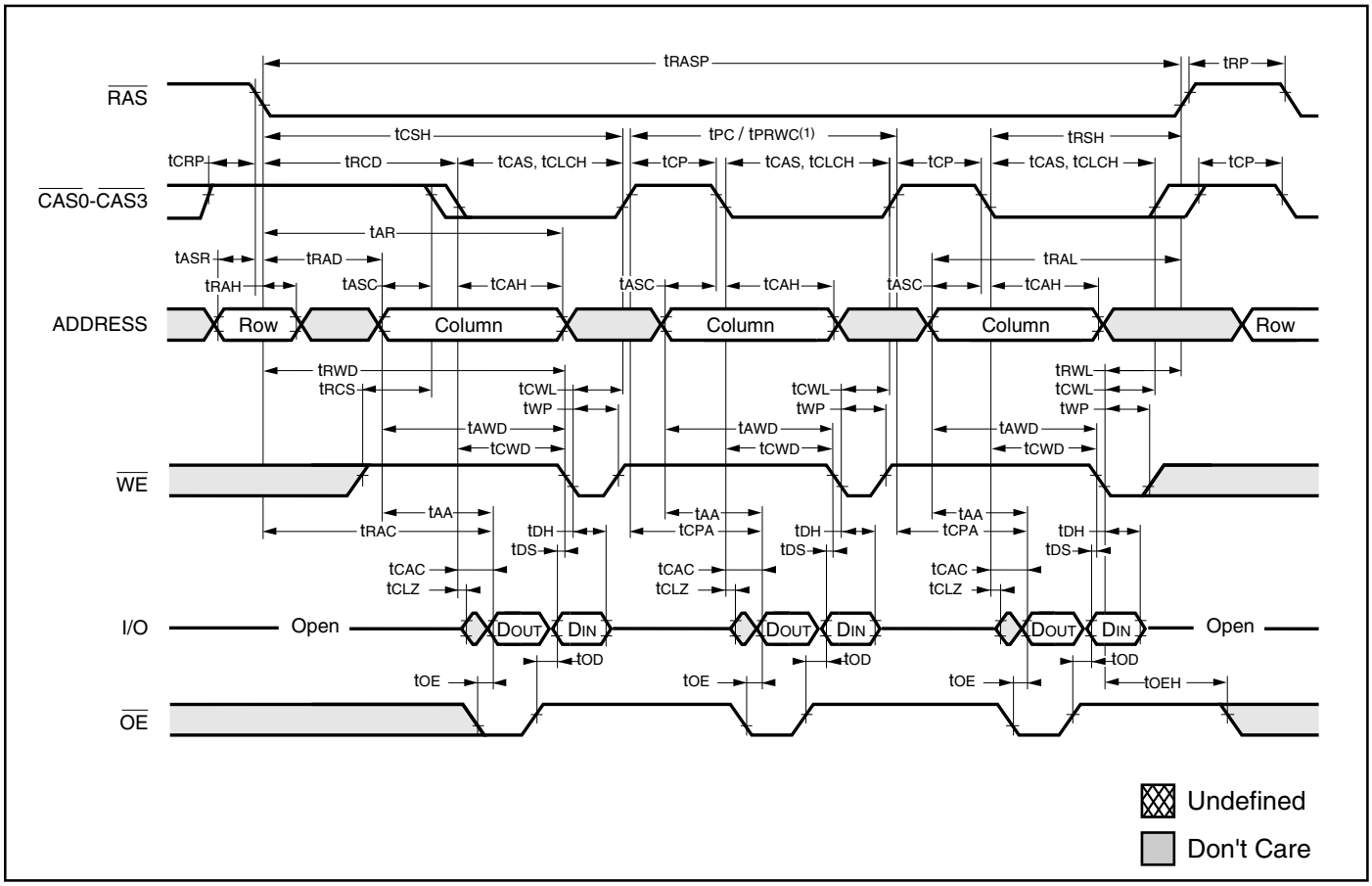


Note:
1. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specifications.

EDO-PAGE-MODE EARLY-WRITE CYCLE



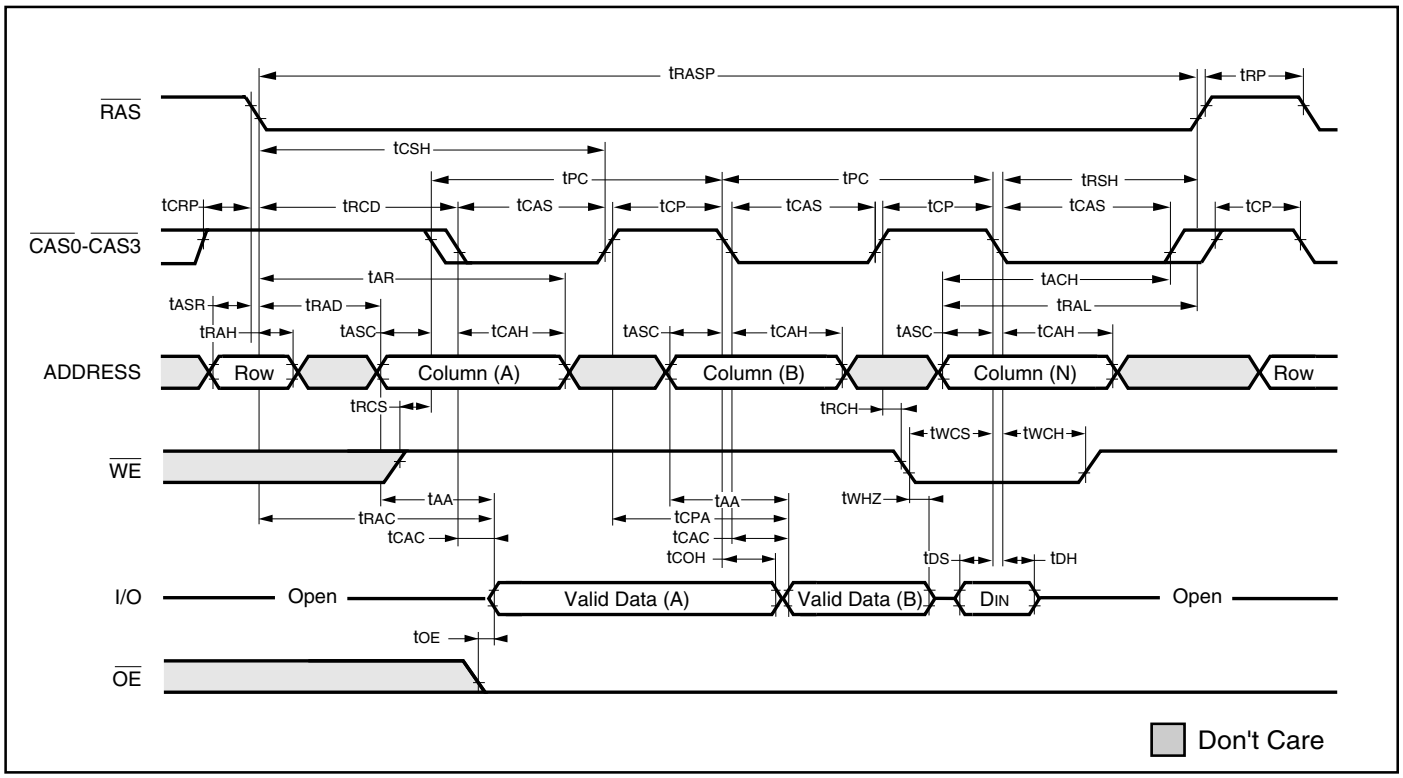
EDO-PAGE-MODE READ-WRITE CYCLE (LATE WRITE and READ-MODIFY WRITE Cycles)



Note:

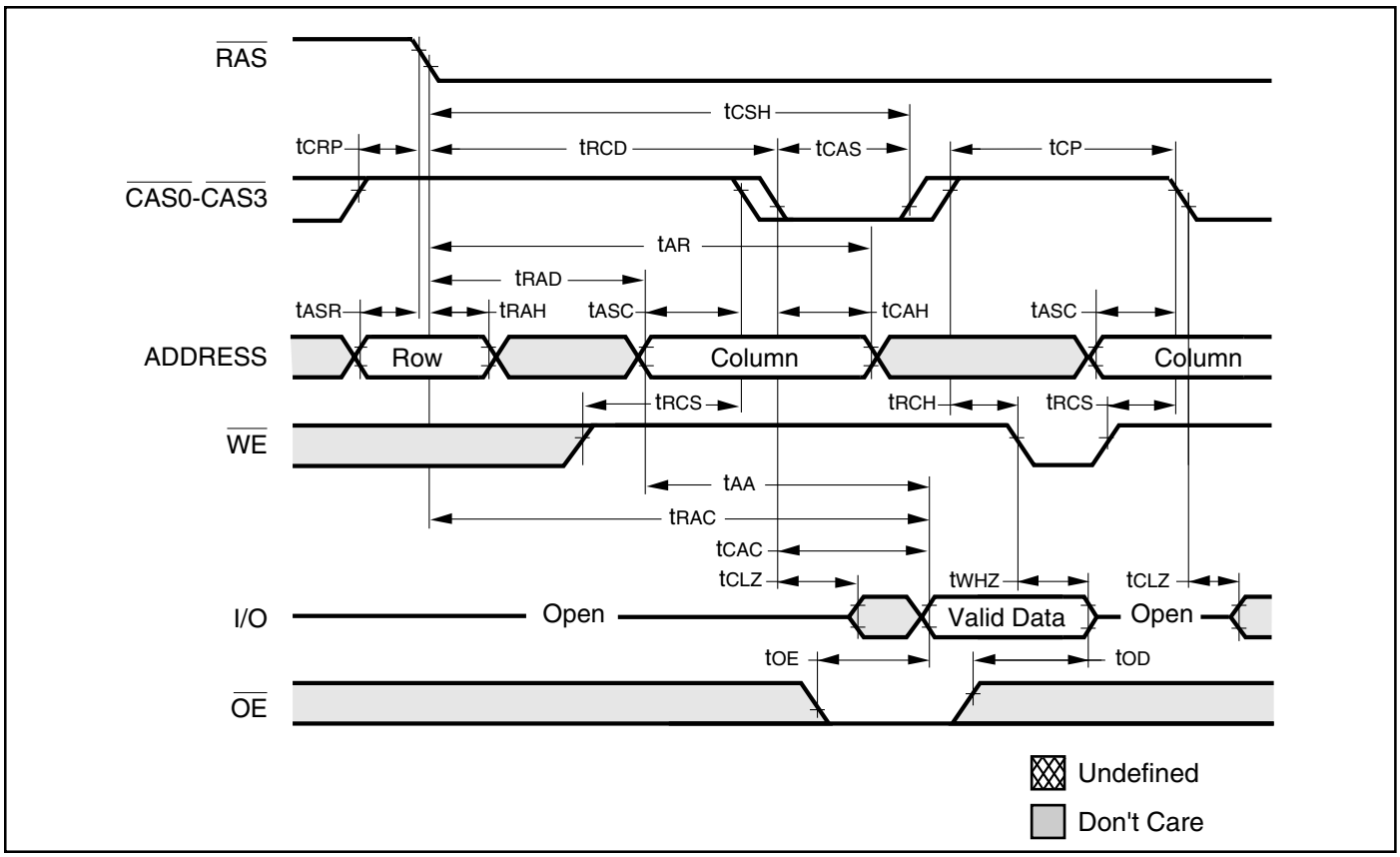
1. t_{PC} can be measured from falling edge of $\overline{CAS}$ to falling edge of $\overline{CAS}$, or from rising edge of $\overline{CAS}$ to rising edge of $\overline{CAS}$. Both measurements must meet the t_{PC} specifications.

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE (Psuedo READ-MODIFY WRITE)

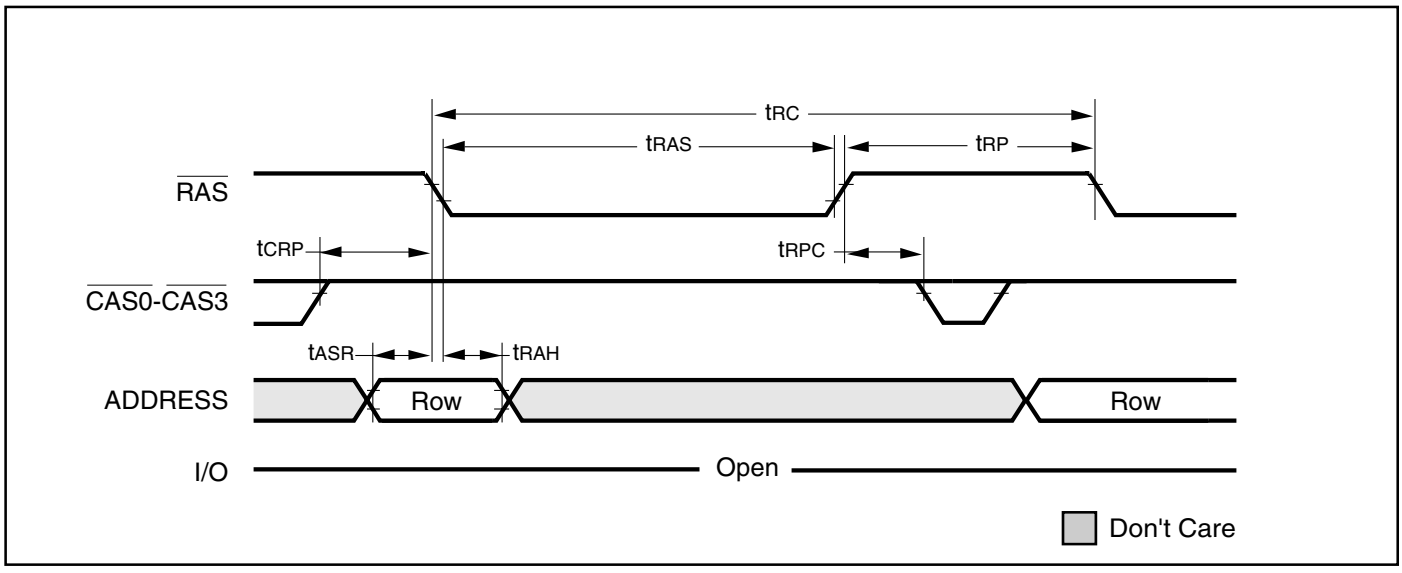


AC WAVEFORMS

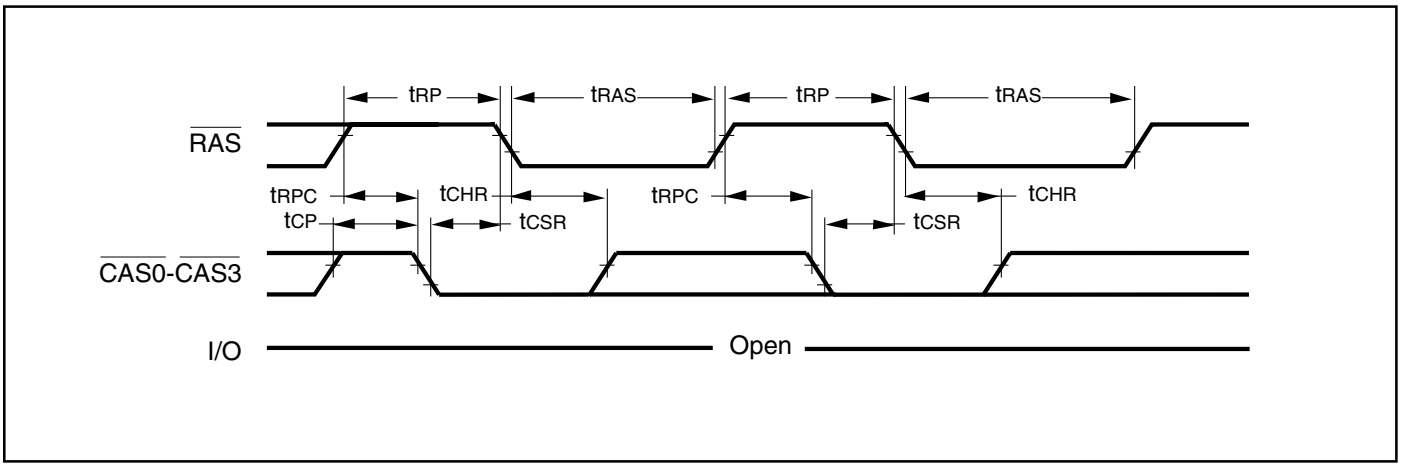
READ CYCLE (With $\overline{WE}$-Controlled Disable)



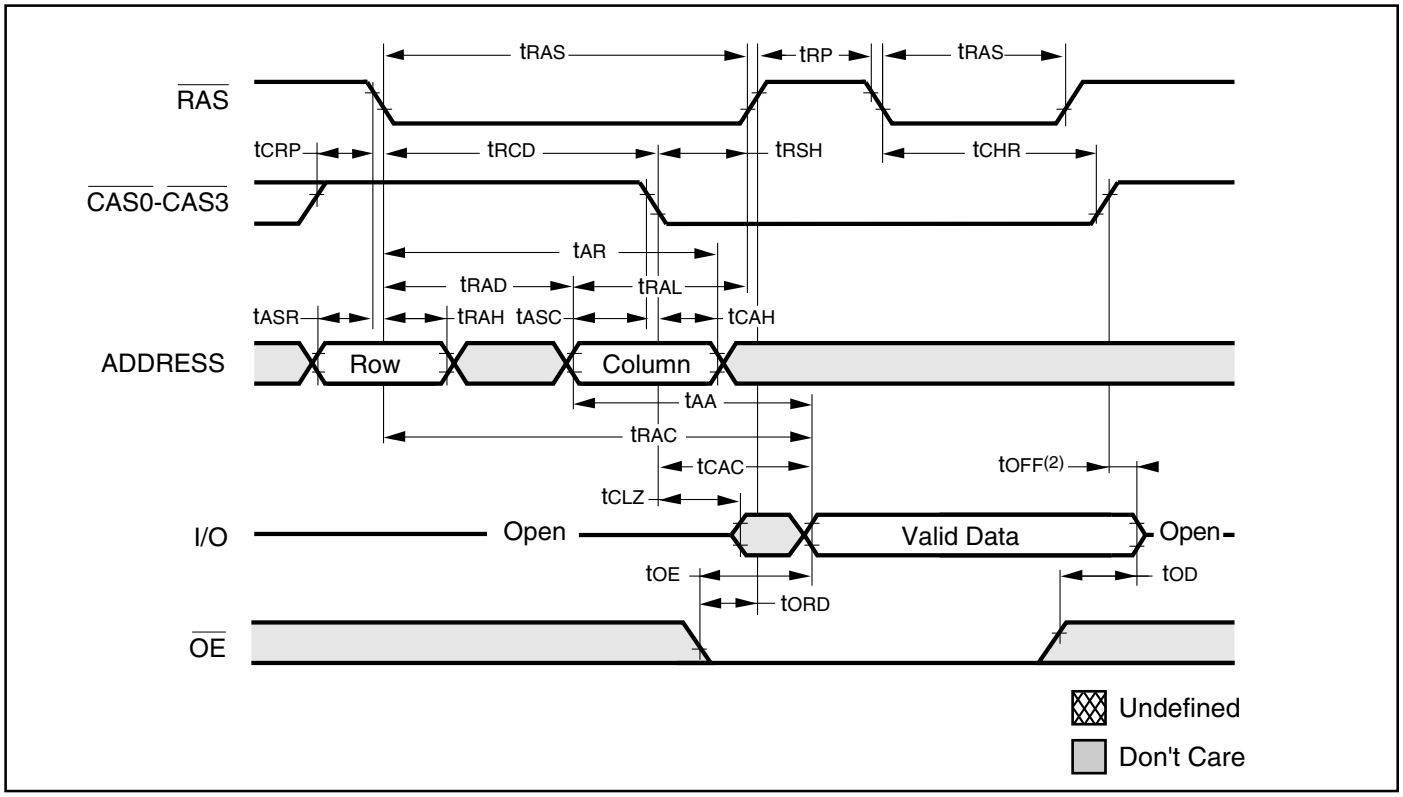
$\overline{RAS}$-ONLY REFRESH CYCLE ($\overline{OE}$, $\overline{WE}$ = DON'T CARE)



$\overline{\text{CBR}}$ REFRESH CYCLE (Addresses; $\overline{\text{WE}}$, $\overline{\text{OE}}$ = DON'T CARE)



HIDDEN REFRESH CYCLE ($\overline{\text{WE}}$ = HIGH; $\overline{\text{OE}}$ = LOW)(1)



Notes:
1. A Hidden Refresh may also be performed after a Write Cycle. In this case, $\overline{\text{WE}}$ = LOW and $\overline{\text{OE}}$ = HIGH.
2. tOFF is referenced from rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$, whichever occurs last.

ORDERING INFORMATION

Commercial Range: 0·C to 70·C

Speed (ns)	Order Part No.	Package
28	IS41LV32256-28PQ	PQFP
	IS41LV32256-28TQ	TQFP
30	IS41LV32256-30PQ	PQFP
	IS41LV32256-30TQ	TQFP
35	IS41LV32256-35PQ	PQFP
	IS41LV32256-35TQ	TQFP

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