



IS61LV12816

128K x 16 HIGH-SPEED CMOS STATIC RAM WITH 3.3V SUPPLY

FEATURES

- High-speed access time: 8, 10, 12, and 15 ns
- CMOS low power operation
- TTL and CMOS compatible interface levels
- Single 3.3V \pm 10% power supply
- Fully static operation: no clock or refresh required
- Three state outputs
- Data control for upper and lower bytes
- Industrial temperature available

DESCRIPTION

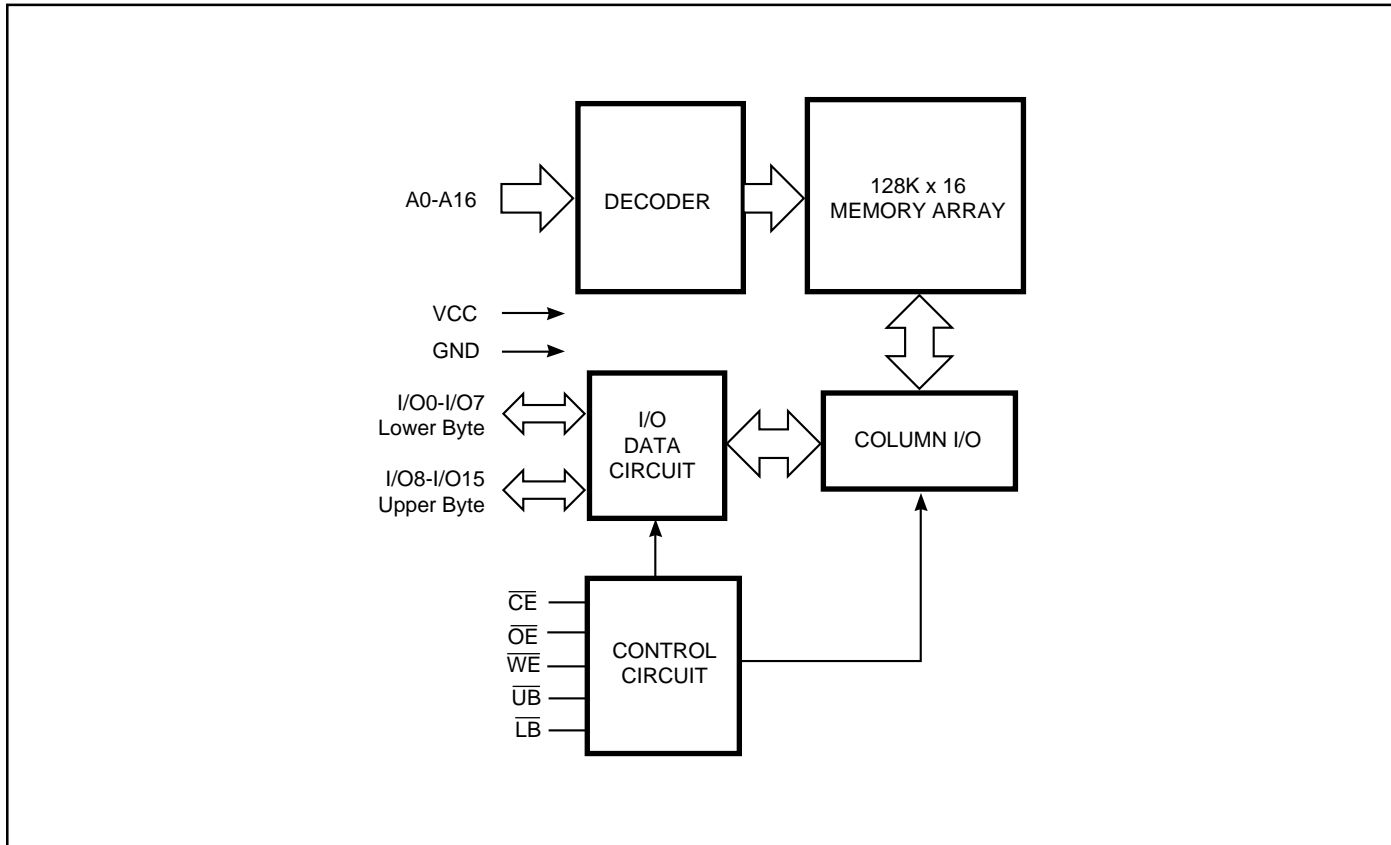
The *ICSI* IS61LV12816 is a high-speed, 2,097,152-bit static RAM organized as 131,072 words by 16 bits. It is fabricated using *ICSI*'s high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields access times as fast as 8 ns with low power consumption.

When \overline{CE} is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down with CMOS input levels.

Easy memory expansion is provided by using Chip Enable and Output Enable inputs, \overline{CE} and \overline{OE} . The active LOW Write Enable (\overline{WE}) controls both writing and reading of the memory. A data byte allows Upper Byte (\overline{UB}) and Lower Byte (\overline{LB}) access.

The IS61LV12816 is packaged in the JEDEC standard 44-pin 400mil SOJ, 44-pin 400mil TSOP-2, and 48-pin 6*8mm TF-BGA.

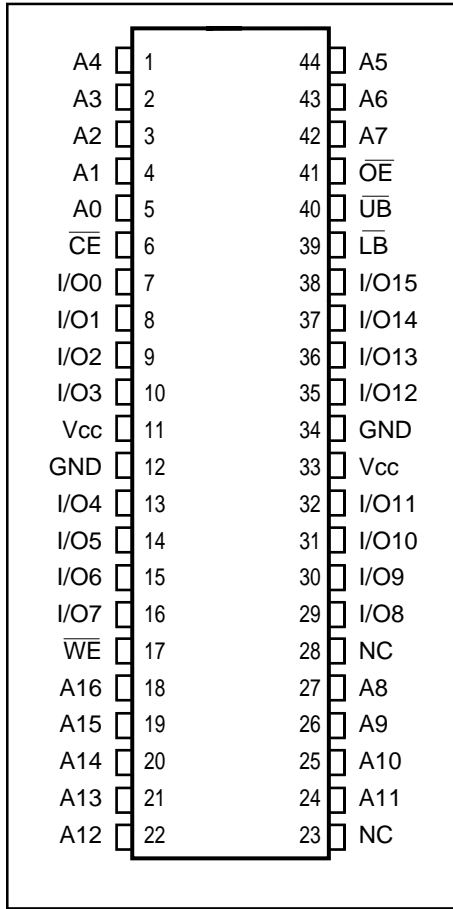
FUNCTIONAL BLOCK DIAGRAM



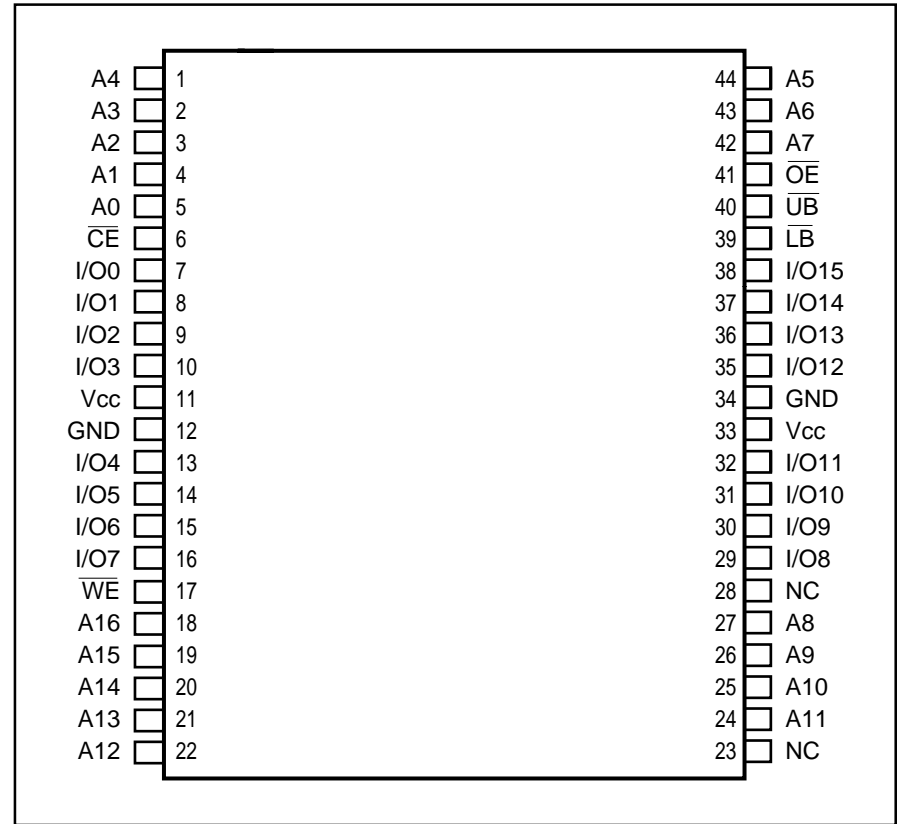
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PIN CONFIGURATIONS

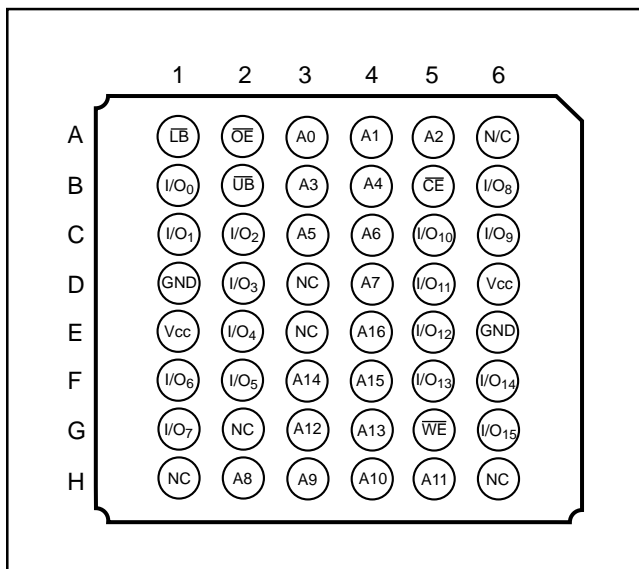
44-Pin SOJ



44-Pin TSOP-2



48-Pin TF-BGA



PIN DESCRIPTIONS

| | |
|-----------------|---------------------------------|
| A0-A16 | Address Inputs |
| I/O0-I/O15 | Data Inputs/Outputs |
| \overline{CE} | Chip Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{WE} | Write Enable Input |
| \overline{LB} | Lower-byte Control (I/O0-I/O7) |
| \overline{UB} | Upper-byte Control (I/O8-I/O15) |
| NC | No Connection |
| Vcc | Power |
| GND | Ground |

OPERATING RANGE

| Range | Ambient Temperature | Vcc |
|------------|---------------------|------------|
| Commercial | 0°C to +70°C | 3.3V ± 10% |
| Industrial | -40°C to +85°C | 3.3V ± 10% |

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit | |
|-------------------|--------------------------------------|------------------------------|------------|----|
| V _{CC} | Power Supply Voltage Relative to GND | -0.5 to 4.0 | V | |
| V _{TERM} | Terminal Voltage with Respect to GND | -0.5 to V _{CC} +0.5 | V | |
| T _{STG} | Storage Temperature | -65 to +150 | °C | |
| T _{BIAS} | Temperature Under Bias: | Com. | -65 to +85 | °C |
| | | Ind. | -45 to +90 | °C |
| P _T | Power Dissipation | 2.0 | W | |
| I _{OUT} | DC Output Current (LOW) | ±20 | mA | |

Note:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | Min. | Max. | Unit | |
|-----------------|----------------------------------|--|------|-----------------------|------|----|
| V _{OH} | Output HIGH Voltage | V _{CC} = Min., I _{OH} = -4.0 mA | 2.4 | — | V | |
| V _{OL} | Output LOW Voltage | V _{CC} = Min., I _{OL} = 8.0 mA | — | 0.4 | V | |
| V _{IH} | Input HIGH Voltage | | 2 | V _{CC} + 0.3 | V | |
| V _{IL} | Input LOW Voltage ⁽¹⁾ | | -0.3 | 0.8 | V | |
| I _{LI} | Input Leakage | GND ≤ V _{IN} ≤ V _{CC} | Com. | -1 | 1 | μA |
| | | | Ind. | -5 | 5 | μA |
| I _{LO} | Output Leakage | GND ≤ V _{OUT} ≤ V _{CC} , Outputs Disabled | Com. | -1 | 1 | μA |
| | | | Ind. | -5 | 5 | μA |

Notes:

1. V_{IL} (min.) = -2.0V for pulse width less than 10 ns.
2. The V_{CC} operating range for 8 ns is 3.3V +10%, -5%.

TRUTH TABLE

| Mode | \overline{WE} | \overline{CE} | \overline{OE} | \overline{LB} | \overline{UB} | I/O PIN | | Vcc Current |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|------------------|-------------------------------------|
| | | | | | | I/O0-I/O7 | I/O8-I/O15 | |
| Not Selected | X | H | X | X | X | High-Z | High-Z | I _{SB1} , I _{SB2} |
| Output Disabled | H | L | H | X | X | High-Z | High-Z | I _{CC} |
| | X | L | X | H | H | High-Z | High-Z | |
| Read | H | L | L | L | H | D _{OUT} | High-Z | I _{CC} |
| | H | L | L | H | L | High-Z | D _{OUT} | |
| | H | L | L | L | L | D _{OUT} | D _{OUT} | |
| Write | L | L | X | L | H | D _{IN} | High-Z | I _{CC} |
| | L | L | X | H | L | High-Z | D _{IN} | |
| | L | L | X | L | L | D _{IN} | D _{IN} | |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | -8 ns | | -10 ns | | -12 ns | | -15 ns | | Unit | |
|------------------|--------------------------------------|---|-------|------|--------|------|--------|------|--------|------|------|----|
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | | |
| I _{CC} | Vcc Dynamic Operating Supply Current | V _{CC} = Max., $\overline{CE} = V_{IL}$ | Com. | — | 220 | — | 200 | — | 180 | — | 165 | mA |
| | | I _{OUT} = 0 mA, f = f _{MAX} | Ind. | — | 230 | — | 210 | — | 190 | — | 175 | |
| I _{SB1} | TTL Standby Current (TTL Inputs) | V _{CC} = Max., | Com. | — | 30 | — | 30 | — | 30 | — | 30 | mA |
| | | V _{IN} = V _{IH} or V _{IL} $\overline{CE} \geq V_{IH}$, f = 0 | Ind. | — | 40 | — | 40 | — | 40 | — | 40 | |
| I _{SB2} | CMOS Standby Current (CMOS Inputs) | V _{CC} = Max., | Com. | — | 10 | — | 10 | — | 10 | — | 10 | mA |
| | | $\overline{CE} \geq V_{CC} - 0.2V$, V _{IN} ≥ V _{CC} - 0.2V, or V _{IN} ≤ 0.2V, f = 0 | Ind. | — | 15 | — | 15 | — | 15 | — | 15 | |

Note:

1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE⁽¹⁾

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Note:

1. Tested initially and after any design or process changes that may affect these parameters.

READ CYCLE SWITCHING CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | -8 | | -10 | | -12 | | -15 | | Unit |
|----------------------------------|--|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{RC} | Read Cycle Time | 8 | — | 10 | — | 12 | — | 15 | — | ns |
| t _{AA} | Address Access Time | — | 8 | — | 10 | — | 12 | — | 15 | ns |
| t _{oHA} | Output Hold Time | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t _{ACE} | \overline{CE} Access Time | 8 | — | — | 10 | — | 12 | — | 15 | ns |
| t _{DOE} | \overline{OE} Access Time | — | 3 | — | 4 | — | 5 | — | 6 | ns |
| t _{HZOE} ⁽²⁾ | \overline{OE} to High-Z Output | — | 3 | — | 4 | — | 5 | 0 | 6 | ns |
| t _{LZOE} ⁽²⁾ | \overline{OE} to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{HZCE} ⁽²⁾ | \overline{CE} to High-Z Output | 0 | 3 | 0 | 4 | 0 | 5 | 0 | 8 | ns |
| t _{LZCE} ⁽²⁾ | \overline{CE} to Low-Z Output | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t _{BA} | \overline{LB} , \overline{UB} Access Time | — | 3 | — | 4 | — | 5 | — | 6 | ns |
| t _{HZB} ⁽²⁾ | \overline{LB} , \overline{UB} to High-Z Output | 0 | 3 | 0 | 4 | 0 | 5 | 0 | 6 | ns |
| t _{LZB} ⁽²⁾ | \overline{LB} , \overline{UB} to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 3 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

Notes:

1. The V_{cc} operating range for 8 ns is 3.3V +10%, -5%.

AC TEST LOADS

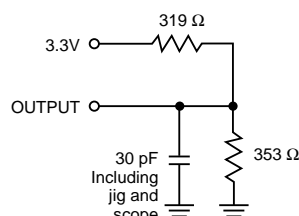


Figure 1.

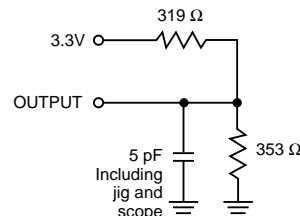
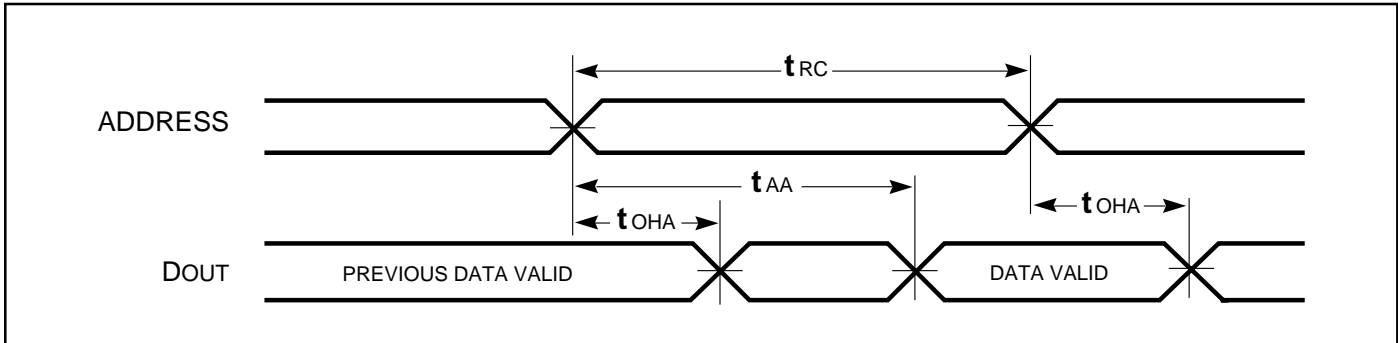


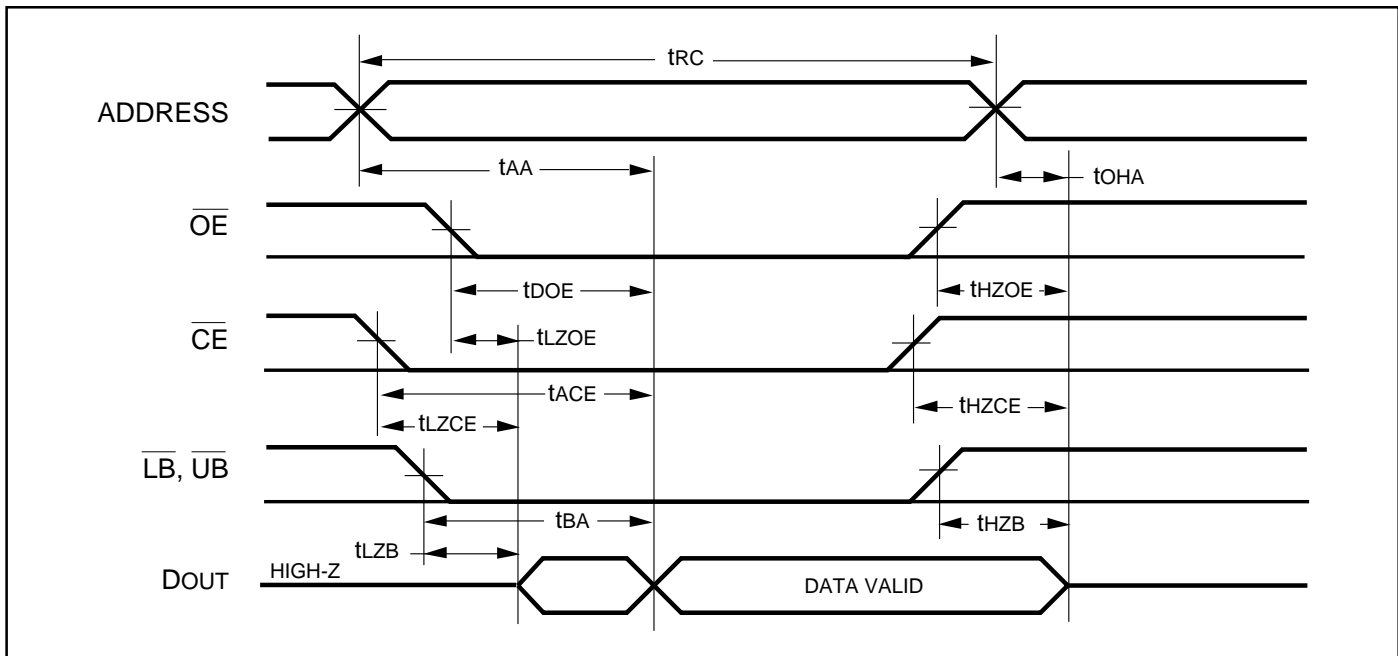
Figure 2.

AC WAVEFORMS

READ CYCLE NO. 1^(1,2) (Address Controlled) ($\overline{CE} = \overline{OE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$)



READ CYCLE NO. 2^(1,3)



Notes:

1. \overline{WE} is HIGH for a Read Cycle.
2. The device is continuously selected. \overline{OE} , \overline{CE} , \overline{UB} , or $\overline{LB} = V_{IL}$.
3. Address is valid prior to or coincident with \overline{CE} LOW transition.

WRITE CYCLE SWITCHING CHARACTERISTICS^(1,3) (Over Operating Range)

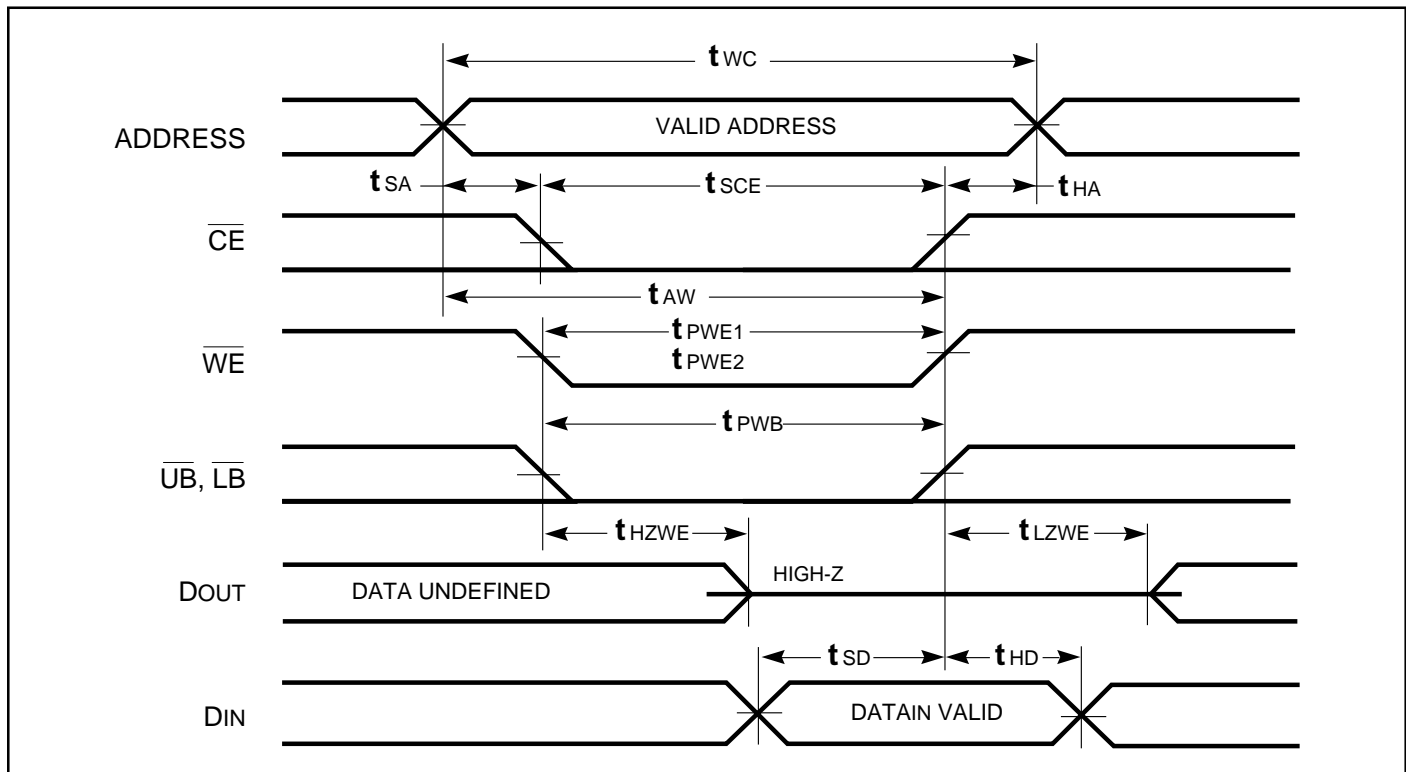
| Symbol | Parameter | -8 | | -10 | | -12 | | -15 | | Unit |
|---------------------------------|---|------|------|------|------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| t _{WC} | Write Cycle Time | 8 | — | 10 | — | 12 | — | 15 | — | ns |
| t _{SCE} | \overline{CE} to Write End | 7 | — | 8 | — | 8 | — | 10 | — | ns |
| t _{AW} | Address Setup Time to Write End | 7 | — | 8 | — | 8 | — | 10 | — | ns |
| t _{HA} | Address Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{SA} | Address Setup Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PWB} | \overline{LB} , \overline{UB} Valid to End of Write | 7 | — | 8 | — | 9 | — | 10 | — | ns |
| t _{PWE⁽⁴⁾} | \overline{WE} Pulse Width | 7 | — | 8 | — | 9 | — | 10 | — | ns |
| t _{SD} | Data Setup to Write End | 4.5 | — | 5 | — | 6 | — | 7 | — | ns |
| t _{HD} | Data Hold from Write End | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{HZWE⁽²⁾} | \overline{WE} LOW to High-Z Output | — | 3 | — | 4 | — | 5 | — | 6 | ns |
| t _{LZWE⁽²⁾} | \overline{WE} HIGH to Low-Z Output | 0 | — | 0 | — | 0 | — | 0 | — | ns |

Notes:

1. Test conditions assume signal transition times of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ± 500 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of \overline{CE} LOW and \overline{UB} or \overline{LB} , and \overline{WE} LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the write.
4. Tested with \overline{OE} Hith.

AC WAVEFORMS

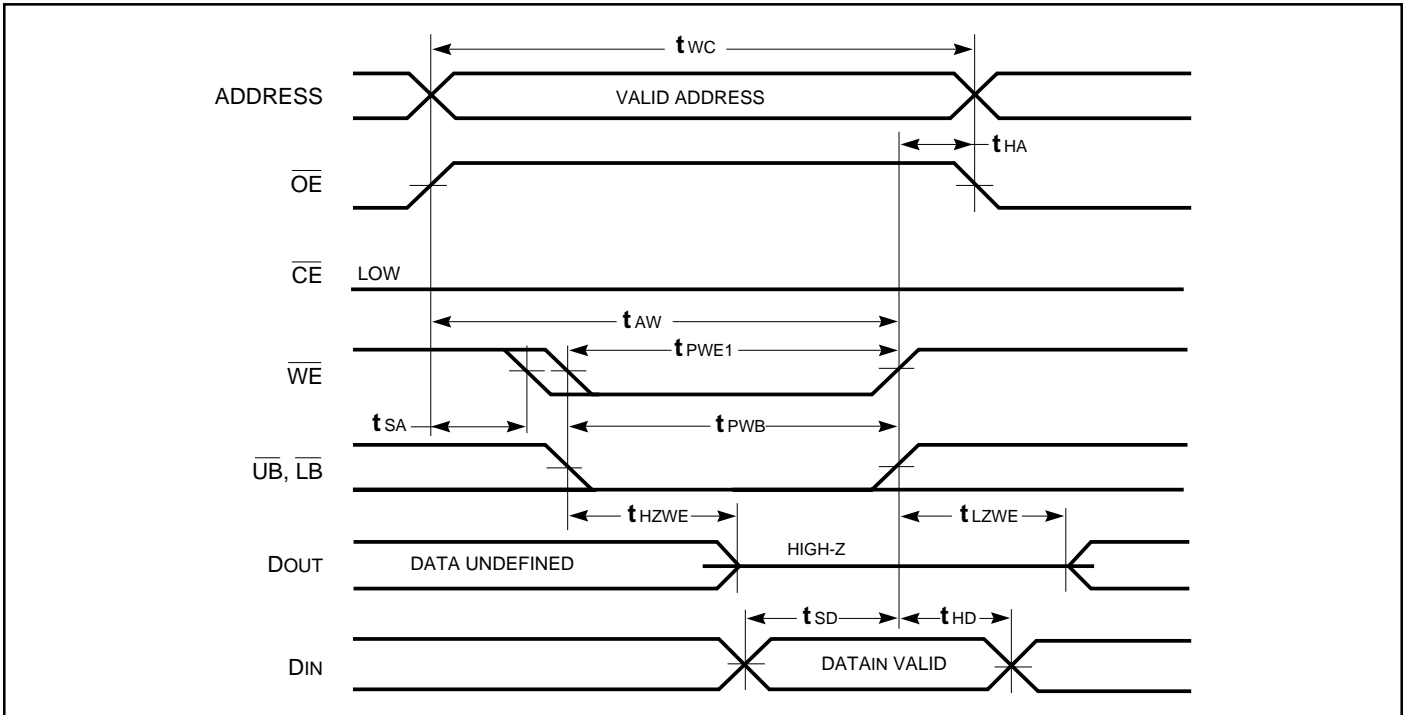
WRITE CYCLE NO. 1 ^(1,2)(\overline{CE} Controlled, \overline{OE} is HIGH or LOW)



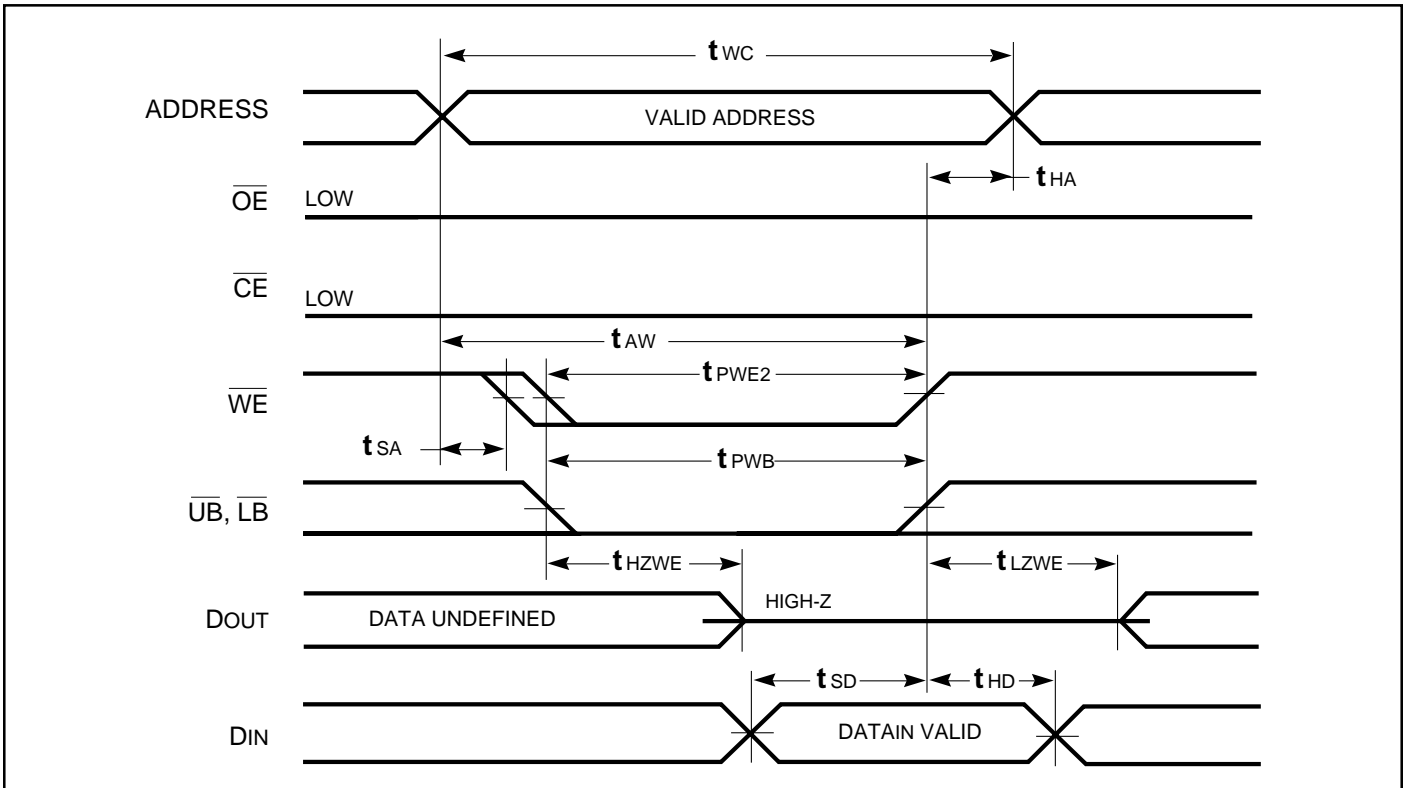
Notes:

1. WRITE is an internally generated signal asserted during an overlap of the LOW states on the \overline{CE} and \overline{WE} inputs and at least one of the \overline{LB} and \overline{UB} inputs being in the LOW state.
2. WRITE = (\overline{CE}) [(\overline{LB}) = (\overline{UB})] (\overline{WE}).

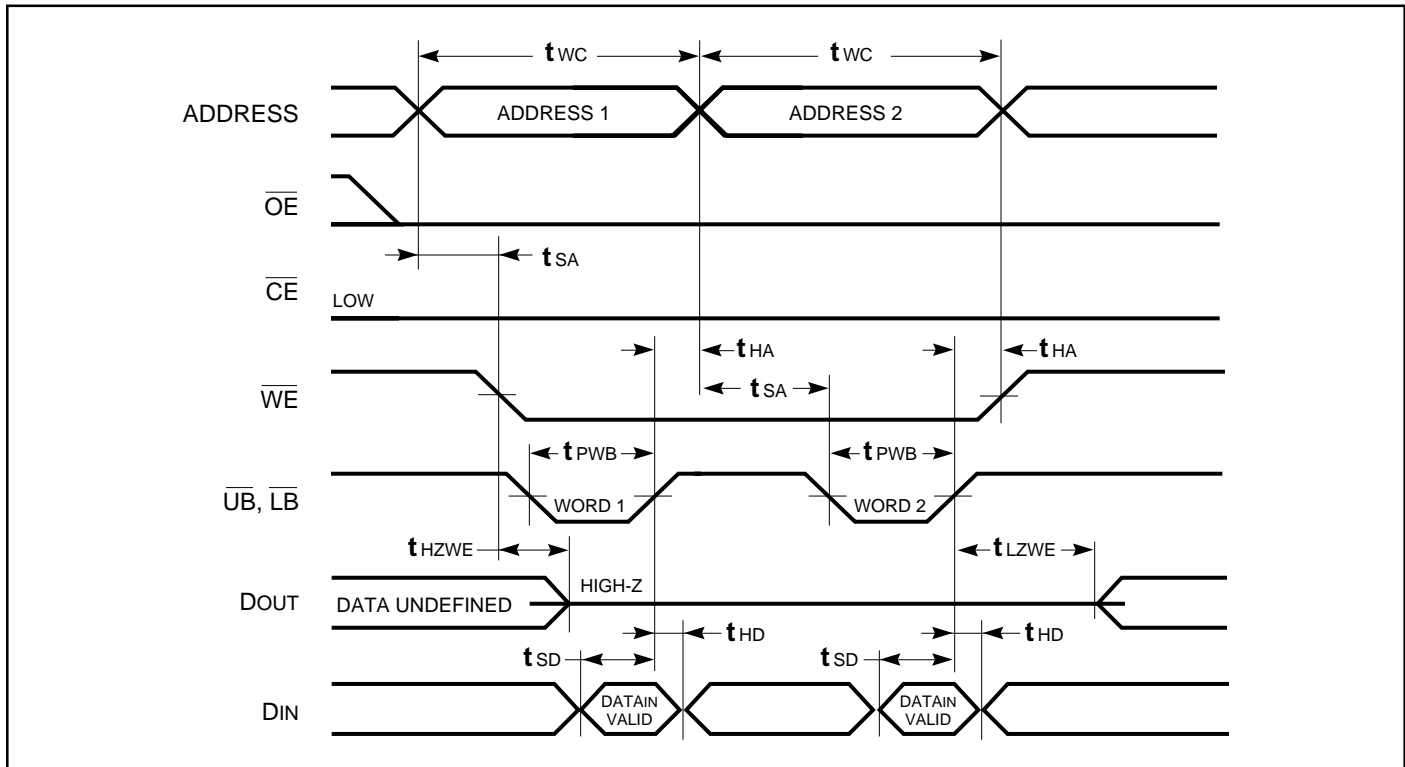
WRITE CYCLE NO. 2⁽¹⁾ (\overline{WE} Controlled. \overline{OE} is HIGH During Write Cycle)



WRITE CYCLE NO. 3 (\overline{WE} Controlled. \overline{OE} is LOW During Write Cycle)



WRITE CYCLE NO. 4 ^(1,3)($\overline{\text{LB}}$, $\overline{\text{UB}}$ Controlled, Back-to-Back Write)



Notes:

1. The internal Write time is defined by the overlap of $\overline{\text{CE}} = \text{LOW}$, $\overline{\text{UB}}$ and/or $\overline{\text{LB}} = \text{LOW}$, and $\overline{\text{WE}} = \text{LOW}$. All signals must be in valid states to initiate a Write, but any can be deasserted to terminate the Write. The t_{SA} , t_{HA} , t_{SD} , and t_{HD} timing is referenced to the rising or falling edge of the signal that terminates the Write.
2. Tested with $\overline{\text{OE}}$ HIGH for a minimum of 4 ns before $\overline{\text{WE}} = \text{LOW}$ to place the I/O in a HIGH-Z state.
3. $\overline{\text{WE}}$ may be held LOW across many address cycles and the $\overline{\text{LB}}$, $\overline{\text{UB}}$ pins can be used to control the Write function.

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

| Speed (ns) | Order Part No. | Package |
|------------|-----------------|---------------|
| 8 | IS61LV12816-8B | 6*8mm TF-BGA |
| 8 | IS61LV12816-8K | 400mil SOJ |
| 8 | IS61LV12816-8T | 400mil TSOP-2 |
| 10 | IS61LV12816-10B | 6*8mm TF-BGA |
| 10 | IS61LV12816-10K | 400mil SOJ |
| 10 | IS61LV12816-10T | 400mil TSOP-2 |
| 12 | IS61LV12816-12B | 6*8mm TF-BGA |
| 12 | IS61LV12816-12K | 400mil SOJ |
| 12 | IS61LV12816-12T | 400mil TSOP-2 |
| 15 | IS61LV12816-15B | 6*8mm TF-BGA |
| 15 | IS61LV12816-15K | 400mil SOJ |
| 15 | IS61LV12816-15T | 400mil TSOP-2 |

ORDERING INFORMATION

Industrial Range: -40°C to +85°C

| Speed (ns) | Order Part No. | Package |
|------------|------------------|---------------|
| 8 | IS61LV12816-8BI | 6*8mm TF-BGA |
| 8 | IS61LV12816-8KI | 400mil SOJ |
| 8 | IS61LV12816-8TI | 400mil TSOP-2 |
| 10 | IS61LV12816-10BI | 6*8mm TF-BGA |
| 10 | IS61LV12816-10KI | 400mil SOJ |
| 10 | IS61LV12816-10TI | 400mil TSOP-2 |
| 12 | IS61LV12816-12BI | 6*8mm TF-BGA |
| 12 | IS61LV12816-12KI | 400mil SOJ |
| 12 | IS61LV12816-12TI | 400mil TSOP-2 |
| 15 | IS61LV12816-15BI | 6*8mm TF-BGA |
| 15 | IS61LV12816-15KI | 400mil SOJ |
| 15 | IS61LV12816-15TI | 400mil TSOP-2 |



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