IS61NVVP25672
IS61NVVP51236

ISSI®

256K x 72 and 512K x 36, 18Mb PIPELINE 'NO WAIT' STATE BUS SRAM

ADVANCE INFORMATION
JULY 2002

FEATURES

- 100 percent bus utilization
- No wait cycles between Read and Write
- Internal self-timed write cycle
- Individual Byte Write Control
- Single R/W (Read/Write) control pin
- Clock controlled, registered address, data and control
- Interleaved or linear burst sequence control using MODE input
- Power Down mode
- Common data inputs and data outputs
- $\overline{CKE}$ pin to enable clock and suspend operation
- JEDEC 119-ball PBGA (x36) and 209-ball (x72) PBGA packages
- Single +1.8V (± 5%) power supply
- JTAG Boundary Scan
- Industrial temperature available

DESCRIPTION

The 16 Meg 'NVVP' product family feature high-speed, low-power synchronous static RAMs designed to provide a burstable, high-performance, 'no wait' state, device for network and communications customers. They are organized as 256K words by 72 bits, 512K words by 36 bits and are fabricated with *ISSI*'s advanced CMOS technology.

Incorporating a 'no wait' state feature, wait cycles are eliminated when the bus switches from read to write, or write to read. This device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit.

All synchronous inputs pass through registers are controlled by a positive-edge-triggered single clock input. Operations may be suspended and all synchronous inputs ignored when Clock Enable, $\overline{CKE}$ is HIGH. In this state the internal device will hold their previous values.

All Read, Write and Deselect cycles are initiated by the ADV input. When the ADV is HIGH the internal burst counter is incremented. New external addresses can be loaded when ADV is LOW.

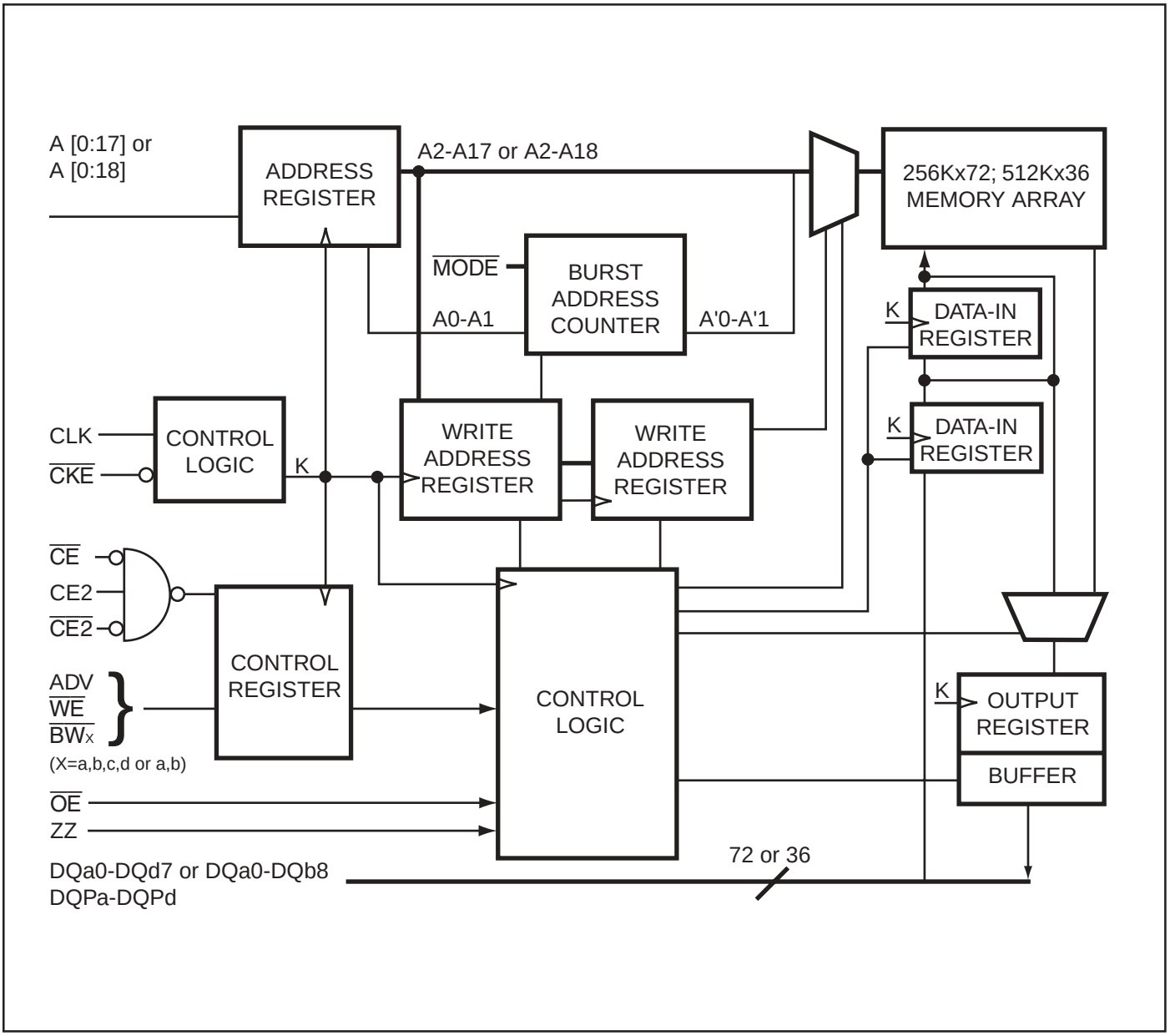
Write cycles are internally self-timed and are initiated by the rising edge of the clock inputs and when $\overline{WE}$ is LOW. Separate byte enables allow individual bytes to be written.

A burst mode pin (MODE) defines the order of the burst sequence. When tied HIGH, the interleaved burst sequence is selected. When tied LOW, the linear burst sequence is selected.

FAST ACCESS TIME

Symbol	Parameter	-250	-200	Units
t_{KQ}	Clock Access Time	2.6	3.2	ns
t_{KC}	Cycle Time	4	5	ns
	Frequency	250	200	MHz

BLOCK DIAGRAM



PIN CONFIGURATION — 256K X 72, 209-Ball PBGA (TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	DQg	DQg	A	CE2	A	ADV	A	$\overline{CE2}$	A	DQb	DQb
B	DQg	DQg	$\overline{BW}$c	$\overline{BW}$g	NC	$\overline{WE}$	A	$\overline{BW}$b	$\overline{BW}$f	DQb	DQb
C	DQg	DQg	$\overline{BW}$h	$\overline{BW}$d	NC	$\overline{CE}$	NC	$\overline{BW}$e	$\overline{BW}$a	DQb	DQb
D	DQg	DQg	GND	NC	NC	$\overline{OE}$	NC	NC	GND	DQb	DQb
E	DQPg	DQPc	V_{CCQ}	V_{CCQ}	V_{CC}	V_{CC}	V_{CC}	V_{CCQ}	V_{CCQ}	DQPf	DQPb
F	DQc	DQc	GND	GND	GND	NC	GND	GND	GND	DQf	DQf
G	DQc	DQc	V_{CCQ}	V_{CCQ}	V_{CC}	NC	V_{CC}	V_{CCQ}	V_{CCQ}	DQf	DQf
H	DQc	DQc	GND	GND	GND	NC	GND	GND	GND	DQf	DQf
J	DQc	DQc	V_{CCQ}	V_{CCQ}	V_{CC}	NC	V_{CC}	V_{CCQ}	V_{CCQ}	DQf	DQf
K	NC	NC	CLK	NC	GND	$\overline{CKE}$	GND	NC	NC	NC	NC
L	DQh	DQh	V_{CCQ}	V_{CCQ}	VCC	NC	V_{CC}	V_{CCQ}	V_{CCQ}	DQa	DQa
M	DQh	DQh	GND	GND	GND	NC	GND	GND	GND	DQa	DQa
N	DQh	DQh	V_{CCQ}	V_{CCQ}	VCC	NC	V_{CC}	V_{CCQ}	V_{CCQ}	DQa	DQa
P	DQh	DQh	GND	GND	GND	ZZ	GND	GND	GND	DQa	DQa
R	DQPd	DQPh	V_{CCQ}	V_{CCQ}	V_{CC}	V_{CC}	V_{CC}	V_{CCQ}	V_{CCQ}	DQPa	DQPe
T	DQd	DQd	GND	NC	NC	MODE	NC	NC	GND	DQe	DQe
U	DQd	DQd	NC	A	NC	A	NC	A	NC	DQe	DQe
V	DQd	DQd	A	A	A	A1	A	A	A	DQe	DQe
W	DQd	DQd	TMS	TDI	A	A0	A	TDO	TCK	DQe	DQe

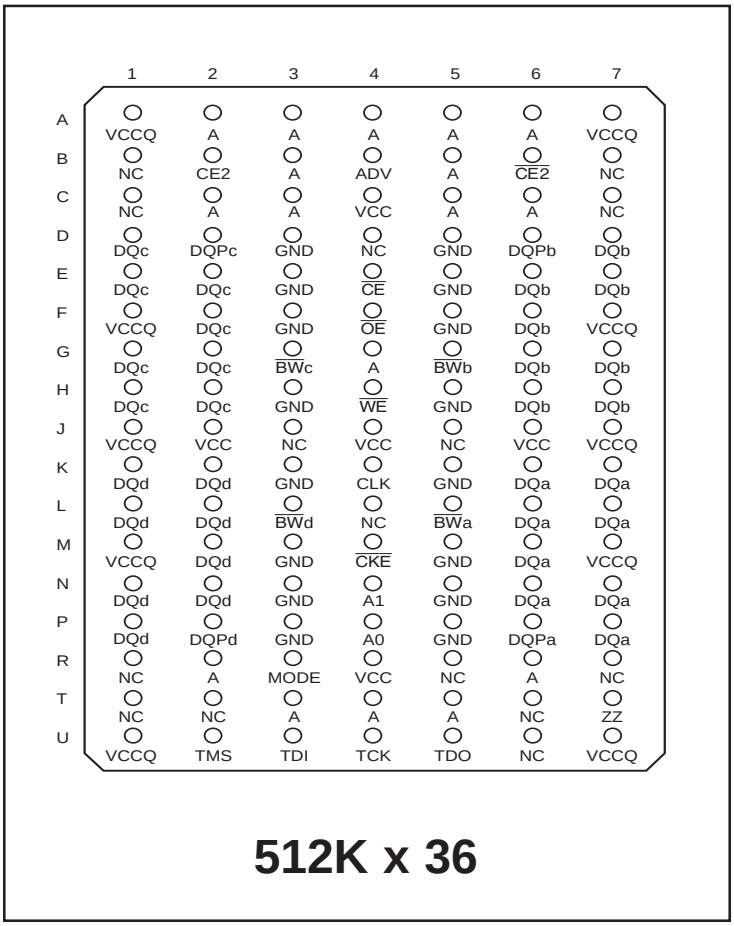
11 x 19 Ball BGA—14 x 22 mm^2 Body—1 mm Ball Pitch

PIN DESCRIPTIONS

A	Synchronous Address Inputs
A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
ADV	Synchronous Burst Address Advance
$\overline{BW}$a-$\overline{BW}$h	Synchronous Byte Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
DQa-DQh	Synchronous Data Input/Output
DQPa-DQPh	Parity Data Input/Output

GND	Ground
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Output Enable
TCK, TDI TDO, TMS	JTAG Boundary Scan Pins
V_{CC}	+1.8V Power Supply
V_{CCQ}	Isolated Output Buffer Supply: 1.8V
$\overline{WE}$	Write Enable
ZZ	Snooze Enable

PIN CONFIGURATION
119-pin PBGA (Top View)



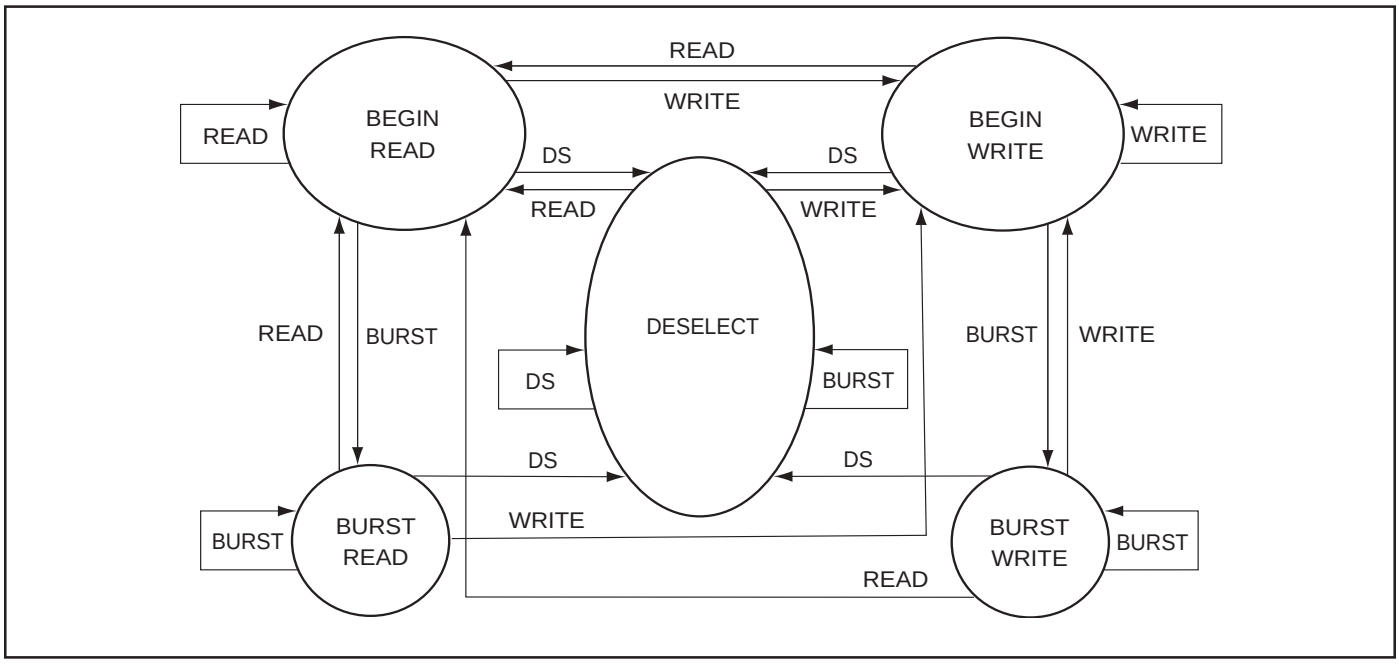
512K x 36

PIN DESCRIPTIONS

A	Synchronous Address Inputs
A0, A1	Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus.
ADV	Synchronous Burst Address Advance
$\overline{BW}$a-$\overline{BW}$h	Synchronous Byte Write Enable
$\overline{CE}$, $\overline{CE2}$, CE2	Synchronous Chip Enable
CLK	Synchronous Clock
$\overline{CKE}$	Clock Enable
DQa-DQd	Synchronous Data Input/Output
DQPa-DQPd	Parity Data Input/Output

GND	Ground
MODE	Burst Sequence Mode Selection
$\overline{OE}$	Output Enable
TCK, TDI TDO, TMS	JTAG Boundary Scan Pins
V_{CC}	1.8V Power Supply
V_{CCQ}	Isolated Output Buffer Supply: 1.8V
$\overline{WE}$	Write Enable
ZZ	Snooze Enable

STATE DIAGRAM



SYNCHRONOUS TRUTH TABLE(1)

Operation	Address Used	$\overline{CS}1$	CS2	$\overline{CS}2$	ADV	$\overline{WE}$	$\overline{BW}x$	$\overline{OE}$	$\overline{CKE}$	CLK
Not Selected Continue	N/A	X	X	X	H	X	X	X	L	↑
Not Selected	N/A	H	X	X	L	X	X	X	L	↑
Not Selected	N/A	X	L	X	L	X	X	X	L	↑
Not Selected	N/A	X	X	H	L	X	X	X	L	↑
Begin Burst Read	External Address	L	H	L	L	H	X	L	L	↑
Continue Burst Read	Next Address	X	X	X	H	X	X	L	L	↑
NOP/Dummy Read	External Address	L	H	L	L	H	X	H	L	↑
Dummy Read	Next Address	X	X	X	H	X	X	H	L	↑
Begin Burst Write	External Address	L	H	L	L	L	L	X	L	↑
Continue Burst Write	Next Address	X	X	X	H	X	L	X	L	↑
NOP/Write Abort	N/A	L	H	L	L	L	H	X	L	↑
Write Abort	Next Address	X	X	X	H	X	H	X	L	↑
Ignore Clock	Current Address	X	X	X	X	X	X	X	H	↑

Notes:
1. "X" means don't care.
2. The rising edge of clock is symbolized by ↑
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WE}$ = L means Write operation in Write Truth Table.
   $\overline{WE}$ = H means Read operation in Write Truth Table.
5. Operation finally depends on status of asynchronous pins (ZZ and $\overline{OE}$).

ASYNCHRONOUS TRUTH TABLE(1)

Operation	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L L	L H	DQ High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes:

1. X means "Don't Care".
2. For write cycles following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
3. Sleep Mode means power Sleep Mode where stand-by current does not depend on cycle time.
4. Deselected means power Sleep Mode where stand-by current depends on cycle time.

WRITE TRUTH TABLE (x36)

Operation	$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b	$\overline{BW}$c	$\overline{BW}$d
READ	H	X	X	X	X
WRITE BYTE a	L	L	H	H	H
WRITE BYTE b	L	H	L	H	H
WRITE BYTE c	L	H	H	L	H
WRITE BYTE d	L	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H

Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

WRITE TRUTH TABLE (x72)

Operation	$\overline{WE}$	$\overline{BW}$a	$\overline{BW}$b	$\overline{BW}$c	$\overline{BW}$d	$\overline{BW}$e	$\overline{BW}$f	$\overline{BW}$g	$\overline{BW}$h
READ	H	X	X	X	X	X	X	X	X
WRITE BYTE a	L	L	H	H	H	H	H	H	H
WRITE BYTE b	L	H	L	H	H	H	H	H	H
WRITE BYTE c	L	H	H	L	H	H	H	H	H
WRITE BYTE d	L	H	H	H	L	H	H	H	H
WRITE BYTE e	L	H	H	H	H	L	H	H	H
WRITE BYTE f	L	H	H	H	H	H	L	H	H
WRITE BYTE g	L	H	H	H	H	H	H	L	H
WRITE BYTE h	L	H	H	H	H	H	H	H	L
WRITE ALL BYTEs	L	L	L	L	L	L	L	L	L
WRITE ABORT/NOP	L	H	H	H	H	H	H	H	H

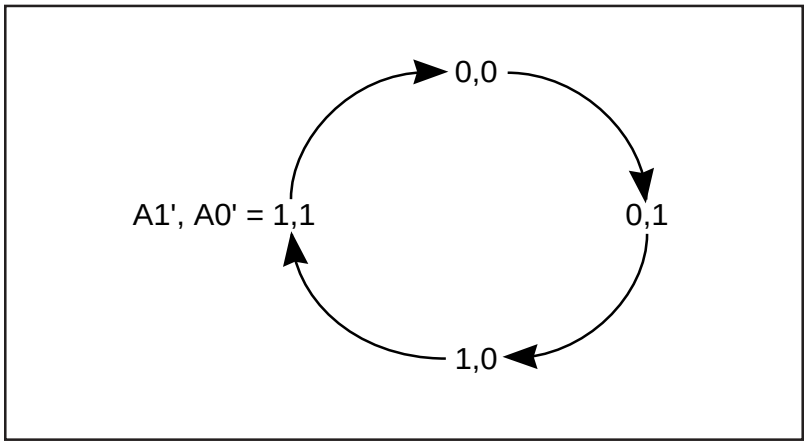
Notes:

1. X means "Don't Care".
2. All inputs in this table must beet setup and hold time around the rising edge of CLK.

INTERLEAVED BURST ADDRESS TABLE (MODE = Vcc)

External Address A1 A0	1st Burst Address A1 A0	2nd Burst Address A1 A0	3rd Burst Address A1 A0
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

LINEAR BURST ADDRESS TABLE (MODE = GND)



ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter		Value	Unit
T_{OPR}	Operating Temperature	Com Ind	–0 to +70 -40 to +85	°C
T_{STG}	Storage Temperature		–65 to +150	°C
P_D	Power Dissipation		1.6	W
I_{OUT}	Output Current (per I/O)		100	mA
V_{IN}, V_{OUT}	Voltage Relative to GND for I/O Pins		–0.5 to V_{CCQ} + 0.3	V
V_{IN}	Voltage Relative to GND for for Address and Control Inputs		–0.5 to V_{CCQ} + 0.3	V

Notes:
1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE

Range	Ambient Temperature	V_{CC}	V_{CCQ}
Commercial	0°C to +70°C	1.8V ± 5%	1.8V ± 5%
Industrial	-40°C to +85°C	1.8V ± 5%	1.8V ± 5%

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

			1.8V		
Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –4.0 mA	V_{CCQ} –0.4	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		1.1	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage		–0.3	0.6	V
I_{LI}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}[1]	–5	5	µA
I_{LO}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CCQ}, $\overline{OE}$ = V_I	–10	10	µA

POWER SUPPLY CHARACTERISTICS[1] (Over Operating Range)

Symbol	Parameter	Test Conditions		-250 MAX x36	-250 MAX x72	-200 MAX x36	-200 MAX x72	Unit
I_{CC}	AC Operating Supply Current	Device Selected, $\overline{OE}$ = V_{IH}, ZZ ≤ V_{IL}, All Inputs ≤ 0.2V or ≥ V_{CC} – 0.2V, Cycle Time ≥ t_{KC} min.	Com.	450	500	400	450	mA
			Ind.	500	550	450	500	
I_{SB}	Standby Current TTL Input	Device Deselected, V_{CC} = Max., All Inputs ≤ 0.2V or ≥ V_{CC} – 0.2V, ZZ ≤ V_{IL}, f = Max.	Com.	225	250	175	200	mA
			Ind.	—	—	200	230	
I_{SBI}	Standby Current CMOS Input	Device Deselected, V_{CC} = Max., V_{IN} ≤ GND + 0.2V or ≥ V_{CC} – 0.2V f = 0	Com.	150	150	150	150	mA
			Ind.	—	—	200	200	

Note:
1. MODE pin has an internal pullup and should be tied to Vcc or GND. It exhibits ±30 µA maximum leakage current when tied to ≤ GND + 0.2V or ≥ Vcc – 0.2V.

CAPACITANCE[1,2]

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	pF
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0V	8	pF

Notes:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, Vcc = 3.3V.

1.8V I/O AC TEST CONDITIONS

Parameter	Unit
Input Pulse Level	0.4V to 1.4V
Input Rise and Fall Times	2V/ ns
Input and Output Timing and Reference Level	0.9V
Output Load	See Figures 1 and 2

1.8V I/O OUTPUT LOAD EQUIVALENT

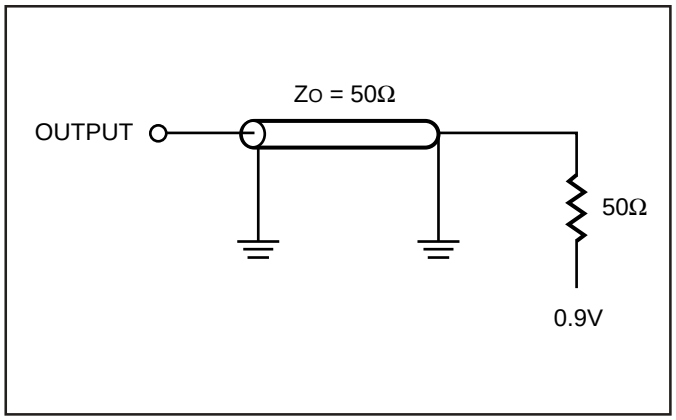


Figure 1

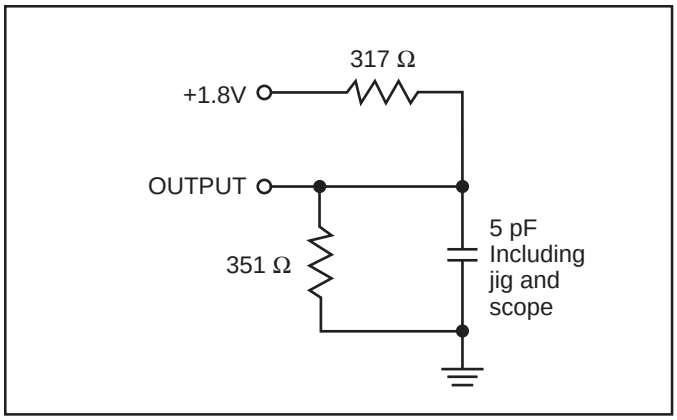


Figure 2

READ/WRITE CYCLE SWITCHING CHARACTERISTICS[1] (Over Operating Range)

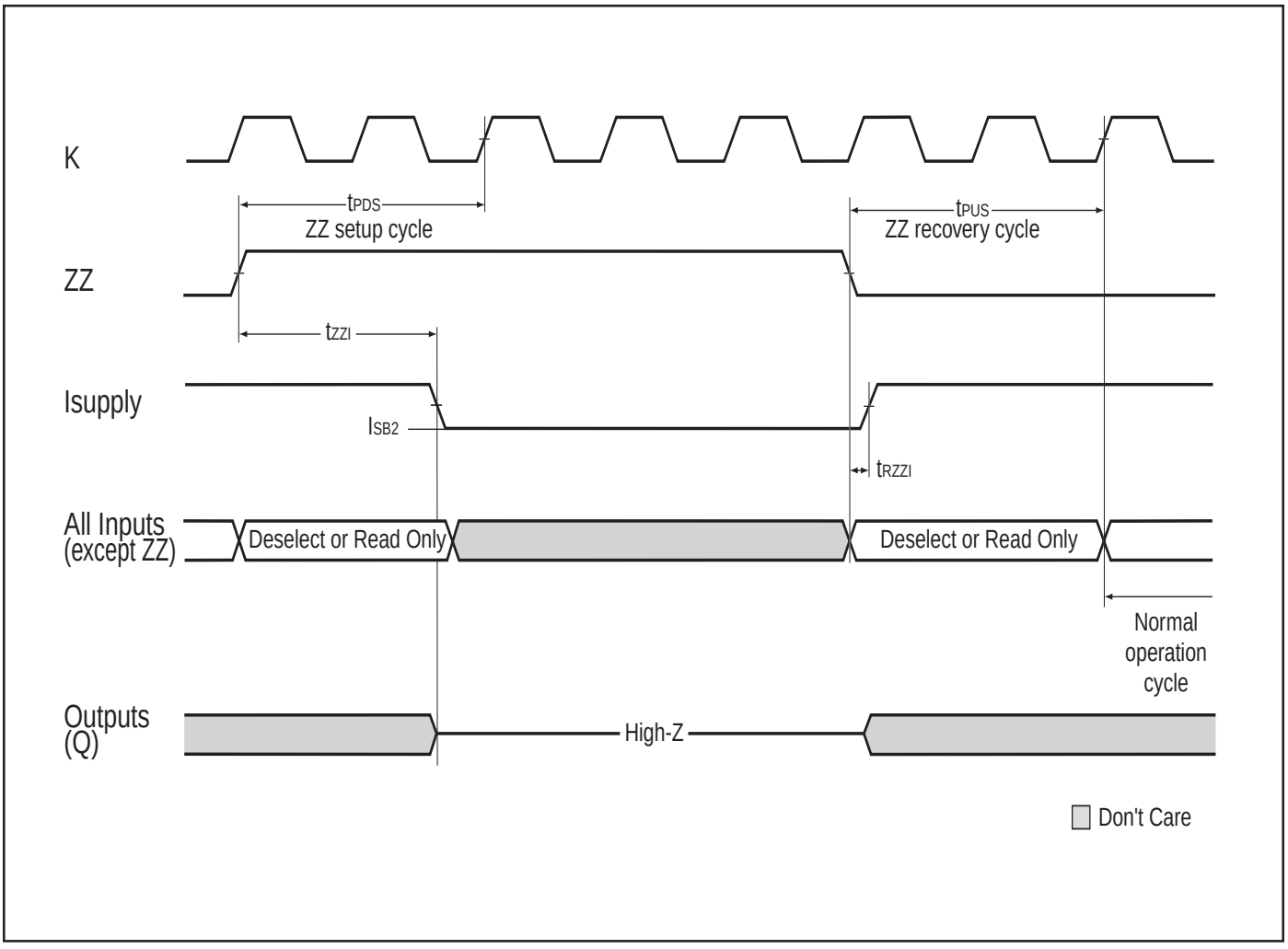
Symbol	Parameter	-250 Min.	-250 Max.	-200 Min.	-200 Max.	Unit
fmax	Clock Frequency	—	250	—	200	MHz
t_{KC}	Cycle Time	4.0	—	5	—	ns
t_{KH}	Clock High Time	1.7	—	2	—	ns
t_{KL}	Clock Low Time	1.7	—	2	—	ns
t_{KQ}	Clock Access Time	—	2.6	—	3.0	ns
t_{KQX}[2]	Clock High to Output Invalid	0.8	—	1.5	—	ns
t_{KQLZ}[2,3]	Clock High to Output Low-Z	0.8	—	1	—	ns
t_{KQHZ}[2,3]	Clock High to Output High-Z	—	2.6	—	3.0	ns
t_{OEQ}	Output Enable to Output Valid	—	2.6	—	3.0	ns
t_{OELZ}[2,3]	Output Enable to Output Low-Z	0	—	0	—	ns
t_{OEHZ}[2,3]	Output Disable to Output High-Z	—	2.6	—	3.0	ns
t_{AS}	Address Setup Time	1.0	—	1.2	—	ns
t_{WS}	Read/Write Setup Time	1.0	—	1.2	—	ns
t_{CES}	Chip Enable Setup Time	1.0	—	1.2	—	ns
t_{SE}	Clock Enable Setup Time	1.0	—	1.2	—	ns
t_{ADVS}	Address Advance Setup Time	1.0	—	1.2	—	ns
t_{DS}	Data Setup Time	1.0	—	1.2	—	ns
t_{AH}	Address Hold Time	0.5	—	0.5	—	ns
t_{HE}	Clock EnableHold Time	0.5	—	0.5	—	ns
t_{WH}	Write Hold Time	0.5	—	0.5	—	ns
t_{CEH}	Chip Enable Hold Time	0.5	—	0.5	—	ns
t_{ADVH}	Address Advance Hold Time	0.5	—	0.5	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{PDS}	ZZ High to Power Down	—	2	—	2	cyc
t_{PUS}	ZZ Low to Power Down	—	2	—	2	cyc

Notes:
1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

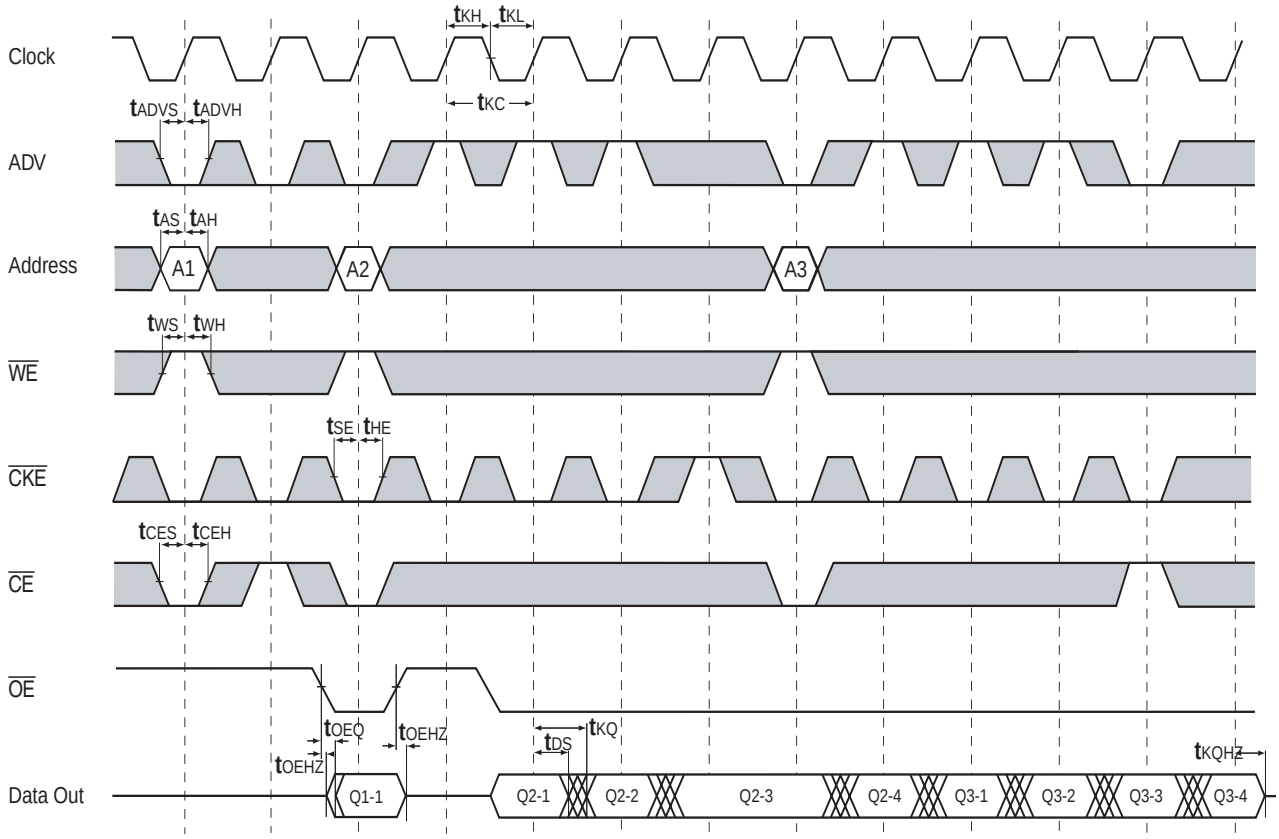
SLEEP MODE ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min.	Max.	Unit
I_{SB2}	Current during SLEEP MODE	ZZ ≥ Vih		150	mA
t_{PDS}	ZZ active to input ignored	ZZ ≥ Vih	2		cycle
t_{PUS}	ZZ inactive to input sampled	ZZ ≤ Vil	2		cycle
t_{ZZI}	ZZ active to SLEEP current	ZZ ≥ Vih	2		cycle
t_{RZZI}	ZZ inactive to exit SLEEP current	ZZ ≤ Vil	0		ns

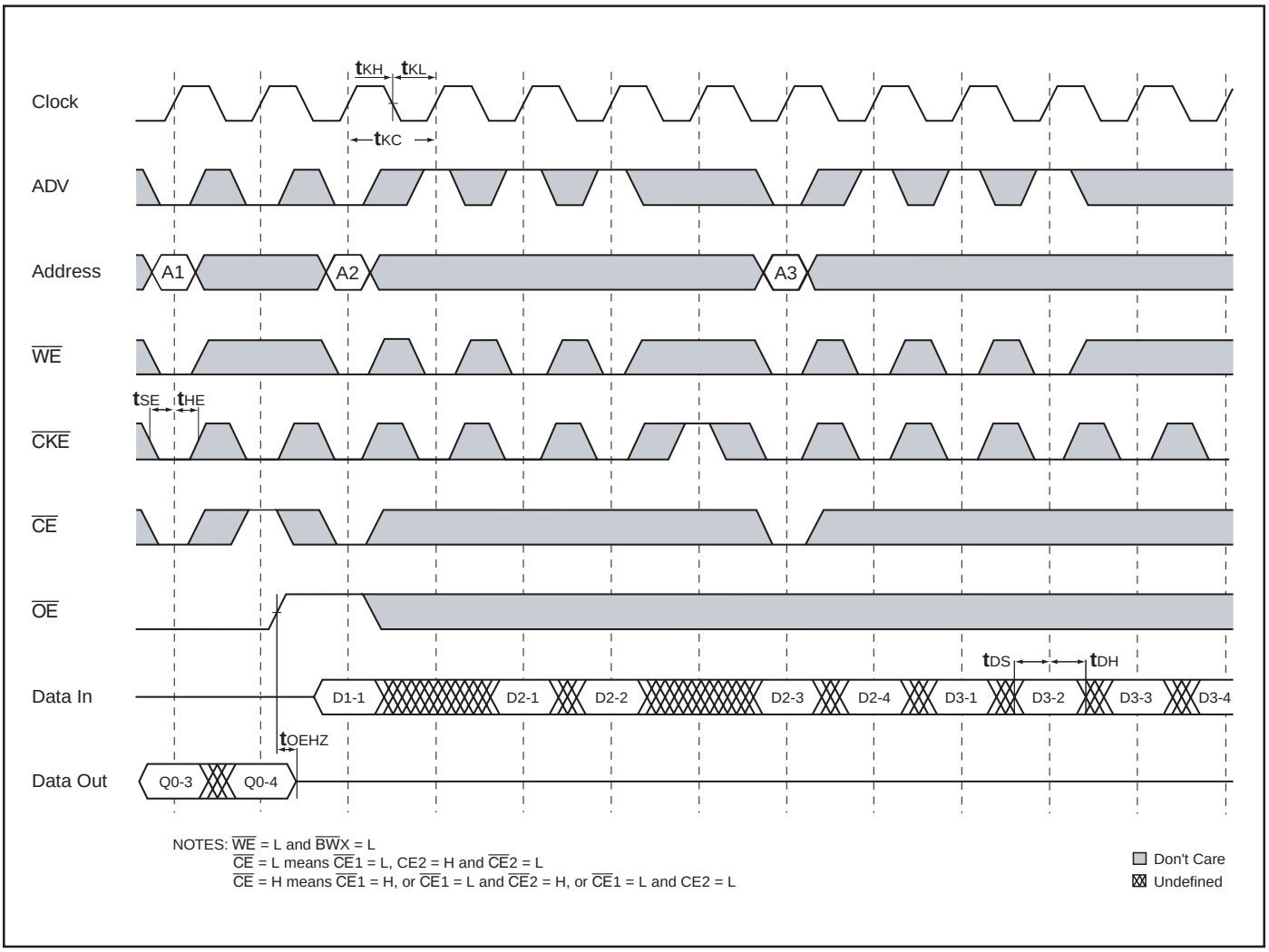
SLEEP MODE TIMING



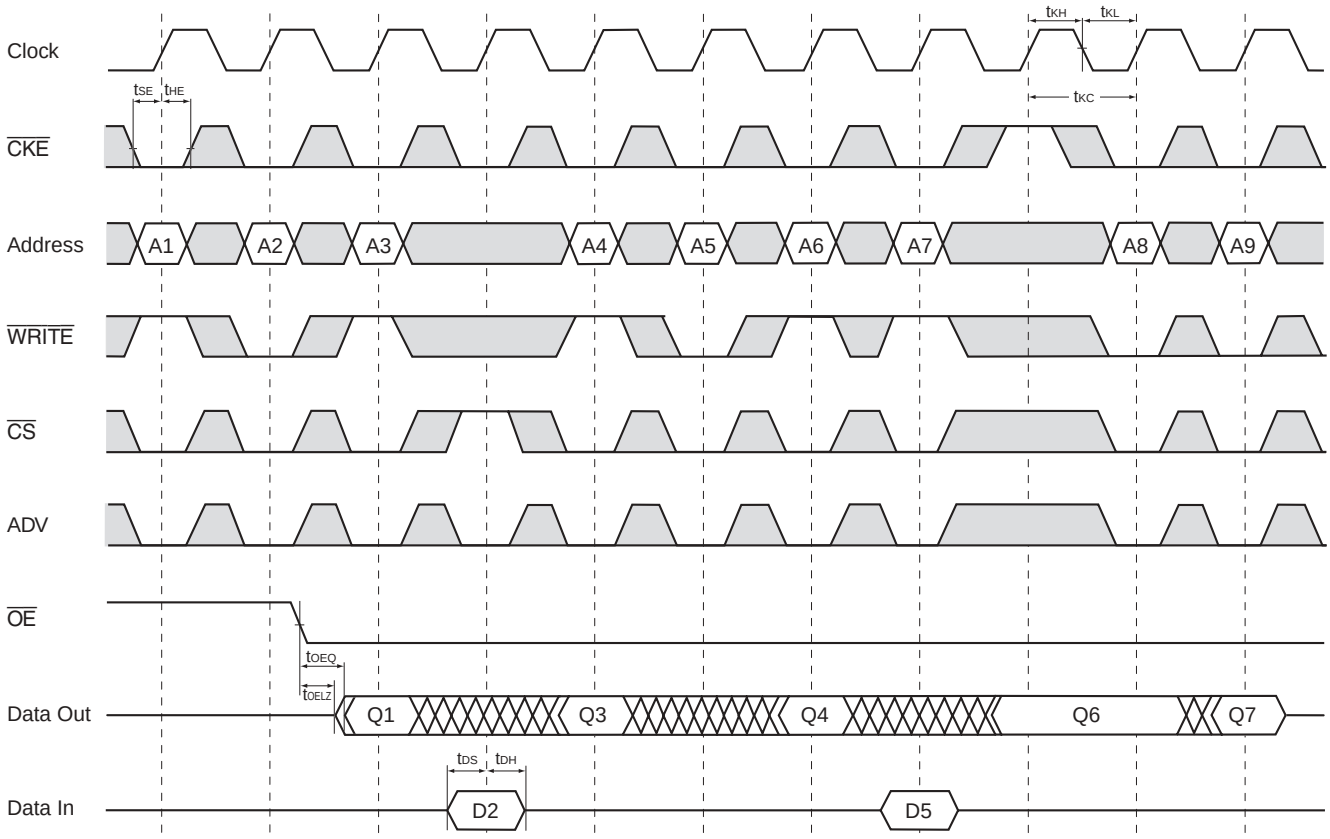
READ CYCLE TIMING



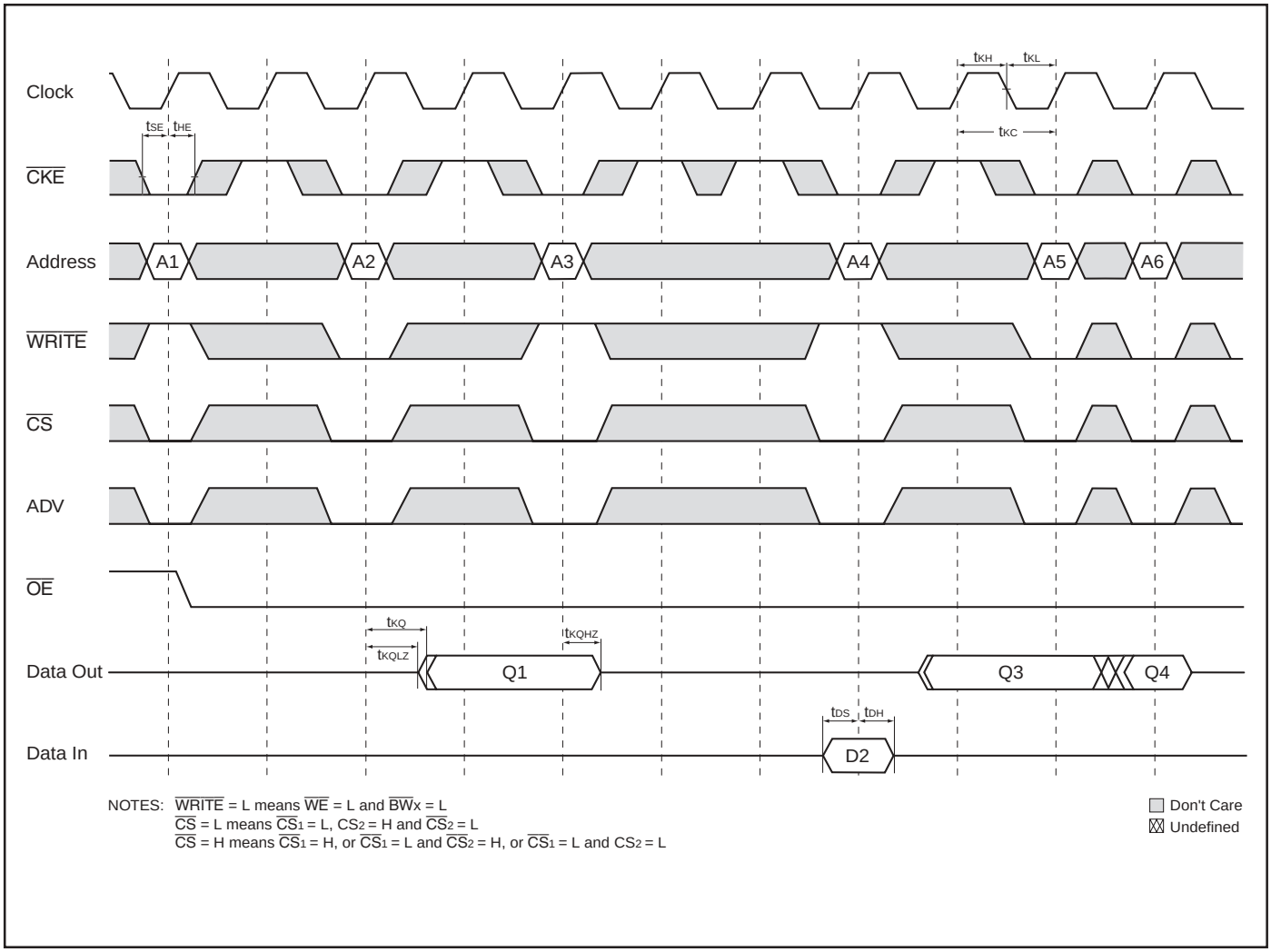
WRITE CYCLE TIMING



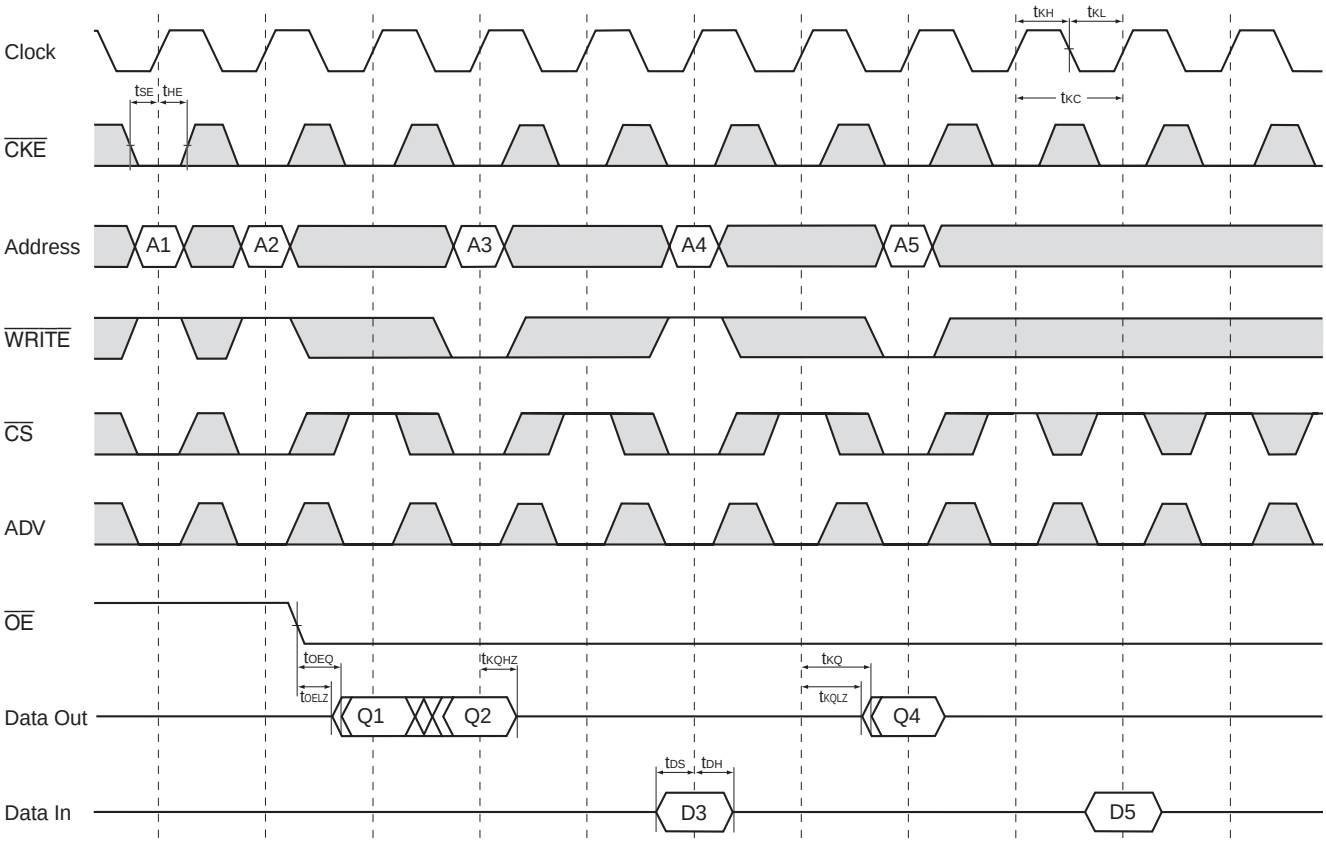
SINGLE READ/WRITE CYCLE TIMING



$\overline{CKE}$ OPERATION TIMING



$\overline{CS}$ OPERATION TIMING



IEEE 1149.1 SERIAL BOUNDARY SCAN (JTAG)

The IS61NVVP51236 and IS61NVVP25672 have a serial boundary scan Test Access Port (TAP) in the PBGA package only. This port operates in accordance with IEEE Standard 1149.1-1900, but does not include all functions required for full 1149.1 compliance. These functions from the IEEE specification are excluded because they place added delay in the critical speed path of the SRAM. The TAP controller operates in a manner that does not conflict with the performance of other devices using 1149.1 fully compliant TAPs. The TAP operates using JEDEC standard 1.8V I/O logic levels.

DISABLING THE JTAG FEATURE

The SRAM can operate without using the JTAG feature. To disable the TAP controller, TCK must be tied LOW (GND) to prevent clocking of the device. TDI and TMS are internally pulled up and may be disconnected. They may alternately be connected to V_{CC} through a pull-up resistor. TDO should be left disconnected. On power-up, the device will start in a reset state which will not interfere with the device operation.

TEST ACCESS PORT (TAP) - TEST CLOCK

The test clock is only used with the TAP controller. All inputs are captured on the rising edge of TCK and outputs are driven from the falling edge of TCK.

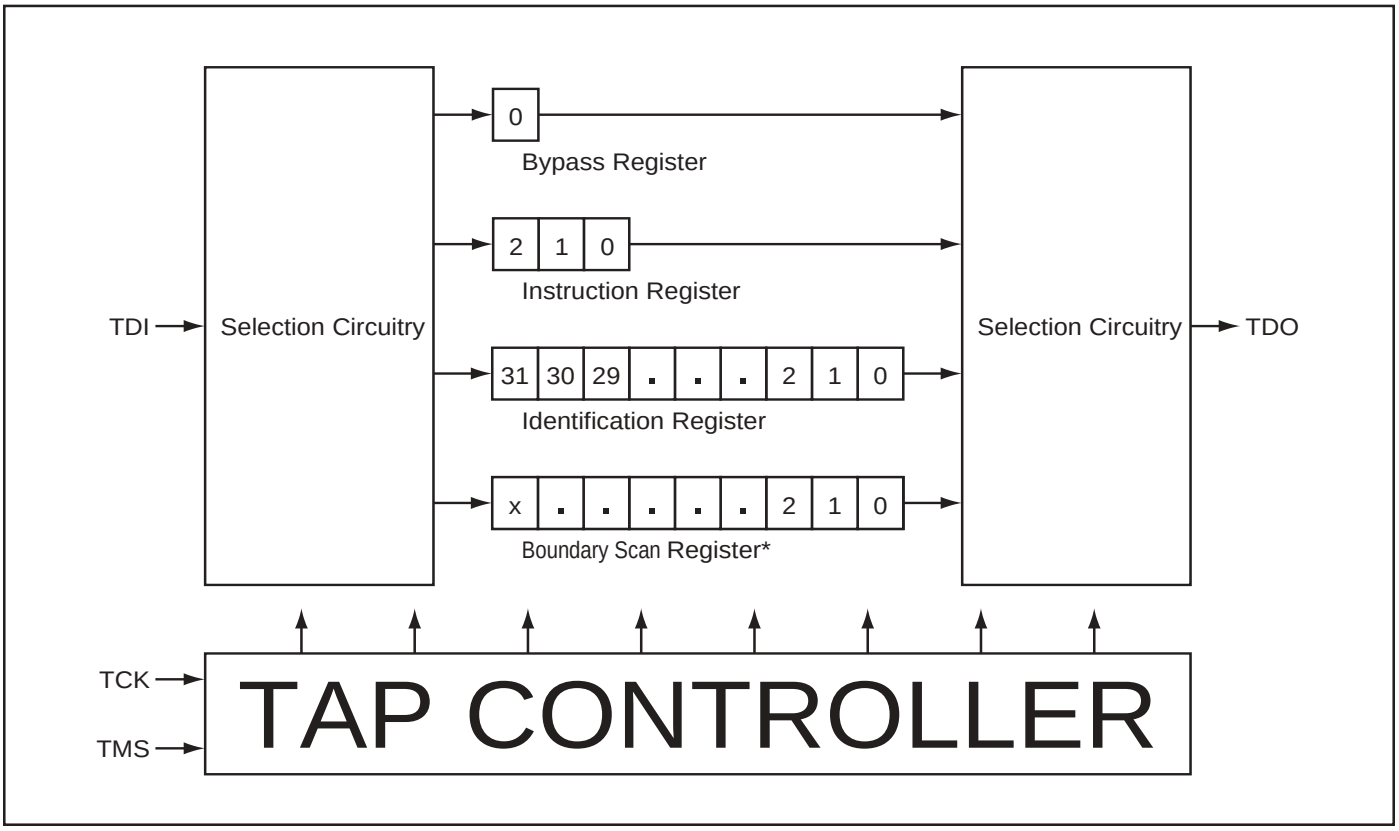
TEST MODE SELECT (TMS)

The TMS input is used to send commands to the TAP controller and is sampled on the rising edge of TCK. This pin may be left disconnected if the TAP is not used. The pin is internally pulled up, resulting in a logic HIGH level.

TEST DATA-IN (TDI)

The TDI pin is used to serially input information to the registers and can be connected to the input of any register. The register between TDI and TDO is chosen by the instruction loaded into the TAP instruction register. For information on instruction register loading, see the TAP Controller State Diagram. TDI is internally pulled up and can be disconnected if the TAP is unused in an application. TDI is connected to the Most Significant Bit (MSB) on any register.

TAP CONTROLLER BLOCK DIAGRAM



TEST DATA OUT (TDO)

The TDO output pin is used to serially clock data-out from the registers. The output is active depending on the current state of the TAP state machine (see TAP Controller State Diagram). The output changes on the falling edge of TCK and TDO is connected to the Least Significant Bit (LSB) of any register.

PERFORMING A TAP RESET

A Reset is performed by forcing TMS HIGH (V_{CC}) for five rising edges of TCK. RESET may be performed while the SRAM is operating and does not affect its operation. At power-up, the TAP is internally reset to ensure that TDO comes up in a high-Z state.

TAP REGISTERS

Registers are connected between the TDI and TDO pins and allow data to be scanned into and out of the SRAM test circuitry**.** Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK and output on the TDO pin on the falling edge of TCK.

Instruction Register

Three-bit instructions can be serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins. (See TAP Controller Block Diagram) At power-up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state as previously described.

When the TAP controller is in the CaptureIR state, the two least significant bits are loaded with a binary “01” pattern to allow for fault isolation of the board level serial test path.

Bypass Register

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain states. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This allows data to be shifted through the SRAM with minimal delay. The bypass register is set LOW (GND) when the BYPASS instruction is executed.

Boundary Scan Register

The boundary scan register is connected to all input and output pins on the SRAM. Several no connect (NC) pins are also included in the scan register to reserve pins for higher density devices. The x36 configuration has a 84-bit-long register and the x72 configuration has a 123-bit-long register. The boundary scan register is loaded with the contents of the RAM Input and Output ring when the TAP controller is in the Capture-DR state and then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD and SAMPLE Z instructions can be used to capture the contents of the Input and Output ring.

The Boundary Scan Order tables show the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

Scan Register Sizes

Register Name	Bit Size (x36)	Bit Size (x72)
Instruction	3	3
Bypass	1	1
ID	32	32
Boundary Scan	84	123

Identification (ID) Register

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded to the instruction register. The IDCODE is hardwired into the SRAM and can be shifted out when the TAP controller is in the Shift-DR state. The ID register has vendor code and other information described in the Identification Register Definitions table.

IDENTIFICATION (ID) REGISTER

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID REGISTER CONTENTS

	Die Revision Code				Not Used												I/O Configuration				ISSI Technology JEDEC Vendor ID Code										Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x72	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	1	0	1	0	1	0	1	1
x36	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	1	0	1	0	1	0	1	1

TAP INSTRUCTION SET

Eight instructions are possible with the three-bit instruction register and all combinations are listed in the Instruction Code table. Three instructions are listed as RESERVED and should not be used and the other five instructions are described below. The TAP controller used in this SRAM is not fully compliant with the 1149.1 convention because some mandatory instructions are not fully implemented. The TAP controller cannot be used to load address, data or control signals and cannot preload the Input or Output buffers. The SRAM does not implement the 1149.1 commands EXTEST or INTEST or the PRELOAD portion of SAMPLE/PRELOAD; instead it performs a capture of the Inputs and Output ring when these instructions are executed. Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted from the instruction register through the TDI and TDO pins. To execute an instruction once it is shifted in, the TAP controller must be moved into the Update-IR state.

EXTEST

EXTEST is a mandatory 1149.1 instruction which is to be executed whenever the instruction register is loaded with all 0s. Because EXTEST is not implemented in the TAP controller, this device is not 1149.1 standard compliant. The TAP controller recognizes an all-0 instruction. When an EXTEST instruction is loaded into the instruction register, the SRAM responds as if a SAMPLE/PRELOAD instruction has been loaded. There is a difference between the instructions, unlike the SAMPLE/PRELOAD instruction, EXTEST places the SRAM outputs in a High-Z state.

IDCODE

The IDCODE instruction causes a vendor-specific, 32-bit code to be loaded into the instruction register. It also places the instruction register between the TDI and TDO pins and allows the IDCODE to be shifted out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register upon power-up or whenever the TAP controller is given a test logic reset state.

SAMPLE Z

The SAMPLE Z instruction causes the boundary scan register to be connected between the TDI and TDO pins when the TAP controller is in a Shift-DR state. It also places all SRAM outputs into a High-Z state.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. The PRELOAD portion of this instruction is not implemented, so the TAP controller is not fully 1149.1 compliant. When the SAMPLE/PRELOAD instruction is loaded to the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the inputs and output pins is captured in the boundary scan register.

It is important to realize that the TAP controller clock operates at a frequency up to 10 MHz, while the SRAM clock runs more than an order of magnitude faster. Because of the clock frequency differences, it is possible that during the Capture-DR state, an input or output will under-go a transition. The TAP may attempt a signal capture while in transition (metastable state). The device will not be harmed, but there is no guarantee of the value that will be captured or repeatable results.

To guarantee that the boundary scan register will capture the correct signal value, the SRAM signal must be stabilized long enough to meet the TAP controller's capture set-up plus hold times (t_{CS} and t_{CH}). To insure that the SRAM clock input is captured correctly, designs need a way to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is not an issue, it is possible to capture all other signals and simply ignore the value of the CLK and $\overline{CLK}$ captured in the boundary scan register.

Once the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

Note that since the PRELOAD part of the command is not implemented, putting the TAP into the Update to the Update-DR state while performing a SAMPLE/PRELOAD instruction will have the same effect as the Pause-DR command.

BYPASS

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

RESERVED

These instructions are not implemented but are reserved for future use. Do not use these instructions.

JTAG TAP INSTRUCTION SET SUMMARY

Instruction	Code	Description
EXTEST(1)	000	Places the Boundary Scan Register between TDI and TDO. When EXTEST is selected, data will be driven out of the DQ pad.
IDCODE(1,2)	001	Preloads ID Register and places it between TDI and TDO.
SAMPLE-Z(1)	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all Data and Clock output drivers to High-Z.
RFU(1)	011	Do not use this instruction; Reserved for Future Use. Replicates BYPASS instruction. Places Bypass Register between TDI and TDO.
SAMPLE/PRELOAD(1)	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.
Private(1)	101	Private instruction.
RFU(1)	110	Do not use this instruction; Reserved for Future Use.
BYPASS(1)	111	Places Bypass Register between TDI and TDO.

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in Test-Logic-Reset state.

TAP ELECTRICAL CHARACTERISTICS Over the Operating Range(1,2)

Symbol	Parameter	Test Conditions	Min.	Max.	Units
V_{OH1}	Output HIGH Voltage	I_{OH} = –100 µA	Vcc –0.1	—	V
V_{OH2}	Output HIGH Voltage	I_{OH} = –8 mA	Vcc –0.4	—	V
V_{OL1}	Output LOW Voltage	I_{OL} = 100 µA	—	0.1	V
V_{OL2}	Output LOW Voltage	I_{OL} = 8 mA	—	0.4	V
V_{IH}	Input HIGH Voltage		1.2	V_{CC} +0.3	V
V_{IL}	Input LOW Voltage	I_{OLT} = 2mA	–0.3	0.6	V
I_X	Input Leakage Current	GND ≤ V I ≤ V_{DDQ}	–10	10	µA

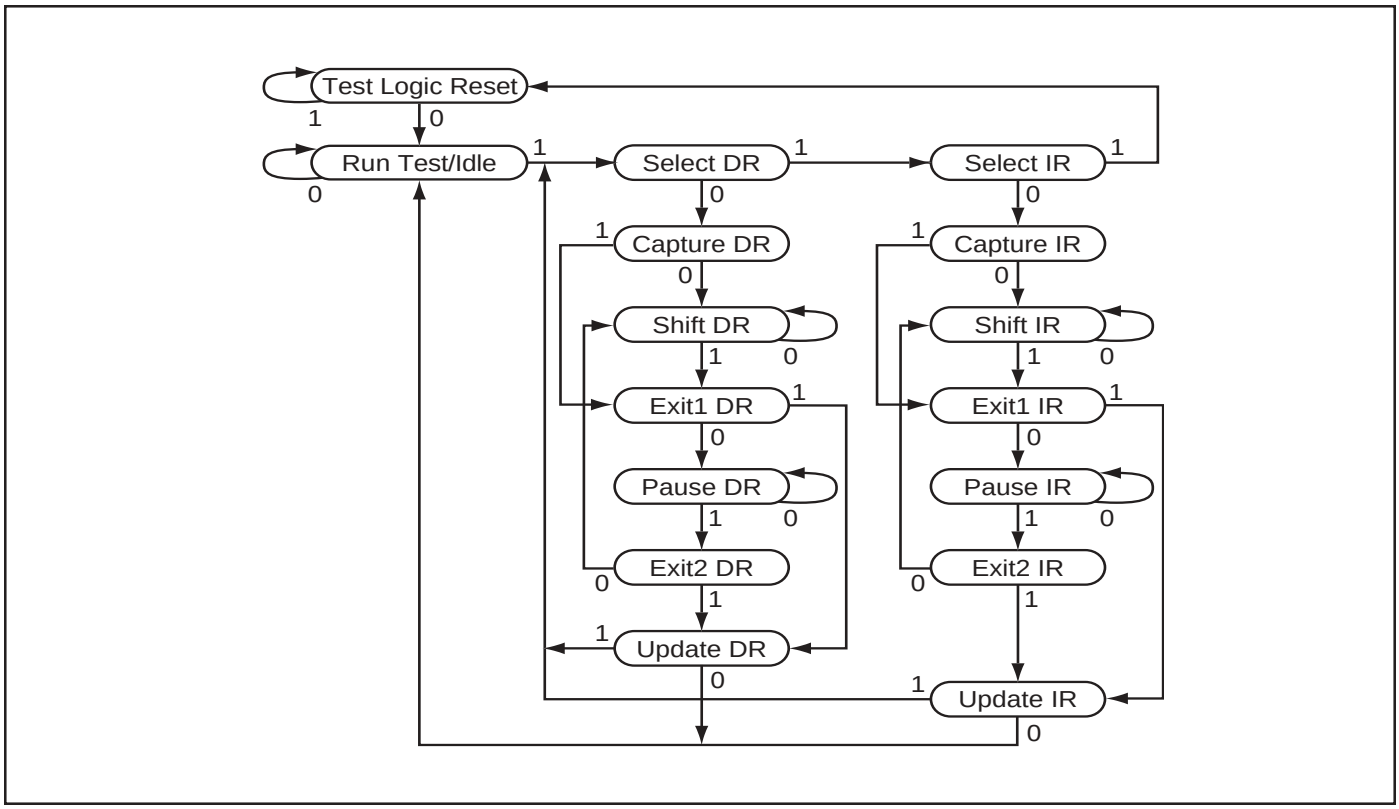
Notes:
1. All Voltage referenced to Ground.
2. Overshoot: V_{IH} (AC) ≤ V_{DD} +1.5V for t ≤ t_{TCYC}/2,
   Undershoot:V_{IL} (AC) ≤ 0.5V for t ≤ t_{TCYC}/2,
   Power-up: V_{IH} < 2.6V and V_{DD} < 2.4V and V_{DDQ} < 1.4V for t < 200 ms.

TAP AC ELECTRICAL CHARACTERISTICS[1] (OVER OPERATING RANGE)

Symbol	Parameter	Min.	Max.	Unit
t_{TCYC}	TCK Clock cycle time	100	—	ns
f_{TF}	TCK Clock frequency	—	10	MHz
t_{TH}	TCK Clock HIGH	40	—	ns
t_{TL}	TCK Clock LOW	40	—	ns
t_{TMSS}	TMS setup to TCK Clock Rise	10	—	ns
t_{TDIS}	TDI setup to TCK Clock Rise	10	—	ns
t_{CS}	Capture setup to TCK Rise	10	—	ns
t_{TMSH}	TMS hold after TCK Clock Rise	10	—	ns
t_{TDIH}	TDI Hold after Clock Rise	10	—	ns
t_{CH}	Capture hold after Clock Rise	10	—	ns
t_{TDOV}	TCK LOW to TDO valid	—	20	ns
t_{TDOX}	TCK LOW to TDO invalid	0	—	ns

Notes:
7. t_{CS} and t_{CH}refer to the set-up and hold time requirements of latching data from the boundary scan register.
8. Test conditions are specified using the load in TAP AC test conditions. t_R/t_F = 1 ns.

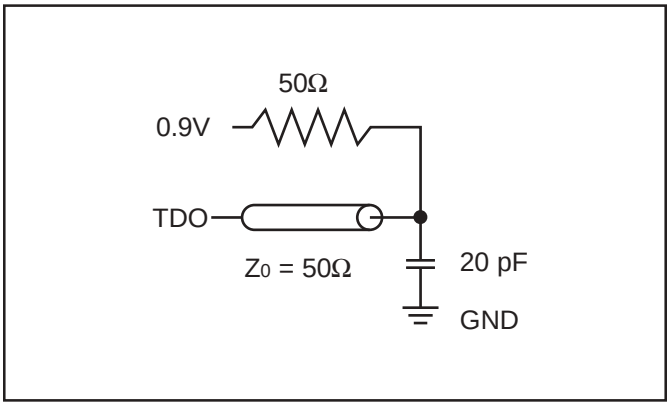
TAP CONTROLLER STATE DIAGRAM



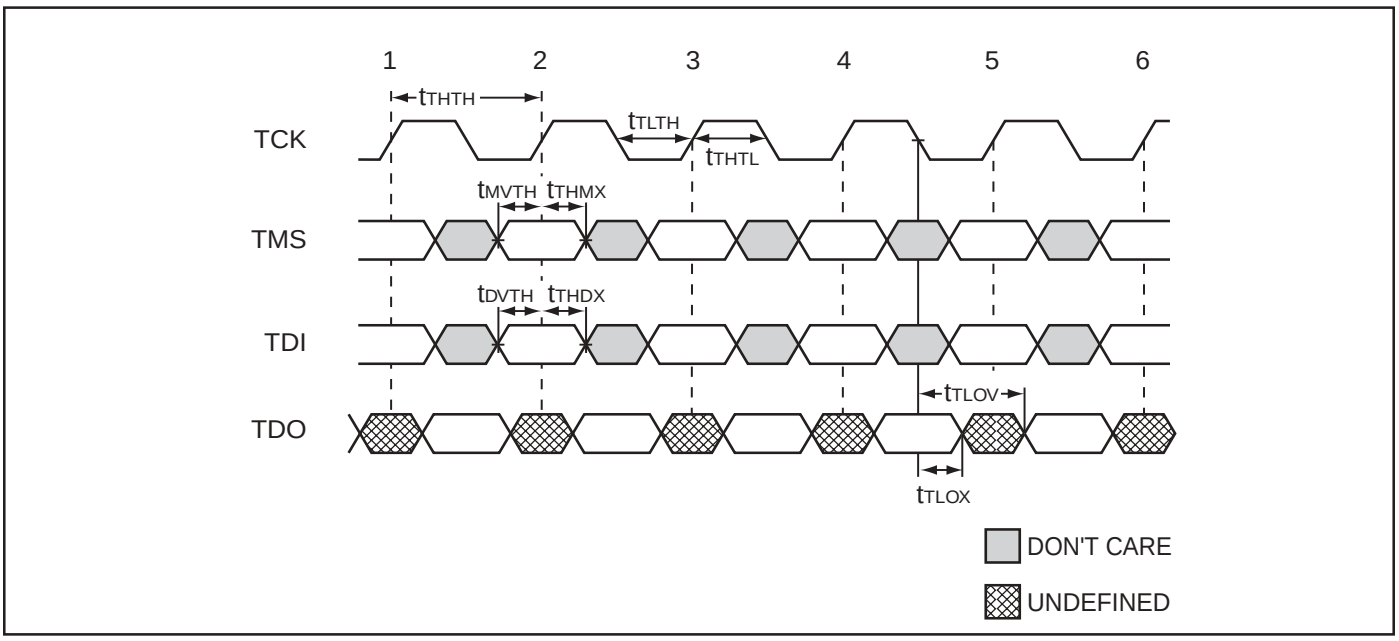
TAP AC TEST CONDITIONS

Input pulse levels	0.2 to 1.6V
Input rise and fall times	1ns
Input timing reference levels	0.9V
Output reference levels	0.9V
Test load termination supply voltage	0.9V

TAP OUTPUT LOAD EQUIVALENT



TAP TIMING



BOUNDARY SCAN ORDER ASSIGNMENTS (by Exit Sequence) PH =Place Holder

X72			X36		
Sequence	Pkg. Ball	Ball Location	Sequence	Pkg. Ball	Ball Location
1	A0	W6	1	A0	
2	A	V7	2	A	
3	A	V8	3	A	
4	A	U8	4	A	
5	A	V9	5	A	
6	A	U6	6	A	
7	PH(1)	U5	7	PH(1)	
8	A	W7	8	A	
9	PH(1)	U7	9	PH(1)	
10	Mode	T6	10	Mode	
11	NC(2)	M6	11	NC(2)	
12	NC(2)	J6	12	NC(2)	
13	$\overline{CKE}$	K6	13	$\overline{CKE}$	
14	$\overline{OE}$	D6	14	$\overline{OE}$	
15	PH(1)	C7	15	PH(1)	
16	$\overline{Be}$	C8			
17	$\overline{Ba}$	C9	16	$\overline{Ba}$	
18	$\overline{Bb}$	B8	17	$\overline{Bb}$	
19	$\overline{Bf}$	B9			
20	$\overline{W}$	B6	18	$\overline{W}$	
21	ADV	A6	19	ADV	
22	A	B7	20	A	
23	$\overline{CE2}$	A8	21	$\overline{CE2}$	
24	A	A9	22	A	
25	NC(2)	F6	23	NC	
26	A	A3	24	A	
27	CE2	A4	25	CE2	
28	A	A5	26	A	
29	A	A7	27	A	
		B5	28	A	
30	$\overline{Bc}$	B3	29	$\overline{Bc}$	
31	$\overline{Bg}$	B4			
32	$\overline{Bh}$	C3			
33	$\overline{Bd}$	C4	30	$\overline{Bd}$	
34	PH(1)	C5	31	PH(1)	
35	$\overline{CE}$	C6	32	$\overline{CE}$	
36	NC(2)	G6	33	NC	

Notes:
1.Input of PH register connected to VSS
2. NC = Don't care

BOUNDARY SCAN ORDER ASSIGNMENTS (by Exit Sequence) Continued:

X72			X36		
Sequence	Pkg. Ball	Ball Location	Sequence	Pkg. Ball	Ball Location
37	NC(2)	H6	34	NC(2)	
38	CK	K3	35	CK	
39	NC(2)	L6	36	NC(2)	
40	NC(2)	N6	37	NC(2)	
41	ZZ	P6	38	ZZ	
42	A	V3	39	A	
43	A	U4	40	A	
44	A	V4	41	A	
45	A	V5	42	A	
46	A	W5	43	A	
47	A	V6	44	A1	
48	DQd	W2	45	DQd	
49	DQd	W1	46	DQd	
50	DQd	V2	47	DQd	
51	DQd	V1	48	DQd	
52	DQd	U2	49	DQd	
53	DQd	U1	50	DQd	
54	DQd	T2	51	DQd	
55	DQd	T1	52	DQd	
56	DQPd	R1	53	DQPd	
57	DQPh	R2			
58	DQh	P2			
59	DQh	P1			
60	DQh	N2			
61	DQh	N1			
62	DQh	M2			
63	DQh	M1			
64	DQh	L2			
65	DQh	L1			
66	NC(2)	K2	54	NC(2)	
67	NC(2)	K1	55	NC(2)	
68	DQc	J2	56	DQc	
69	DQc	J1	57	DQc	
70	DQc	H2	58	DQc	
71	DQc	H1	59	DQc	
72	DQc	G2	60	DQc	
73	DQc	G1	61	DQc	

Notes:
1.Input of PH register connected to VSS
2. NC = Don't care

BOUNDARY SCAN ORDER ASSIGNMENTS (by Exit Sequence) Continued:

X72			X36		
Sequence	Pkg. Ball	Ball Location	Sequence	Pkg. Ball	Ball Location
74	DQc	F2	62	DQc	
75	DQc	F1	63	DQc	
76	DQPc	E2	64	DQPc	
77	DQPg	E1			
78	DQg	D2			
79	DQg	D1			
80	DQg	C2			
81	DQg	C1			
82	DQg	B2			
83	DQg	B1			
84	DQg	A2			
85	DQg	A1			
86	DQb	A10	65	DQb	
87	DQb	A11	66	DQb	
88	DQb	B10	67	DQb	
89	DQb	B11	68	DQb	
90	DQb	C10	69	DQb	
91	DQb	C11	70	DQb	
92	DQb	D10	71	DQb	
93	DQb	D11	72	DQb	
94	DQPb	E11	73	DQPb	
95	DQPf	E10			
96	DQf	F10			
97	DQf	F11			
98	DQf	G10			
99	DQf	G11			
100	DQf	H10			
101	DQf	H11			
102	DQf	J10			
103	DQf	J11			
104	NC(2)	K11	74	NC(2)	
105	NC(2)	K10	75	NC(2)	
106	DQa	L10	76	DQa	
107	DQa	L11	77	DQa	
108	DQa	M10	78	DQa	
109	DQa	M11	79	DQa	
110	DQa	N10	80	DQa	

Notes:
1.Input of PH register connected to VSS
2. NC = Don't care

BOUNDARY SCAN ORDER ASSIGNMENTS (by Exit Sequence) Continued:

X72			X36		
Sequence	Pkg. Ball	Ball Location	Sequence	Pkg. Ball	Ball Location
111	DQa	N11	81	DQa	
112	DQa	P10	82	DQa	
113	DQa8	P11	83	DQa8	
114	DQPa9	R10	84	DQPa9	
115	DQPe	R11			
116	DQe	T10			
117	DQe	T11			
118	DQe	U10			
119	DQe	U11			
120	DQe	V10			
121	DQe	V11			
122	DQe	W10			
123	DQe	W11			

Notes:
1.Input of PH register connected to VSS
2. NC = Don't care

ORDERING INFORMATION

Commercial Range: 0°C to +70°C

Frequency	Order Part Number	Package
256Kx72		
250	IS61NVVP25672-250B	PBGA
200	IS61NVVP25672-200B	PBGA
512Kx36		
250	IS61NVVP51236-250B	PBGA
200	IS61NVVP51236-200B	PBGA

Industrial Range: -40°C to +85°C

Frequency	Order Part Number	Package
256Kx72		
250	IS61NVVP25672-250BI	PBGA
200	IS61NVVP25672-200BI	PBGA
512Kx36		
250	IS61NVVP51236-250BI	PBGA
200	IS61NVVP51236-200BI	PBGA