Data Sheet | March 9, 2006 | FN9173.4

Li-ion/Li-Polymer Battery Charger

The ISL6298 is an integrated single-cell Li-ion or Li-polymer battery charger optimized for low current applications. The targeted applications include mini-disk (MD) players, Blue Tooth headsets, or other applications that use low-capacity battery cells.

The ISL6298 is a linear charger that charges the battery in a CC/CV (constant current/constant voltage) profile. The charge current is programmable with an external resistor up to 450mA during the CC phase. Once the battery voltage reaches 4.2V (or 4.1V), the charger enters CV mode and the charge current starts to reduce. When the charger current drops to a user-programmable threshold, the charger indicates the end-of-charge with a STATUS pin. The charger does not actually terminate until a user-programmable total fast charge time is reached. If the battery voltage drops to a recharge threshold after termination, the charger will re-charge the battery to its full capacity. The charger preconditions the battery with 20% of the programmed CC current if the battery voltage is below 2.8V. The total precharge time is limited to 1/8 of the total fast charge time.

The ISL6298 features charge current thermal foldback to guarantee safe operation when the printed circuit board is space-limited for thermal dissipation. Additional features include an NTC thermistor interface for monitoring the ambient temperature, the ability to disable the time limit of the fast charge, an FAULT indication, and a thermally enhanced QFN or DFN package.

Ordering Information

PART # (NOTE)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-FREE)	PKG. DWG. #
ISL6298CR4Z	6298CR4Z	-20 to 70	16 Ld 4x4 QFN	L16.4x4
ISL6298CR4Z-T	6298CR4Z	16 Ld 4x4 QFN Tape and Reel		
ISL6298-2CR3Z	982Z	-20 to 70	10 Ld 3x3 DFN	L10.3x3
ISL6298-2CR3Z-T	982Z	10 Ld 3x3 DFN Tape and Reel		
ISL6298-2CR4Z	6298CR4Z	-20 to 70	16 Ld 4x4 QFN	L16.4x4
ISL6298-2CR4Z-T	6298CR4Z	16 Ld 4x4 QFN Tape and Reel		

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Complete Charger for Single-Cell Li-ion Batteries
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- 1% Voltage Accuracy
- Programmable Current Limit up to 450mA
- Programmable End-of-Charge Current
- Preconditioning with 20% Fast Charge Current
- 10% Accuracy at 250mA
- Charge Current Thermal Foldback
- NTC Thermistor Interface for Battery Temperature Monitor
- User Programmable Safety Timer
- Ambient Temperature Range: -20°C to 70°C
- Thermally-Enhanced QFN Packages
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

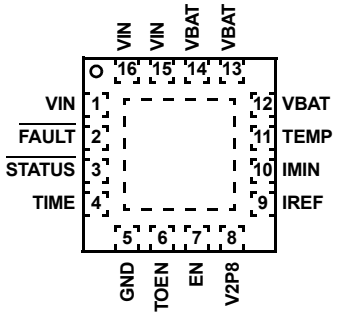
- MD Players, Blue-Tooth Headsets and MP3 Players
- Portable Instruments
- PDAs, Cell Phones and Smart Phones
- Stand-Alone Chargers

Related Literature

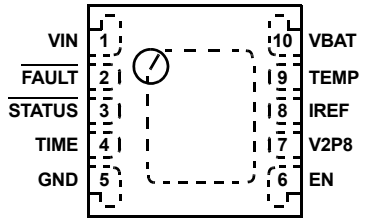
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Pinouts

ISL6298 (16 LD QFN)
TOP VIEW



ISL6298 (10 LD DFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . -0.3 to 7V
Output Pin Voltage (VBAT) . . . . . -0.3 to 5.5V
Signal Input Voltage (TOEN, TIME, IREF, IMIN) . . . . . -0.3 to 3.2V
Output Pin Voltage (STATUS, FAULT) . . . . . -0.3 to 7V
Charge Current 500mA

Recommended Operating Conditions

Ambient Temperature Range . . . . . -20°C to 70°C
Supply Voltage, VIN . . . . . 4.3V to 6.5V
Charge Current . . . . . 75mA to 450mA

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
4x4 QFN Package	41	4
3x3 DFN Package	46	4

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
2. θ_{JC}, "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising VIN Threshold			3.0	3.4	4.0	V
Falling VIN Threshold (Note 3)			2.25	2.4	2.65	V
STANDBY CURRENT						
VBAT Pin Sink Current	$I_{STANDBY}$	VIN floating or EN = LOW	-	-	3.0	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN pulled low	-	30	-	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN floating	-	1	-	mA
VOLTAGE REGULATION						
Output Voltage	V_{CH}	For ISL6298 only	4.059	4.10	4.141	V
Output Voltage	V_{CH}	For ISL6298-2 only	4.158	4.20	4.242	V
Power MOSFET On Resistance		VBAT = 3.7V, I_{CHARGE} = 0.3A	-	0.5	-	Ω
CHARGE CURRENT						
Constant Charge Current	I_{CHARGE}	R_{IREF} = 80kΩ, V_{BAT} = 3.7V	225	250	275	mA
Trickle Charge Current	$I_{TRICKLE}$	R_{IREF} = 80kΩ, V_{BAT} = 2.0V	45	55	64	mA
Constant Charge Current	I_{CHARGE}	V_{IREF} > 1.2V, V_{BAT} = 3.7V	-	255	-	mA
Trickle Charge Current	$I_{TRICKLE}$	V_{IREF} > 1.2V, V_{BAT} = 2.0V	-	52	-	mA
Constant Charge Current	I_{CHARGE}	V_{IREF} < 0.4V, V_{BAT} = 3.7V, T_A = 25°C	75	100	125	mA
Constant Charge Current	I_{CHARGE}	V_{IREF} < 0.4V, V_{BAT} = 3.7V, 0°C ~ 50°C	70	100	130	mA
Trickle Charge Current	$I_{TRICKLE}$	V_{IREF} < 0.4V, V_{BAT} = 2.0V	-	23	-	mA
End-of-Charge Threshold	I_{EOC}	R_{IMIN} = 80kΩ	14	25	36	mA
RECHARGE THRESHOLD						
Recharge Voltage Threshold	V_{RECHRG}	For ISL6298 only	-	3.9	-	V
Recharge Voltage Threshold	V_{RECHRG}	For ISL6298-2 only	-	4.0	-	V

Electrical Specifications Typical values are tested at VIN = 5V and 25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to 70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRICKLE CHARGE THRESHOLD						
Trickle Charge Threshold Voltage	V_{MIN}	For ISL6298 only	2.63	2.73	2.93	V
Trickle Charge Threshold Voltage	V_{MIN}	For ISL6298-2 only	2.7	2.8	3.0	V
TEMPERATURE MONITORING						
Low Battery Temperature Threshold	V_{TMIN}	V2P8 = 3.0V	1.45	1.51	1.57	V
Low Battery Temperature Hysteresis		V2P8 = 3.0V	-	220	-	mV
High Battery Temperature Threshold	V_{TMAX}	V2P8 = 3.0V	0.36	0.38	0.40	V
High Battery Temperature Hysteresis		V2P8 = 3.0V	-	60	-	mV
Battery Removal Threshold	V_{RMV}	V2P8 = 3.0V	-	2.25	-	V
Charge Current Foldback Threshold (Note 4)	T_{FOLD}		85	100	115	°C
Current Foldback Gain (Note 4)	G_{FOLD}		-	25	-	mA/°C
OSCILLATOR						
Oscillation Period	T_{OSC}	C_{TIME} = 15nF	2.4	3.0	3.6	ms
LOGIC INPUT AND OUTPUT						
TOEN Input High			2.0	-	-	V
TOEN and EN Input Low			-	-	0.8	V
IREF and IMIN Input High			1.2	-	-	V
IREF and IMIN Input Low			-	-	0.4	V
STATUS/FAULT Sink Current		Pin Voltage = 0.8V	5	-	-	mA

NOTES:

3. The POR falling edge voltage is guaranteed to be lower than the Trickle Charge Threshold Voltage (V_{MIN}) by actual tests.
4. Guaranteed by characterization.

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, $R_{IREF} = R_{IMIN}$ = 80kΩ, V_{BAT} = 3.7V, Unless Otherwise Noted

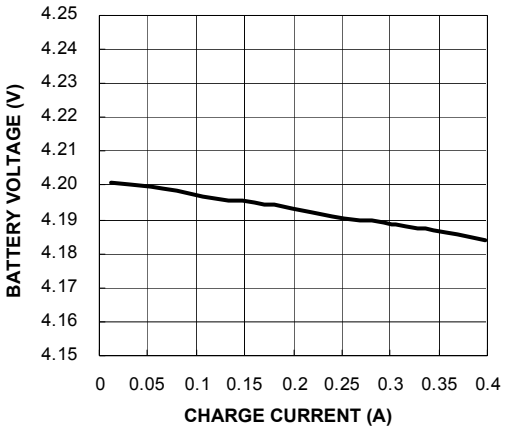


FIGURE 1. CHARGER OUTPUT VOLTAGE vs CHARGE CURRENT

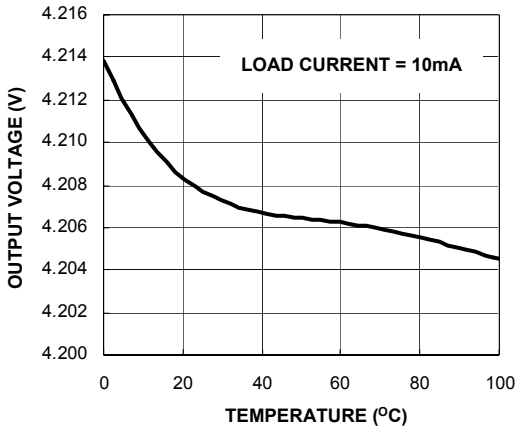


FIGURE 2. CHARGER OUTPUT VOLTAGE vs TEMPERATURE

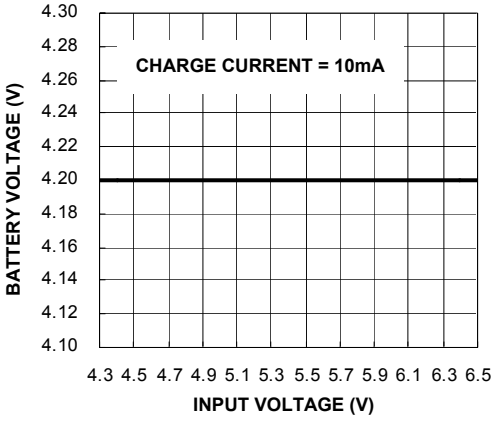


FIGURE 3. CHARGER OUTPUT VOLTAGE vs INPUT VOLTAGE CHARGE CURRENT IS 50mA

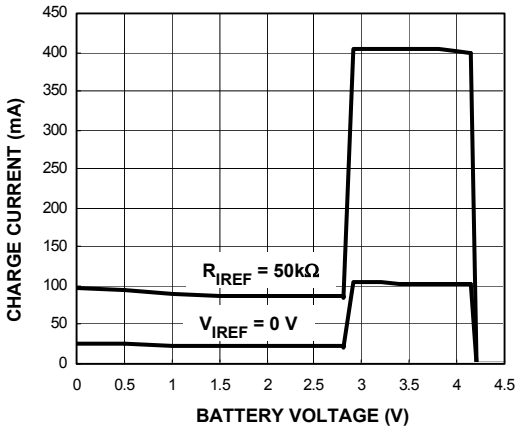


FIGURE 4. CHARGE CURRENT vs BATTERY VOLTAGE

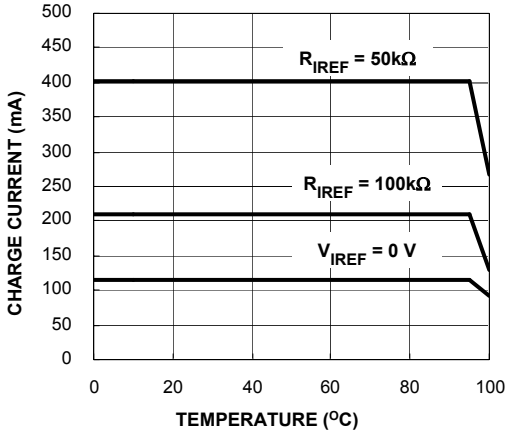


FIGURE 5. CHARGE CURRENT vs AMBIENT TEMPERATURE

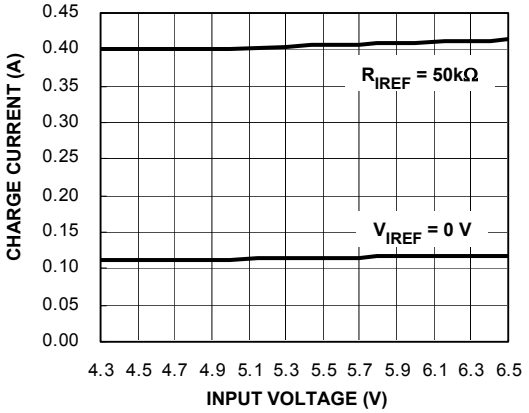


FIGURE 6. CHARGE CURRENT vs INPUT VOLTAGE

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, Unless Otherwise Noted **(Continued)**

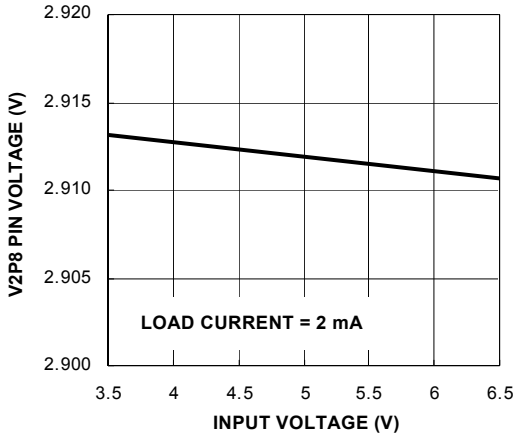


FIGURE 7. V2P8 OUTPUT vs INPUT VOLTAGE

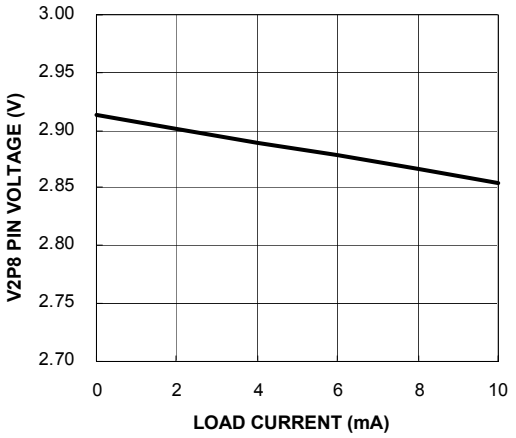


FIGURE 8. V2P8 OUTPUT vs ITS LOAD CURRENT

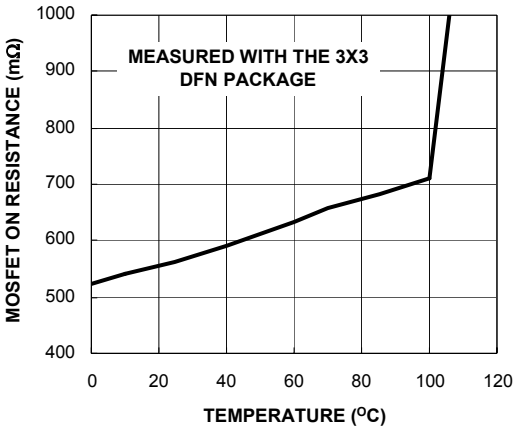


FIGURE 9. $r_{DS(ON)}$ vs TEMPERATURE AT 3.7V OUTPUT

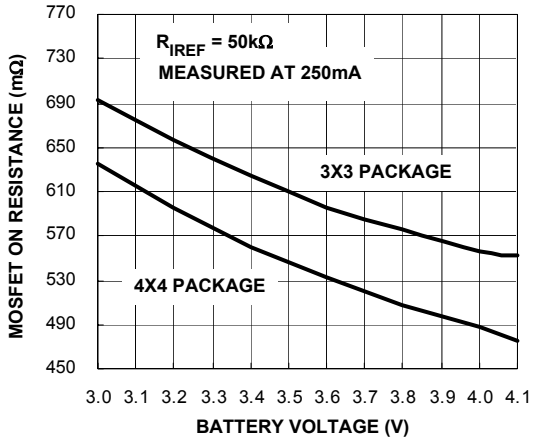


FIGURE 10. $r_{DS(ON)}$ vs OUTPUT VOLTAGE USING CURRENT LIMITED ADAPTERS

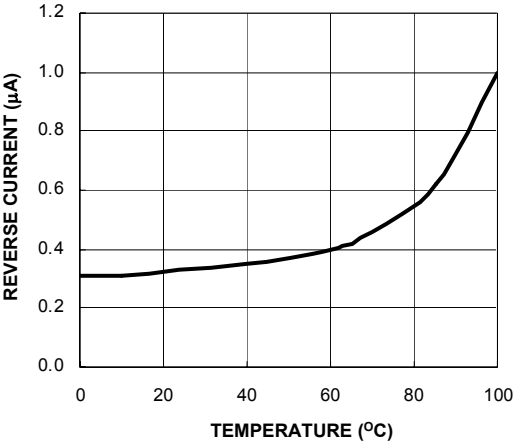


FIGURE 11. REVERSE CURRENT vs TEMPERATURE

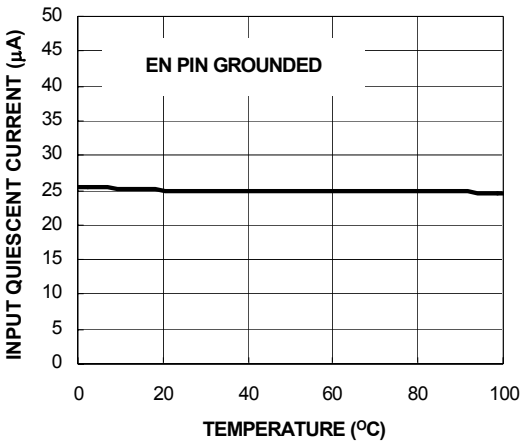


FIGURE 12. INPUT QUIESCENT CURRENT vs TEMPERATURE

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = 25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, Unless Otherwise Noted **(Continued)**

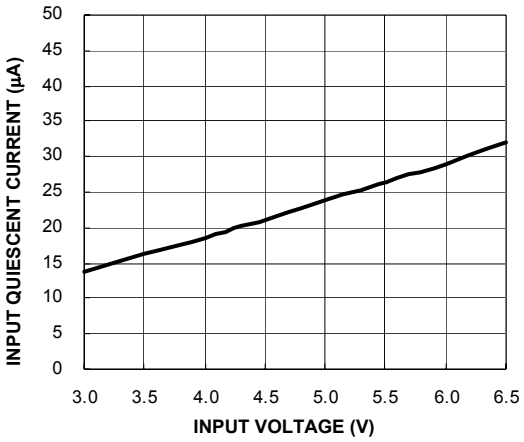


FIGURE 13. INPUT QUIESCENT CURRENT vs INPUT VOLTAGE WHEN SHUTDOWN

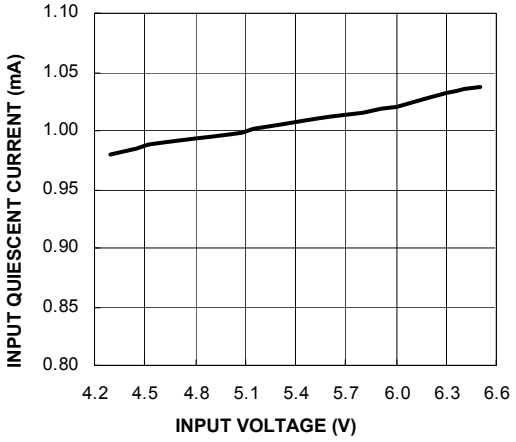


FIGURE 14. INPUT QUIESCENT CURRENT vs INPUT VOLTAGE WHEN NOT SHUTDOWN

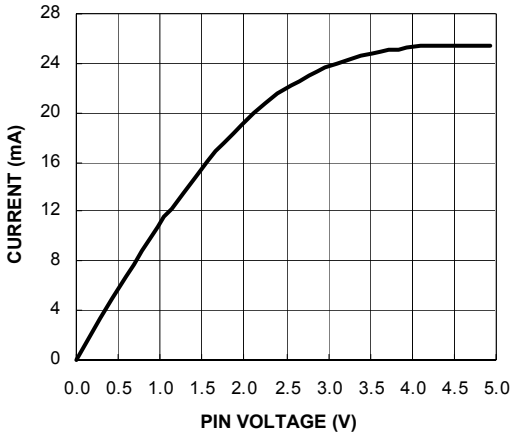


FIGURE 15. STATUS/FAULT PIN VOLTAGE vs CURRENT WHEN THE OPEN-DRAIN MOSFET TURNS ON

Pin Description

VIN (Pin 1, 15, 16 for 4x4; Pin 1 for 3x3)

VIN is the input power source. Connect to a wall adapter.

Fault (Pin 2)

FAULT is an open-drain output indicating fault status. This pin is pulled to LOW under any fault conditions.

Status (Pin 3)

STATUS is an open-drain output indicating charging and inhibit states. The STATUS pin is pulled LOW when the charger is charging a battery.

Time (Pin 4)

The TIME pin determines the oscillation period by connecting a timing capacitor between this pin and GND. The oscillator also provides a time reference for the charger.

GND (Pin 5)

GND is the connection to system ground.

TOEN (Pin 6 for 4x4; N/A for 3x3)

TOEN is the TIMEOUT enable input pin. Pulling this pin to LOW disables the TIMEOUT function. Leaving this pin HIGH or floating enables the TIMEOUT limit. For the 3x3 DFN package, this pin is left floating internally.

EN (Pin 7 for 4x4; Pin 6 for 3x3)

EN is the enable logic input. Connect the EN pin to LOW to disable the charger or leave it floating to enable the charger.

V2P8 (Pin 8 for 4x4; Pin 7 for 3x3)

This is a 2.8V reference voltage output. This pin outputs a 2.8V voltage source when the input voltage is above POR threshold and outputs zero otherwise. The V2P8 pin can be used as an indication for adapter presence.

IREF (Pin 9 for 4x4; Pin 8 for 3x3)

This is the programming input for the constant charging current.

IMIN (Pin 10 for 4x4; N/A for 3x3)

IMIN is the programmable input for the end-of-charge current. For the 3x3 DFN package, this pin is shorted to the V2P8 pin internally.

TEMP (Pin 11 for 4x4; Pin 9 for 3x3)

TEMP is the input for an external NTC thermistor. The TEMP pin is also used for battery removal detection.

VBAT (Pin 12, 13, 14 for 4x4; Pin 10 for 3x3)

VBAT is the connection to the battery. Typically a 10µF Tantalum capacitor is needed for stability when there is no battery attached. When a battery is attached, only a 1µF ceramic capacitor is required.

Typical Applications

4x4 QFN Package Options

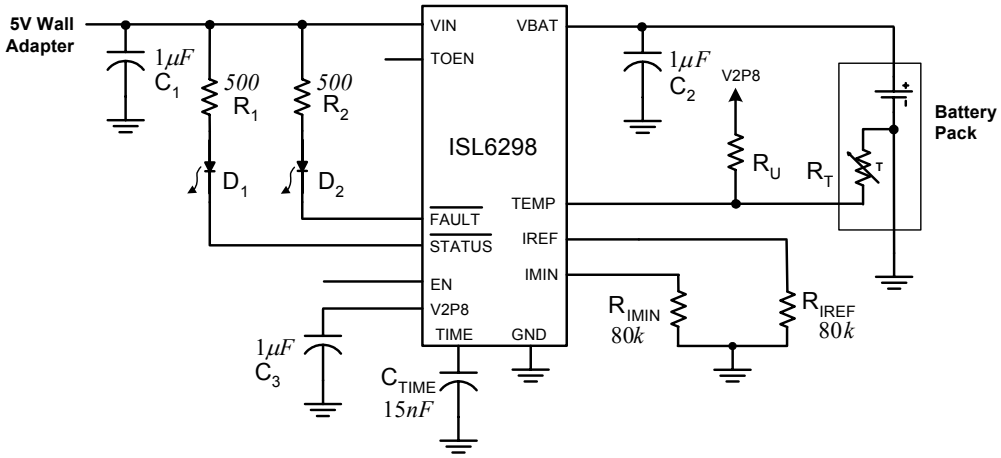


FIGURE 16. TYPICAL APPLICATION CIRCUIT FOR THE 4x4 QFN PACKAGE OPTIONS

Typical Applications (Continued)

3x3 DFN Package Option

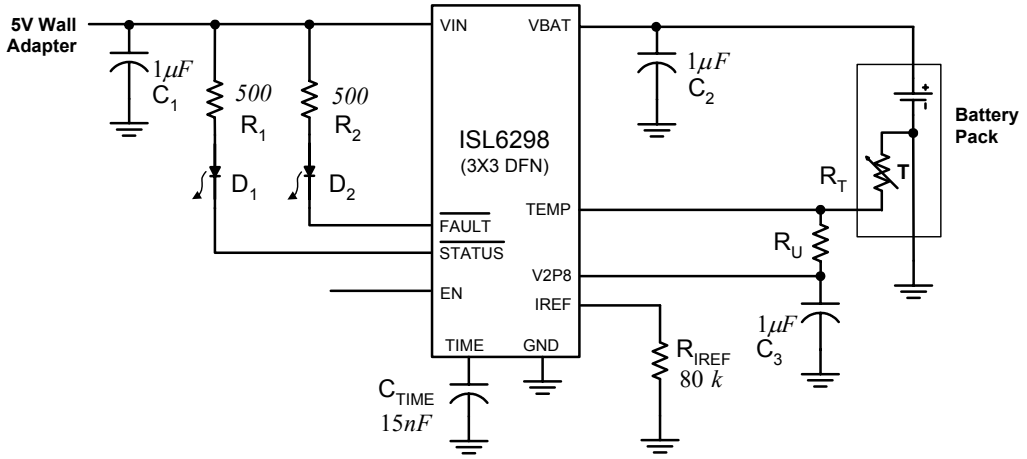


FIGURE 17. TYPICAL APPLICATION CIRCUIT FOR THE 3x3 DFN PACKAGE OPTION

3x3 DFN Package Option

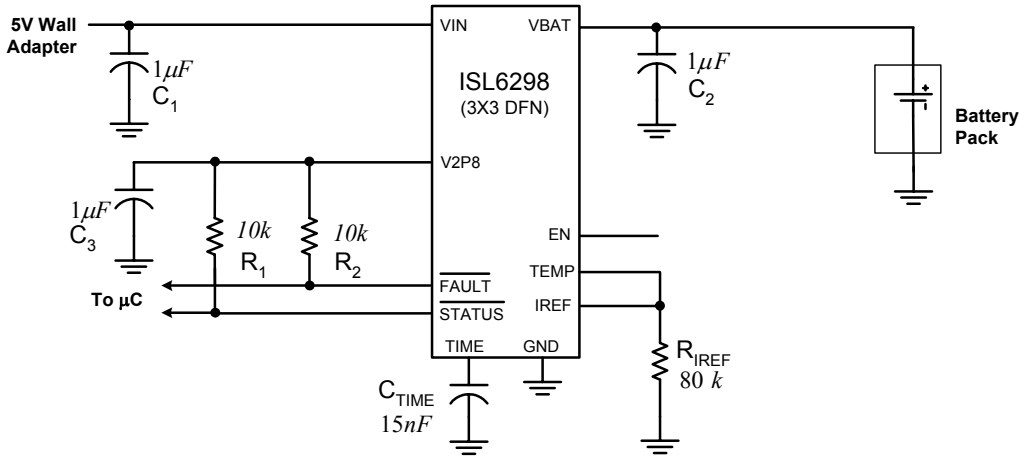
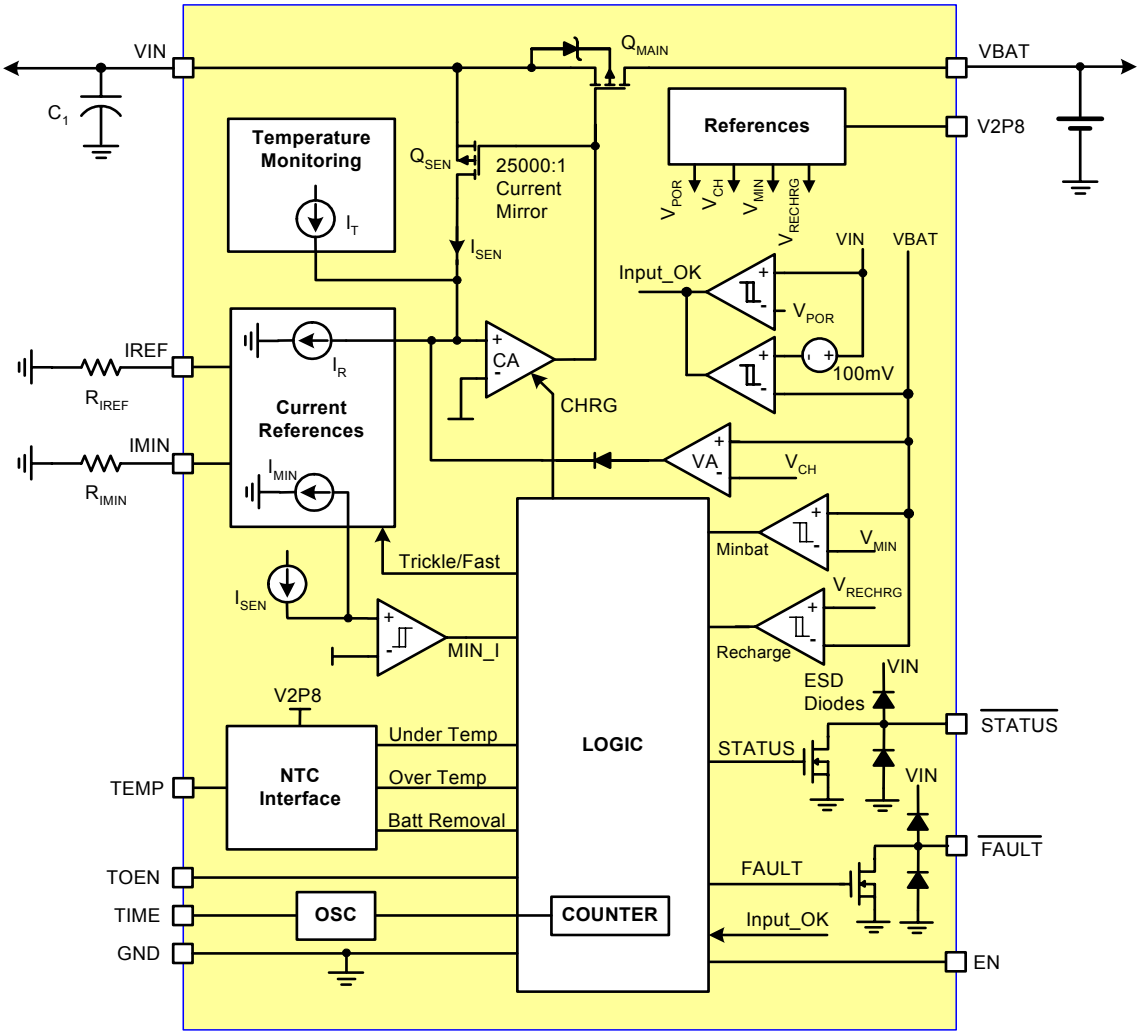


FIGURE 18. TYPICAL APPLICATION CIRCUIT FOR NOT USING AN NTC THERMISTOR AND INTERFACING TO A MICRO-COMPUTER. THE TEMP PIN IS SHORT-CIRCUITED TO IREF PIN. THE INDICATIONS USES V2P8 PIN OUTPUT AS THE PULL-UP VOLTAGE.

Block Diagram



NOTE: For the 3x3 DFN package, the TOEN pin is left floating and the IMIN pin is connected to the V2P8 pin internally.

FIGURE 19. BLOCK PROGRAM

Theory of Operation

The ISL6298 is an integrated charger optimized for low-capacity single-cell Li-ion or Li-polymer batteries. It charges a battery with the constant current (CC) and constant voltage (CV) profile. The charge current is trimmed to have better than 10% accuracy at 250mA and is programmable up to 450mA. The charge voltage has 1% accuracy.

Figure 20 shows the typical operating waveforms after power on. The power is applied at t_0. When the input voltage reaches the power-on reset (POR) threshold at t_1, the V2P8 pin starts to output a 2.8V supply. This supply also powers the internal control circuit. The POR initiates a charge cycle. Six different ways can initiate a charge cycle, as listed in Table 1.

TABLE 1. EVENTS THAT LEADS TO A NEW CHARGE CYCLE

#	EVENT
1	Power on Reset
2	The VIN pin voltage drops below the VBAT pin voltage and then rises back above the VBAT pin voltage
3	A new battery being inserted (detected by TEMP pin)
4	The battery voltage drops below a recharge threshold after completing a charge cycle
5	recovery from a battery over-temperature fault
6	the EN pin is toggled from GND to floating

A charge cycle goes through a trickle mode (t_1 to t_2), a constant current (CC) mode (t_2 to t_3) and a constant voltage (CV) mode (t_3 to t_5). The total fast charge (CC and CV) time (t_2 to t_5) is programmed by users to prevent charging a faulty battery for an excessively long time. At the end of the fast charge time (t_5), the charger is terminated. The charger must reach an end-of-charge (EOC) condition before the termination; otherwise, the charger issues a fault indication through the FAULT pin. The charger issues a logic low signal at the STATUS pin at the beginning of a charge cycle. When the EOC condition is reached, the STATUS rises to high, as shown at t_4.

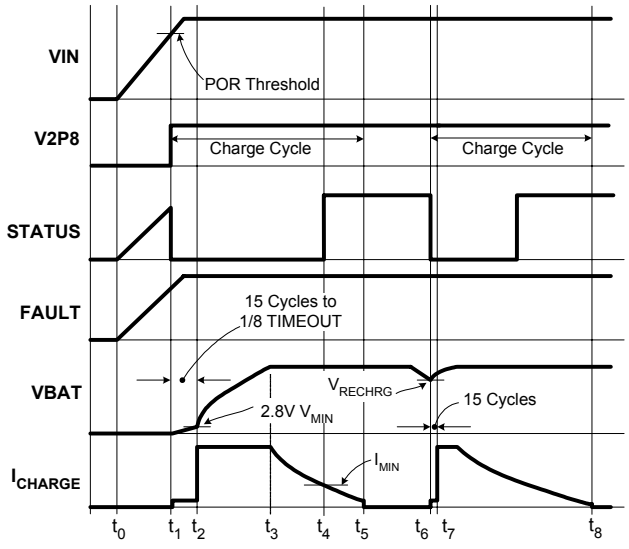


FIGURE 20. TYPICAL OPERATING WAVEFORMS

After termination, if the battery voltage drops below a recharge threshold (t_6 in Figure 20), a re-charge cycle will take place. The total time for the recharge cycle is the total fast charge time (t_7 to t_8). The trickle charge time is negligible in a recharge cycle. More detailed description for the operation is given below.

Power on Reset (POR)

The ISL6298 resets itself as the input voltage rises above the POR rising threshold. The V2P8 pin outputs a 2.8V voltage, the internal oscillator starts to oscillate, the internal timer is reset, and the charger begins to charge the battery. The two indication pins, STATUS and FAULT, indicate a LOW and a HIGH logic signal respectively. Figure 20 illustrates the startup of the charger between t_0 to t_2.

The ISL6298 has a typical rising POR threshold of 3.4V and a falling POR threshold of 2.4V. The 2.4V falling threshold guarantees charger operation with a current-limited adapter to minimize the thermal dissipation. See more details on using a current-limited adapter in the ISL6292 datasheet, available at http://www.intersil.com.

Internal Oscillator

The internal oscillator (see the Block Diagram) establishes a timing reference. The oscillation period is programmable with an external timing capacitor, C_{TIME}, as shown in Typical Applications. The oscillator charges the timing capacitor to 1.5V and then discharges it to 0.5V in one period, both with 10μA current. The period T_{OSC} is:

$$T_{OSC} = 0.2 \cdot 10^6 \cdot C_{TIME} \quad \text{(seconds)} \qquad \text{(EQ. 1)}$$

A 1nF capacitor results in a 0.2ms oscillation period.

Total Fast Charge Time

The total fast charge time TIMEOUT is also programmed by the C_{TIME}. A 22-stage binary counter increments each oscillation period to set the TIMEOUT, thus,

$$TIMEOUT = 2^{22} \cdot T_{OSC} = 14 \cdot \frac{C_{TIME}}{1nF} \quad \text{(minutes)} \qquad \text{(EQ. 2)}$$

A 1nF capacitor leads to 14 minutes of TIMEOUT. If a user needs to set the TIMEOUT to 3.5 hours, a 15nF capacitor is required. The charger must reach EOC before the charger terminates, otherwise, a TIMEOUT fault will be issued.

Trickle Charge Time

The trickle charge time is limited to 1/8 of TIMEOUT. If the trickle charge time (t_1 to t_2) exceeds the limit, a TIMEOUT fault will be issued. The end of trickle charger is determined by the battery voltage staying above the trickle charge threshold (given in the Electrical Specification) for 15 consecutive cycles of T_{OSC}; therefore, the minimum time

the charger stays in the trickle mode is 15 cycles. Usually for a recharge cycle, the trickle charge time is 15 cycles (t_6 to t_7 in Figure 20). If the battery voltage falls below the trickle charge threshold during the 15 cycles, the 15-cycle counter is reset (not the total-trickle-charge-time counter) and the charger remains in the trickle mode.

Disabling TIMEOUT Limit

The TOEN pin allows the user to disable the fast charge TIMEOUT limit by pulling the TOEN pin to LOW or shorting it to GND. When this happens, the charger never terminates. The STATUS pin still issues the EOC indication when the EOC condition is reached. The EOC indication is latched and does not change until a new charge cycle starts, initiated by the events listed in Table 1. Leaving the TOEN pin floating is recommended to enable the TIMEOUT. Driving the TOEN pin above 3.0V is not recommended. The trickle charge time limit can never be disabled. For the 3x3 DFN package option, the TOEN pin is left floating internally and, therefore, the TIMEOUT cannot be disabled.

CC Mode Current Programming

The charge current is programmed by the IREF pin. There are three ways to program the charge current:

1. driving the IREF pin above 1.3V
2. driving the IREF pin below 0.4V,
3. or using the R_{IREF} as shown in the Typical Applications.

The voltage of IREF is regulated to a 0.8V reference voltage when not driven by any external source. The charging current during the CC mode is 25,000 times that of the current in the R_{IREF} resistor. Hence, depending on how the IREF pin is used, the charge current is,

$$I_{CHARGE} = \begin{cases} 255mA & V_{IREF} > 1.3V \\ \frac{0.8V}{R_{IREF}} \times 25000(A) & R_{IREF} \\ 100mA & V_{IREF} < 0.4V \end{cases} \quad \text{(EQ. 3)}$$

The internal reference voltage at the IREF pin is capable of sourcing less than 100µA current. When pulling down the IREF pin with a logic circuit, the logic circuit needs to be able to sink at least 100µA current.

The actual charge current may be affected by the thermal foldback function. See the Thermal Foldback section for more details.

Trickle Mode Current

The charge current in the trickle mode is 20% of the programmed CC mode charge current, that is:

$$I_{TRICKLE} = 0.2 \cdot I_{CHARGE} \quad \text{(EQ. 4)}$$

where I_{CHARGE} is the charge current given in EQ. 3.

End-of-Charge (EOC) Current

The EOC current I_{EOC} sets the level at which the charger starts to indicate the end of the charge with the STATUS pin, as shown in Figure 20. The I_{EOC} is set in two ways:

1. By connecting a resistor between the IMIN pin and ground,
2. Or by connecting the IMIN pin to the V2P8 pin.

When programming with the resistor, the I_{EOC} is set in the equation below:

$$I_{EOC} = 2500 \cdot \frac{V_{REF}}{R_{IMIN}} = 2500 \cdot \frac{0.8V}{R_{IMIN}}(A) \quad \text{(EQ. 5)}$$

where R_{IMIN} is the resistor connected between the IMIN pin and the ground, as shown in the Typical Application Circuit. When connected to the V2P8 pin, the I_{EOC} is set to 1/10 of I_{CHARGE} given in EQ. 3, except when the IREF pin is shorted to GND. Under this exception, I_{EOC} is 5mA. For the ISL6298 in the 3x3 DFN package, the IMIN pin is connected internally to the V2P8 pin.

EOC Conditions

The EOC indication is asserted when the following conditions are satisfied simultaneously:

1. The battery voltage is above the recharge threshold, and
2. The charge current is lower than the EOC current.

The two conditions can prevent prematurely indicating EOC due to thermal foldback or other transient events.

Recharge

After a charge cycle is completed, charging is prohibited until the battery voltage drops to a recharge threshold, V_{RECHRG} (see Electrical Specifications). Then a new charge cycle starts at point t_6 and ends at point t_8, as shown in Figure 20. The safety timer is reset at t_6.

2.8V Voltage Regulator

The V2P8 pin is the output of an internal 2.8V linear regulator. The 2.8V is the voltage supply for the internal control circuit and can also be used by external circuits, such as the NTC thermistor circuit. The external load is not recommended to exceed 2mA. The V2P8 pin is recommended to be decoupled with a 1µF ceramic capacitor.

NTC Thermistor Interface

The TEMP pin offers an interface to an external NTC thermistor. This pin has two functions: to monitor the battery ambient temperature or to monitor the insertion of the battery. The ISL6298 assumes that the NTC thermistor is inside the battery pack. The battery and the NTC thermistor are inserted or removed together. Removing the NTC thermistor disables the charger.

Figure 21 shows the implementation of the TEMP pin. The comparator CP1 monitors the existence of the NTC thermistor. When the thermistor is removed, the TEMP pin voltage is

pulled up to the V2P8 pin voltage, higher than the Battery Removal Threshold V_{RMV}, and the charger is disabled.

Comparators CP2 and CP3 form a window comparator and the two transistors, Q1 and Q2, create hysteresis for the two window thresholds respectively. When the TEMP pin voltage is “out of the window,” determined by the V_{TMIN} and V_{TMAX}, the ISL6298 stops charging and indicates a fault condition. When the temperature returns to within the window, the charger re-starts a charge cycle. See the Application Information for more details on the NTC thermistor selection.

Thermal Foldback

Over-heating is always a concern in a linear charger. The maximum power dissipation usually occurs at the beginning of a charge cycle when the battery voltage is at its minimum but the charge current is at its maximum. The charge current thermal foldback function in the ISL6298 frees users from the over-heating concern.

Figure 22 shows the typical charge curves in a charge cycle, using a constant voltage input. Once the internal temperature reaches 100°C, the ISL6298 starts to reduce the charge current to prevent further temperature rise. The power dissipation is directly related to the thermal impedance, which is related to the layout of the printed-circuit board, and the ambient temperature. The dotted lines show the power limit and the current waveforms in two cases that the thermal foldback occurs. The current is reduced and gradually increases to the constant charge current as the battery voltage rises.

Usually the charge current should not drop below the EOC current because of the thermal foldback. For some extreme cases if that does happen, the charger does not indicate end-of-charge unless the battery voltage is already above the recharge threshold.

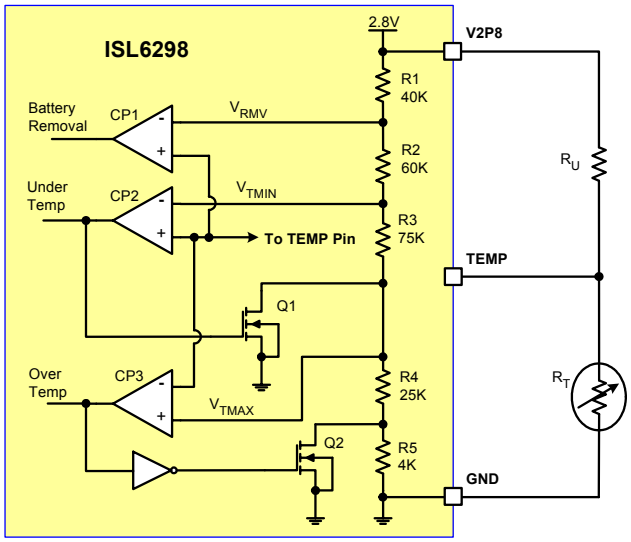


FIGURE 21. THE INTERNAL AND EXTERNAL CIRCUIT FOR THE NTC INTERFACE

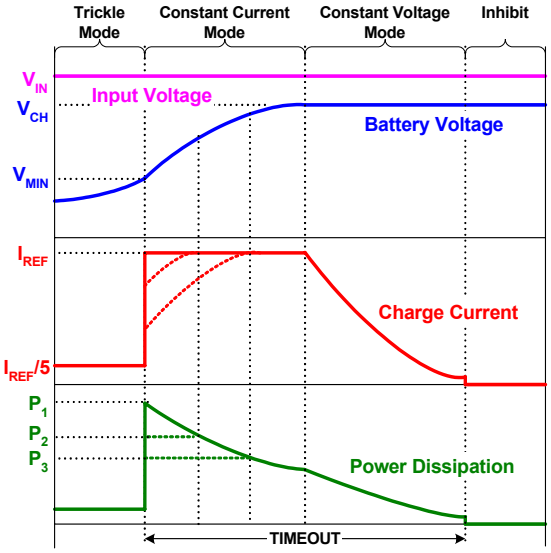


FIGURE 22. TYPICAL CHARGE CURVES USING A CONSTANT-VOLTAGE INPUT

Indications

The ISL6298 has three indications: the input presence, the charge status, and the fault indication. The input presence is indicated by the V2P8 pin while the other two indications are presented by the STATUS pin and FAULT pin respectively.

Figure 23 shows the V2P8 pin voltage vs. the input voltage. The V2P8 pin outputs a 2.8V voltage (blue waveform) when the input voltage (yellow waveform) rises above 3.4V rising POR threshold and falls to zero volt when the input voltage falls below the 2.4V falling POR threshold. The V2P8 pin can be used as a logic signal for the input presence.

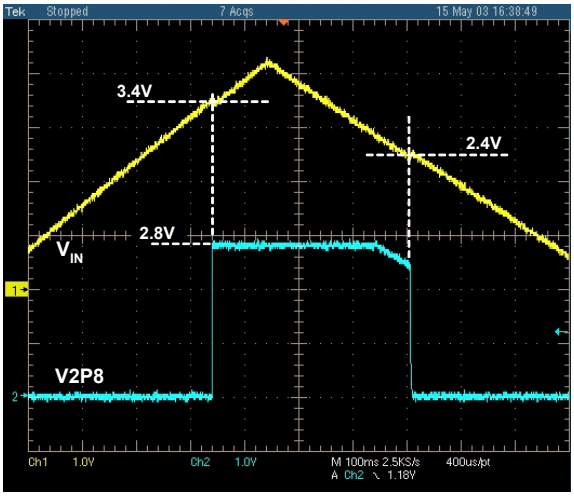


FIGURE 23. THE V2P8 PIN OUTPUT vs THE INPUT VOLTAGE AT THE VIN PIN. VERTICAL: 1V/DIV, HORIZONTAL: 100ms/DIV

Three types of events will result in the FAULT pin to indicate a logic low signal. The following explains the causes and consequences.

1. TEMP pin voltage out of window. This is caused by the ambient temperature being out of the user-set window. When this fault occurs, the charging is halted until the temperature returns within the window.
2. TEMP pin voltage higher than the battery removal threshold. This is caused by the removal of the battery pack. The charger is disabled when the battery is removed and enabled when the battery is re-inserted.
3. TIMEOUT fault during trickle mode or CC mode. The charger is latched when this error occurs. This fault can only be cleared by cycling the input power or the EN input.

The STATUS pin indicates a logic low when a charge cycle starts and indicates a high when the EOC conditions are met. Once the EOC conditions are met, the STATUS signal is latched to high until a new charge cycle.

Both the STATUS and the FAULT pin need be pulled up with external resistors to the 2.8V from the V2P8 pin or the input voltage. Table 2 summarizes the STATUS and FAULT pins.

TABLE 2. INDICATION PINS

FAULT	STATUS	INDICATION
High	High	Charge completed with no fault (Inhibit) or Standby
High	Low	Charging in one of the three modes
Low	High	Fault

*Both outputs are pulled up with external resistors.

Shutdown

The ISL6298 can be shutdown by pulling the EN pin to ground. When shut down, the charger draws typically less than 30μA current from the input power and less than 3μA current from the battery. The 2.8V output at the V2P8 pin is also turned off. The EN pin needs be driven with an open-drain or open-collector logic output, so that the EN pin is floating when the charger is enabled.

Battery Leakage Current

The leakage current from the battery is different when the IC is enabled and disabled. When the IC is disabled, due to removing input power or pulling the EN pin to low, the leakage current is less than 3μA. When the IC is enabled but not charging (due to a fault condition, the battery removal, or after termination), the leakage current is caused mainly by an internal 75kΩ voltage divider for the output voltage feedback. The leakage current is approximately 56μA when the battery voltage is 4.2V.

Applications Information

Capacitor Selection

Typically any type of capacitors can be used for the input and the output. A minimum 1μF ceramic capacitor is recommended to be placed very close to the charger input. Higher value input decoupling capacitance helps the stable operation of the charger.

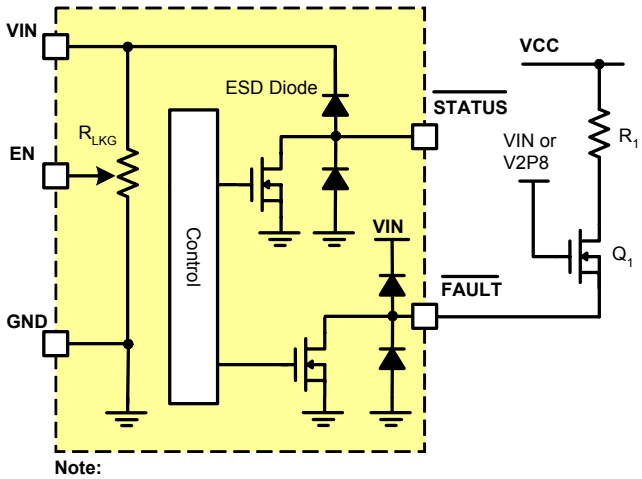
The output capacitor selection is dependent on the availability of the battery during operation. When the battery is attached to the charger, the output capacitor can be any ceramic type with the value higher than 1μF. However, if there is a chance the charger will be used as a linear regulator, a 10μF tantalum capacitor is recommended.

The V2P8 pin supplies power to the internal control circuit as well as external circuits. A good decoupling to this pin is very important to a reliable operation of the charger. It is recommended to use a 1μF ceramic capacitor for this pin.

FAULT and STATUS Pull-Up Resistors

Both FAULT and STATUS pins are open-drain outputs that need an external pull-up resistor. It is recommended that both pins be pulled up to the input voltage or the 2.8V from the V2P8 pin, as shown in the Typical Application Circuits. If the indication pins have to be pulled up to other voltages, the user needs to examine carefully whether or not the ESD diodes will form a leakage current path to the battery when the input power is removed. If the leakage path does exist, an external transistor is required to break the path.

Figure 24 shows the implementation. If the FAULT pin is directly pulled up to the VCC voltage (not shown in Figure 24), a current will flow from the VCC to the FAULT pin, then through the ESD diode to the VIN pin. Any leakage on the VIN pin, caused by an external or internal current path, will result in a current path from VCC to ground.



Note:
R_{LKG} is approximately 240k when EN is floating and is approximately 140k when the EN is grounded.

FIGURE 24. PULL-UP CIRCUIT TO AVOID BATTERY LEAKAGE CURRENT IN THE ESD DIODES.

The N-channel MOSFET Q_1 buffers the FAULT pin. The gate of Q_1 is connected to VIN or the V2P8 pin. When the FAULT pin outputs a logic low signal, Q_1 is turned on and its drain outputs a low signal as well. When FAULT is high impedance, R_1 pulls the Q_1 drain to high. When the input power is removed, the Q_1 gate voltage is also removed, thus the Q_1 drain stays high.

NTC Thermistor Circuit Design

As shown in Figure 21, the thresholds for the NTC circuit are formed by the internal voltage divider. Since the external circuit is also a voltage divider, the accuracy of the bias voltage, that is, the V2P8 pin voltage, becomes not critical. Figure 25 shows the typical values of the thresholds as percentages of the V2P8 pin voltage.

The NTC thermistor resistance is dependent on the ambient temperature. Reducing temperature leads to the increase of the resistance as well as the TEMP pin voltage. When the TEMP pin voltage exceeds 50.3% of the bias voltage, an under-temperature fault is triggered. On the other hand, if the TEMP pin voltage is lower than 12.5%, an over temperature fault occurs. The TEMP pin voltage has to fall back to the 14.5% to 42.9% range for the fault be cleared, as shown in Figure 25.

The ratio, K, of the TEMP pin voltage to the bias voltage is:

$$K = \frac{R_T}{R_T + R_U} \quad \text{(EQ. 6)}$$

Using the ratios at cold and hot temperature limits, as shown in Figure 25, resulting in:

$$\frac{R_{COLD}}{R_{HOT}} = 7.08 \quad \text{(EQ. 7)}$$

and

$$R_U = 1.012 \cdot R_{COLD} \quad \text{(EQ. 8)}$$

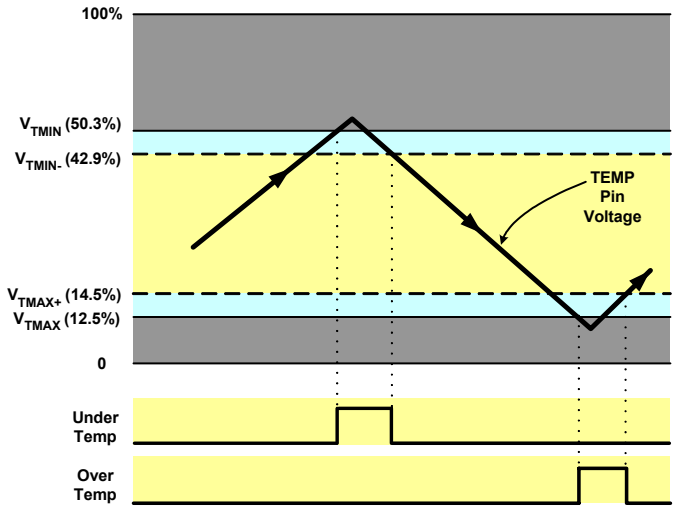


FIGURE 25. CRITICAL VOLTAGE LEVELS FOR TEMP PIN

where R_{COLD} and R_{HOT} are the NTC thermistor resistance values at the cold and hot temperature limits respectively.

It is usually difficult to find an NTC thermistor that has the exact ratio given in EQ. 7. A thermistor with a ratio larger than 7.08, that is:

$$\frac{R_{COLD}}{R_{HOT}} \geq 7.08 \quad \text{(EQ. 9)}$$

can be used in series with a regular resistor to form an effective thermistor that has the right ratio, as shown in Figure 26. With the series resistor R_S, EQ. 7 can be re-written as:

$$\frac{R_S + R_{COLD}}{R_S + R_{HOT}} = 7.08 \quad \text{(EQ. 10)}$$

Once the thermistor and the temperature limits are selected, R_S and R_U can be calculated using

$$R_S = \frac{R_{COLD} - 7.08R_{HOT}}{6.08} \quad \text{(EQ. 11)}$$

and

$$R_U = 1.012 \cdot (R_S + R_{COLD}) \quad \text{(EQ. 12)}$$

To summarize, the NTC thermistor circuit design requires three steps:

1. Find an NTC thermistor that satisfies EQ. 9. The temperature limits are determined by the application requirement.
2. Calculate the series resistance according to EQ. 11.
3. Calculate the pull-up resistance according to EQ. 12.

The following is a design example. The charger is designed to charge the battery with the temperature range from 0°C to 55°C. The 10kΩ NTC thermistor NCP15XH103F03RC from Murata (http://www.murata.com) satisfies EQ. 9. The resistance table is given in Table 3. The typical resistance at

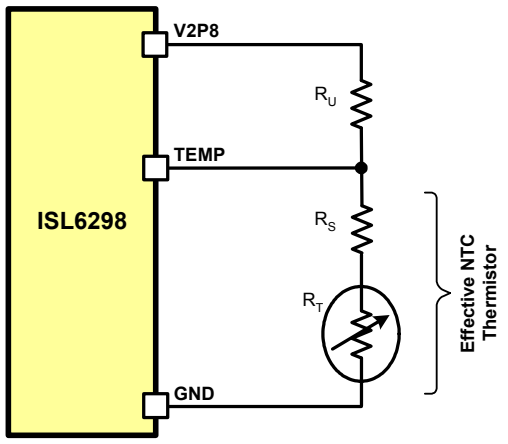


FIGURE 26. EFFECTIVE NTC THERMISTOR CIRCUIT

0°C and 55°C are R_{COLD} = 27.2186kΩ and R_{HOT} = 3.535kΩ respectively. Using EQ. 11 and EQ. 12 result in R_S = 360Ω and R_U = 27.9kΩ.

Hysteresis Temperature Calculation

Using EQ. 6 is re-arranged as:

$$R_T = \frac{K}{1-K} \cdot R_U - R_S \quad \text{(EQ. 13)}$$

Substituting the ratio at the hysteresis threshold results in the NTC thermistor resistance at the threshold. Continuing the example above, the thermistor values are found to be 20.64kΩ and 4.37kΩ respectively at the low and high hysteresis temperatures. The corresponding temperatures are found from the Table 3 to be 7°C and 49°C respectively. In other words, the hysteresis temperatures for the low and high temperature limits are approximately 7°C and 6°C respectively.

Temperature Tolerance Calculation

The temperature accuracy is affected by the accuracy of the thresholds, R_S, R_U, and the NTC thermistor. Using the maximum ratio K, maximum possible R_U, and minimum R_S results in the maximum value of R_T from EQ. 13, that is:

$$R_{T,MAX} = \frac{K_{MAX}}{1-K_{MAX}} \cdot R_{U,MAX} - R_{S,MIN} \quad \text{(EQ. 14)}$$

From the Electrical Specification table, the maximum K is found to be 52.3%. Assuming the resistors have 1% accuracy, the maximum R_U is 28.2kΩ and the minimum R_S is 356Ω. The resultant maximum R_T is then found to be 30.6kΩ and the corresponding temperature is -3°C. Hence the temperature tolerance is 3°C. Similarly, the high temperature maximum thermistor value is 3.98kΩ. Hence, the lowest temperature is 51°C and the tolerance is 4°C.

TABLE 3. RESISTANCE TABLE OF NCP15XH103F03RC

TEMP (°C)	R-Low (kΩ)	R-Center (kΩ)	R-High (kΩ)
-3	30.3641	31.0200	31.6869
0	26.6780	27.2186	27.7675
6	20.7560	21.1230	21.4944
7	19.9227	20.2666	20.6143
50	4.0833	4.1609	4.2395
51	4.9498	4.0262	4.1036
55	3.4634	3.5350	3.6076

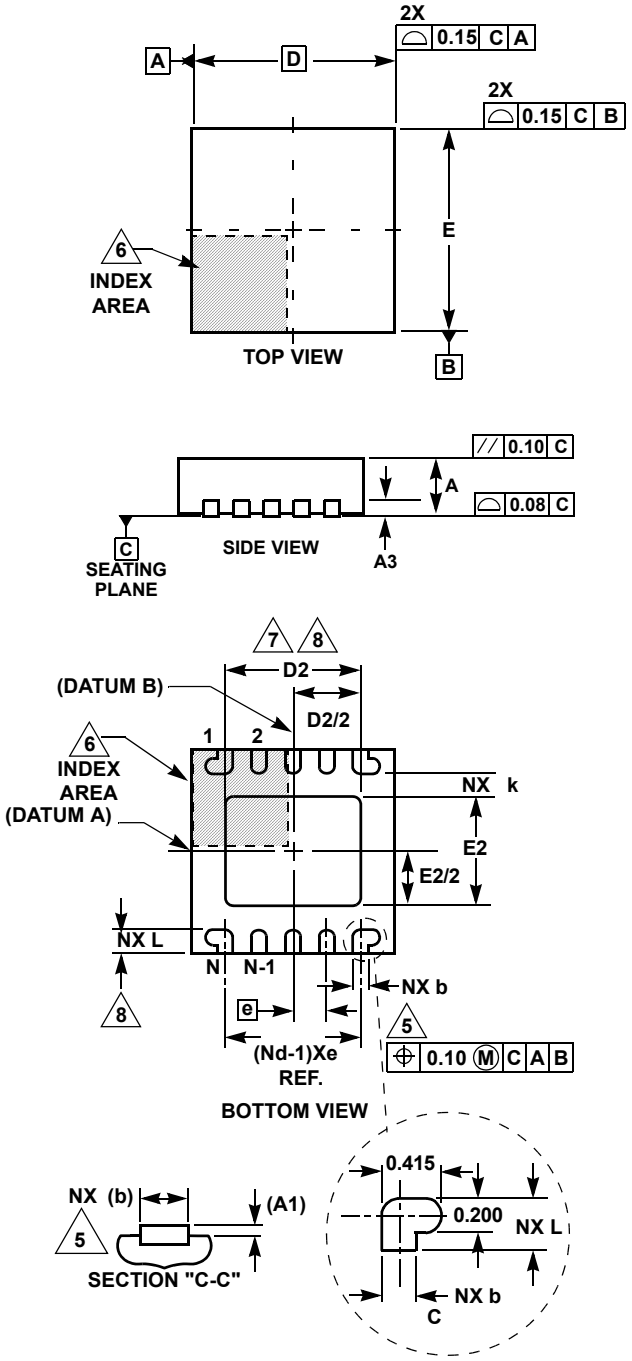
Working with Current-Limited Adapter

The ISL6298 minimizes the thermal dissipation when powered by a current-limited ac adapter. The thermal dissipation can be further reduced when the adapter is properly designed. For more information regarding working with current-limited adapters, please refer to the ISL6292 datasheet available at http://www.intersil.com.

Board Layout Recommendations

The ISL6298 internal thermal foldback function limits the charge current when the internal temperature reaches approximately 100°C. In order to maximize the current capability, it is very important that the exposed pad under the package is properly soldered to the board and is connected to other layers through thermal vias. More thermal vias and more copper attached to the exposed pad usually result in better thermal performance. On the other hand, the number of vias is limited by the size of the pad. The exposed pad for the 4x4 QFN package is able to have 5 vias. The 3x3 DFN package allows 8 vias be placed in two rows. Since the pins on the 3x3 DFN package are on only two sides, as much top layer copper as possible should be connected to the exposed pad to minimize the thermal impedance. Refer to the ISL6298 evaluation boards for layout examples.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

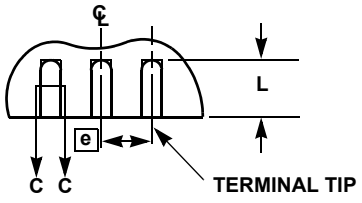
10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

Rev. 3 6/04

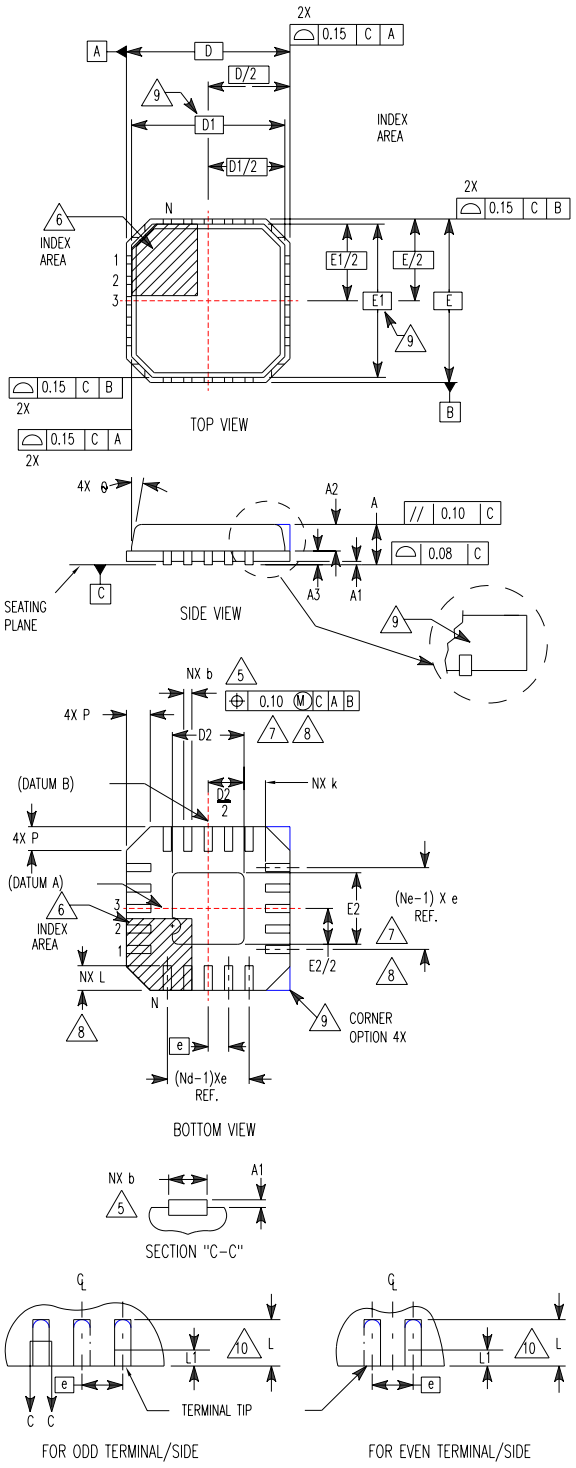
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.