Datasheet May 2002 FN8013.5

CommLink™ Modem Reference Designs

The ISL837030 and ISL83740 Broadband Wireless Modem Reference Designs support a wide range of modulation orders and symbol rates.*

In both Reference Designs, sophisticated coding, equalization, and symbol recovery techniques are employed, resulting in robust wireless link performance.

The ISL837030 and ISL83740 Reference Designs support high-capacity digital microwave radios with data rates up to 238Mbps (ISL83740) and 160Mbps (ISL837030). They provide a flexible, high performance, economical solution for fixed wireless applications.

* Differences between the ISL837030 and ISL83740 are marked in text as needed. Also see **Release Notes on page 25**.

Benefits

- Eliminates the need to develop custom ASICs
- Optimizes wireless link capacity and Bit Error Rate (BER) performance
- Enables rapid prototyping and compliance testing
- Proven technology
- Optional Evaluation Kit supports demo requirements, performance evaluation, and lab testing

Features

- Programmable modulation
  Both: QPSK, 8PSK, 16QAM, 32QAM
  ISL83740 only: 64QAM, 128QAM
- Flexible data rates
  ISL83740: up to 238Mbps
  ISL837030: up to 160Mbps
- Programmable symbol rates
- Reed Solomon (RS) encoding/decoding
- Concatenated coding using RS and PTCM inner code
- FCC and ETSI spectral mask compliance
- Powerful equalization

Includes

- Sample ISL87060MIK Modulator and ISL87060DIK Demodulator Chip Sets for development and test.
- Complete Manufacturing Documentation Package: Bill of Materials, Schematics, PCBA Fabrication Files, including Gerber Files.
- Test Documentation.
- Embedded Monitor and Control Software provides comprehensive setup and test capabilities. Accepts commands in binary or ASCII format.

Optional Evaluation Kit

The modem PCBA is mounted on an Evaluation Platform, allowing the modem to be set up and tested in a standard lab environment. Includes VHF and L-band IF Interfaces and a sophisticated Graphical User Interface for Windows® operating systems. (ISL83700EVAL/ISL83740EVAL)

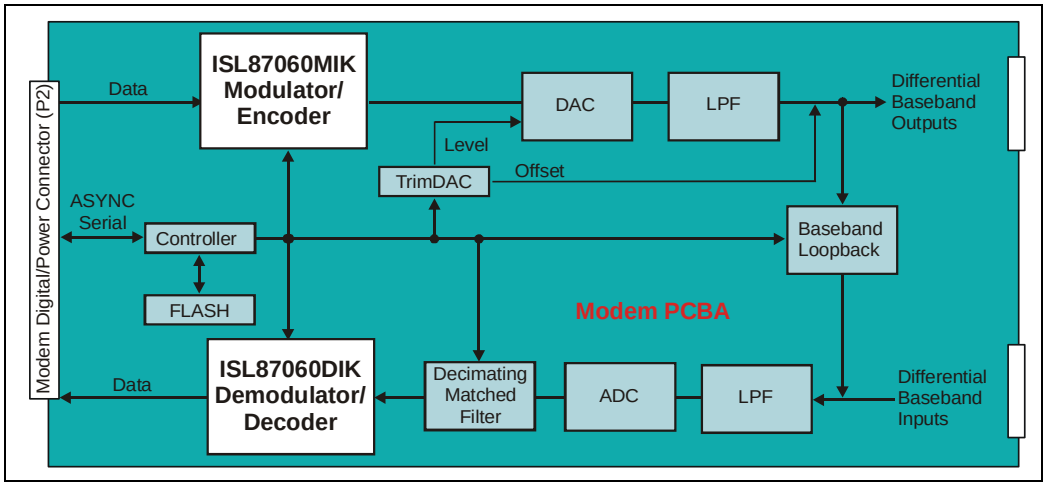

FIGURE 1 Simplified Block Diagram

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Ordering Information

PART NUMBER	DESCRIPTION
ISL83740REF-CD	ISL83740 Reference Design (QPSK, 8PSK, 16QAM, 32QAM, 64QAM, 128QAM)
ISL837030REF-CD	ISL837030 Reference Design (QPSK, 8PSK, 16QAM, 32QAM)
ISL837030KIT-xxx	Kit versions supply sample chips in lots of 24 to 120, in 24-unit increments. Applies to either Reference Design.
ISL83740EVAL	ISL83740 Evaluation Kit (QPSK, 8PSK, 16QAM, 32QAM, 64QAM, 128QAM)
ISL83700EVAL	ISL837030 Evaluation Kit (QPSK, 8PSK, 16QAM, 32QAM)
ISL87060MIK	Modulator Chip
ISL87060DIK	Demodulator Chip

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Functional Description

Intersil's broadband wireless modem devices are fully integrated and support a wide range of modulation orders and symbol rates. Sophisticated coding, equalization, and symbol recovery techniques are employed to enable robust wireless link performance.

The complete modem Printed Circuit Board Assemblies (PCBAs) with standard hardware and software interfaces enable equipment manufacturers to rapidly integrate Intersil modem functionality into their system products.

The ISL837030 and ISL83740 Modem Reference Designs provide a flexible, high performance, economical solution for fixed wireless applications. The modem design provides an off-the-shelf solution for users interested in easily integrating a complete modem into their products.

The modem PCBA architecture implements a complete baseband transmit and receive function:

1. **Modulator Function**
   Converts byte-wide parallel data, encodes and digitizes it, and generates a differential baseband analog signal. This signal can then be up-converted to any IF/RF frequency the user requires.
2. **Demodulator Function**
   Accepts a differential analog baseband signal. Filters, decodes, corrects, and converts it to byte-wide digital data and clock.
3. **Controller**
   Incorporates everything necessary to control and monitor the modem.

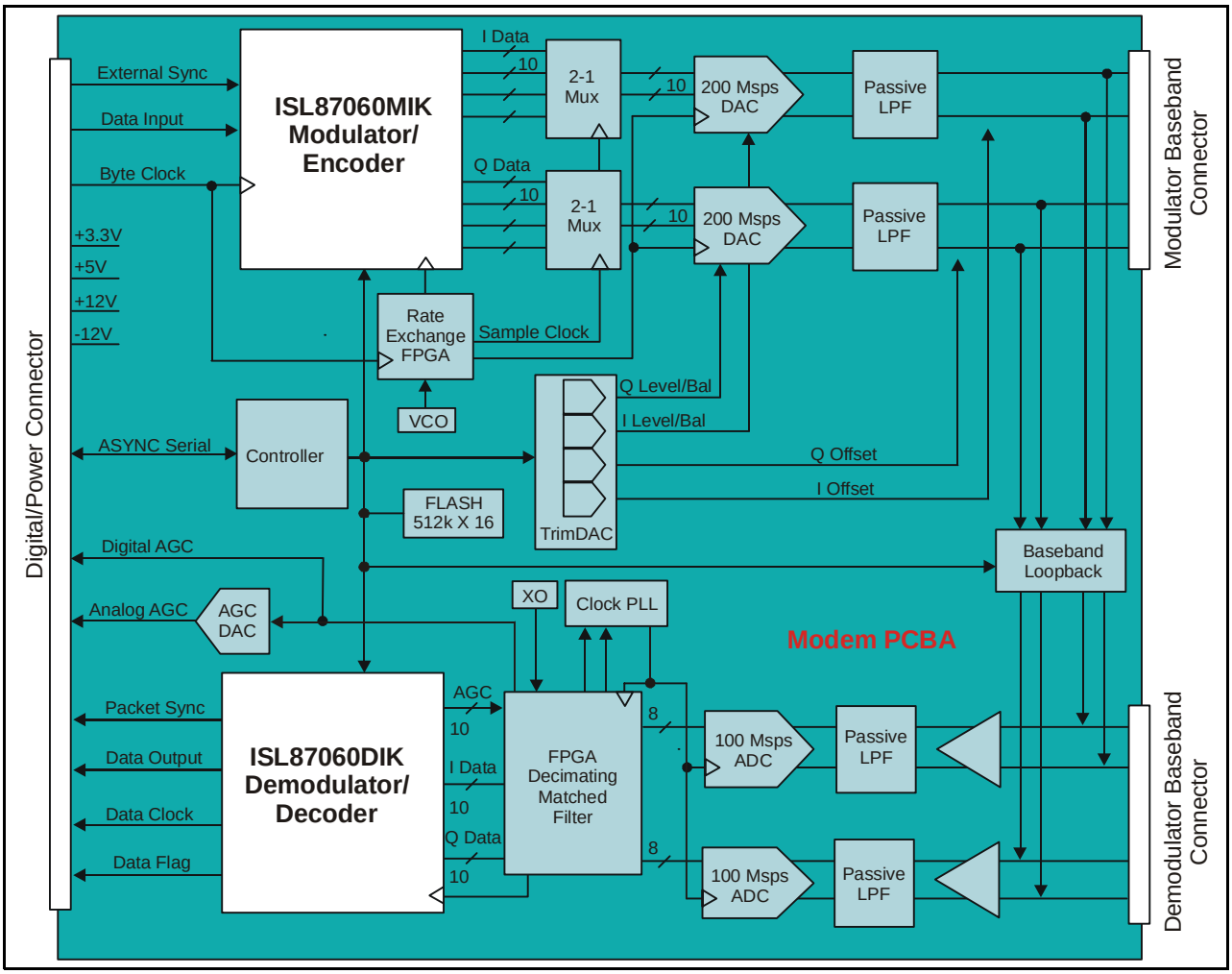


FIGURE 2 Functional Block Diagram

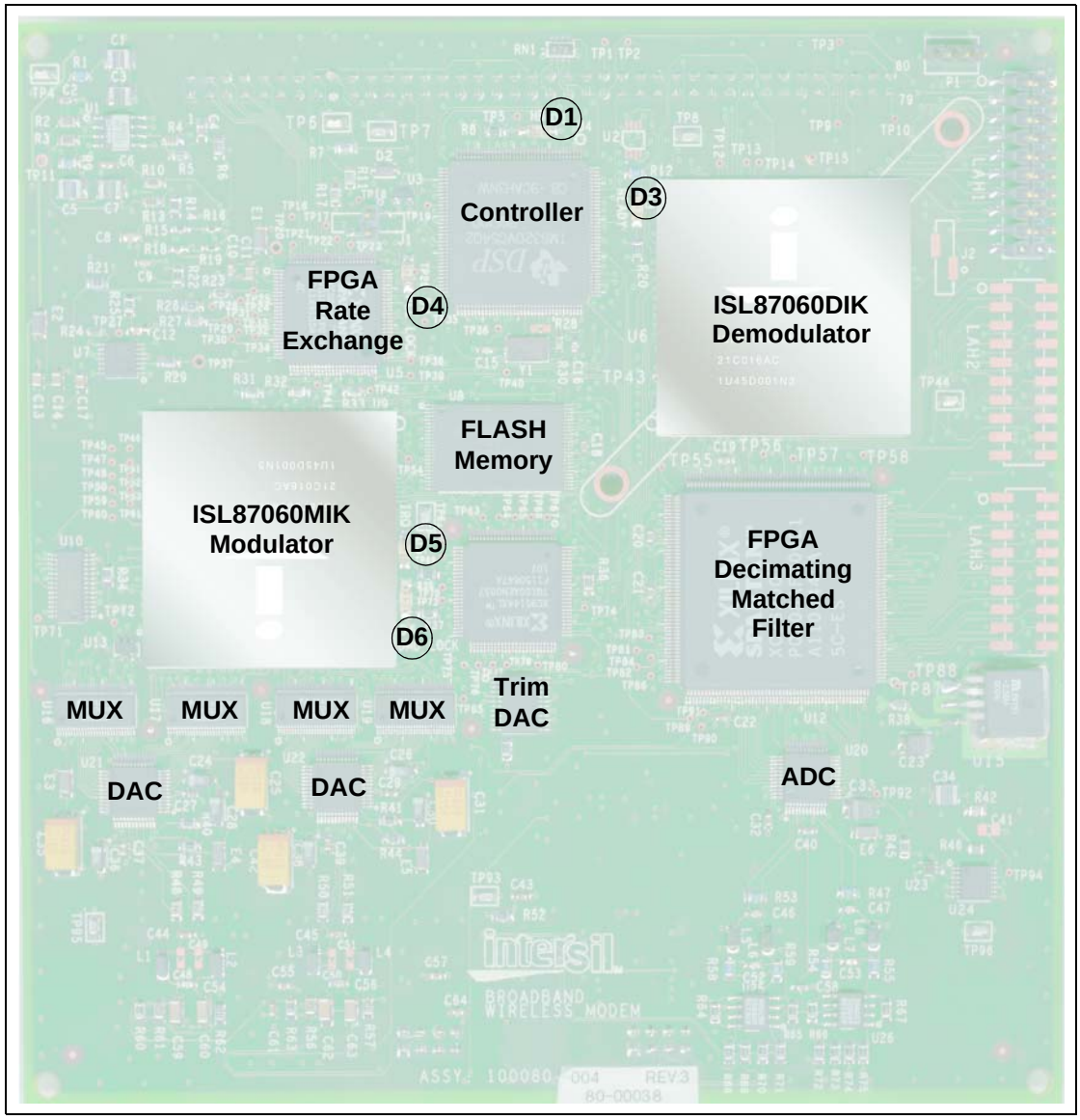


FIGURE 3 Modem Printed Circuit Board Assembly (PCBA)

LED INDICATORS	LIGHT INDICATORS
D1 Controller Status	Blinking indicates controller is functional. Solid off or on indicates not functional.
D3 Modem Ready	Light on indicates modem is ready to accept user commands. Equivalent to the `MODEM_RDY` signal on the interface connector.
D4 PLL Lock Detect	Light on indicates that the modulator rate exchange has successfully locked to the interface input byte clock.
D5 Alarm IRQ	Light on signals active alarm condition. Equivalent to the `IRQ` signal on the interface connector.
D6 Demod Lock	Light on indicates that the demodulator has successfully locked to the input baseband signal.

Modulator Functions

The modulator accepts byte-wide parallel data, encodes it, digitizes it, and produces a balanced analog signal output. This signal can then be up-converted to whatever RF/IF frequency the application requires. It consists of four functions:

1. ISL87060MIK Modulator ASSP

The modulator ASSP provides a digital representation of a modulated analog signal. The chip accepts byte-wide TTL data and applies:

- Energy Dispersal
- Reed-Solomon Forward Error Correction (FEC)
- Convolutional Interleaving
- Symbol Generation for various modulation formats with or without Convolutional Coding
- Pulse Shaping
- Tuning

The digital output from the ASSP consists of eight 10-bit ports, four for I and four for Q. Each port represents at least one of four samples per symbol which requires multiplexing before it is applied to the Digital to Analog Converter (DAC).

2. Digital to Analog Converter (DAC)

The DAC section muxes each of the four 10-bit ports and converts them into an analog signal representation of the digital values produced by the ASSP. The DAC samples at a minimum of four samples per symbol based on the ASSP's Interpolator setting.

TrimDACs, controlled by the processor, provide fine adjustment of the amplitude and DC offset of the I and Q output signals. Two of the TrimDACs control the reference voltage used by the output DACs, thereby adjusting the output signal amplitude. The default setting corresponds to a zero adjustment.

3. Low Pass Filter (LPF)

The analog signal from the DAC is then filtered to eliminate undesired digitizing effects. The TrimDAC is used to control the offset voltage of the output signal, allowing the user to adjust the balance between the I and Q baseband output signals for upconverter optimization.

4. Rate Exchange

The Rate Exchange function generates clocks by converting the byte-wide interface clock to an ASSP processing clock. It then provides the sample clocks to the DAC and Mux sections. The relationship between the byte clock input and the other clocks varies dramatically depending on the FEC and Interpolator settings within the ASSP.

Demodulator Functions

The demodulator accepts differential analog baseband I and Q signals, then filters, decodes, corrects, and converts them to byte-wide digital data and clock. It consists of six functions:

1. Low Pass Filter (LPF)

The LPF eliminates any undesired baseband high frequency artifacts caused by the down conversion process.

2. ADC

The Analog to Digital Converter (ADC) provides a digital representation of the modulated baseband analog signal. It provides eight bits of data for each of the I and Q channels.

3. FPGA Decimating Filter

A Field Programmable Gate Array (FPGA) based Decimating Matched Filter is provided for additional filtering based on the desired symbol rate. Multiple FPGA designs are required to cover the full symbol range. They are stored in the processor's FLASH memory and loaded as required, based on configuration parameters. The modem automatically toggles between the FPGA designs depending on the baud rate.

4. ISL87060DIK Demodulator ASSP

The demodulator ASSP accepts quantized baseband I and Q signals and provides all necessary demodulation functions including:

- Carrier and Symbol Acquisition and Tracking
- Adaptive Equalization
- Data Estimation
- Convolutional Deinterleaving
- Energy Dispersal Removal
- Decoding Functions, including Reed-Solomon decoding

5. Baseband Loopback

The modulator baseband output can be configured to be connected to the input of the demodulator. This allows in-system functional verification of the modem. The loop-back circuit is implemented with a fully differential buffered/switch circuit. When engaged, the loop-back signals are summed with the normal I and Q input signals to the demodulator. This configuration does not require that either the normal modulator I/Q outputs or the normal demodulator I/Q inputs be disconnected. Operation is transparent to the normal loading on these interfaces.

The loop-back signals are summed with the normal input signals. Therefore, when loopback is enabled the system must be set to minimize the signal input from the normal demodulator I/Q input path.

Demodulator (Continued)

6. Automatic Gain Control (AGC)

The demodulator ASSP provides a parallel data word to be used by the AGC to optimize the dynamic range of the input signal to the demodulator. The ASSP averages the magnitude of the input baseband signal, subtracts that from a target value, and accumulates the results. The AGC value is available in either serial digital or analog form. The AGC value output is proportional to the amount by which the incoming signal's amplitude must be increased in order for its level to reach the desired target. Therefore, an increase in the AGC value indicates that the signal level at the input to the AGC amplifier/attenuator has actually decreased. The modem operates in two different AGC modes:

- Open loop is used when there is no external AGC loop implemented.
- Closed loop is used when the modem's AGC features are to be used.

For best performance, closed loop mode is suggested. This automatically sets the demodulator input level to the optimum value. The system default is open loop mode until any AGC parameter is initialized from the host.

The Controller

The Controller is a highly integrated device used to eliminate the complexities of interfacing with the Intersil ASSPs directly. It incorporates everything necessary to control and monitor the modem.

The Controller's processor takes high-level commands from the user and determines what is required to configure and monitor the ASSPs. This relieves the user from any real-time interfacing and algorithm implementation issues.

The executable firmware is held in FLASH memory that is in-circuit upgradeable. This allows the user to upgrade the code or load in a new algorithm as required via the asynchronous serial port (the Monitor and Control port).

Monitor and Control Software

The modem PCBA is configured and monitored using Intersil's embedded Monitor and Control (M&C) software. This software is used to set parameters such as:

- modulation type
- code rate
- payload rate
- symbol rate
- output level/offset
- AGC control
- diagnostics
  - self-test
  - loopback
- alarms
- baseband loopback
- Alpha (pulse shape)
- statistics
  - BER
  - EVM
  - demodulator stress
  - phase & amplitude imbalance
- and more

For details, see the Programmer's Reference AN9935.

Performance Specifications

Modem Parameters

ITEM	DESCRIPTION
Symbol Rate Range	3.0Mbaud to 42.514Mbaud
Payload Data Rate Range	5.6Mbps to 238Mbps (ISL83740) 5.6Mbps to 160Mbps (ISL837030)
Outer Code (Reed Solomon) Packet Size	(255, 238) Internal Sync Mode only (240, 223) External Sync Mode only See **Demodulator RS Data Packet Definition on page 20**.
Power Consumption	18.75W Maximum
FEC Modes	FEC disabled, RS FEC only, concatenated convolutional inner code with RS outer code
Pulse Shape (Alpha)	Square Root Nyquist, programmable α (0.15 to 0.35) in 0.05 steps
Tx Carrier Tuning Range	$\pm$ 500kHz, programmable in 1kHz steps Non-zero tuner offsets may not meet more stringent mask requirements.
Rx Digital Matched Filter	32-tap Root Raised Cosine 0.20 rolloff factor Bandwidth tracks selected symbol rate

Modulation, Inner Code Rates, and Ranges

MODULATION TYPE		INNER CODE RATE[1]		PAYLOAD RATE RANGE IN Mbps[2]		SYMBOL RATE RANGE IN Mbaud	
ASCII	BINARY	ASCII	BINARY	ISL83740	ISL837030	ISL83740	ISL837030
QPSK	0	1	12	5.6000 to 79.3595	5.6000 to 79.3595	All Payload Rates: 3.0000 to 42.5140	3.0000 to 42.5140
8PSK	1	1	12	8.4000 to 119.0392	8.4000 to 119.0392		
16QAM	2	3/4	2	8.4000 to 119.0392	8.4000 to 119.0392		
		7/8	6	9.8000 to 138.8791	9.8000 to 138.8791		
		1	12	11.2000 to 158.7189	11.2000 to 158.7189		
32QAM	4	4/5	3	11.2000 to 158.7189	11.2000 to 158.7189		
		9/10	8	12.6000 to 178.5588	12.6000 to 160.0000		3.0000 to 38.0953
		1	12	14.0000 to 198.3987	14.0000 to 160.0000		3.0000 to 34.2857
64QAM	6	5/6	4	14.0000 to 198.3987	N/A		N/A
		11/12	9	15.4000 to 218.2385			
		1	12	16.8000 to 238.0784			
128QAM	8	6/7	5	16.8000 to 238.0784			

[1] A rate of 1 is equivalent to No Inner Code.
[2] Ranges valid for Internal Sync (RS 255, 238).

To avoid significant performance degradation, interleaving must be enabled when using concatenated coding rates (any rate other than 1). See the mdLeaver command in the Programmer's Reference AN9935.

Modulator Performance Specifications

ITEM	DESCRIPTION	
Baseband Amplitude Imbalance	< 0.1dB after initial trim, over temperature and life < 0.2dB typical without trim	
Spectral flatness (relative to ideal RRC spectrum)	+0.1dB, -0.5dB	
Baseband Phase Imbalance	< 0.5°, over temperature and life	
I/Q Average Group Delay Imbalance	0.3ns maximum	
Residual Output Voltage Noise Floor (>100MHz)	Less than -110dBmV/Hz rms differential	
I/Q Anti-alias Filter Low Pass Response	3-pole, -3dB at 32.0MHz	
I/Q AC Coupling High Pass Response	1-pole, -3dB at 75Hz	
Tx Symbol Timing Jitter (1kHz to baud/2)	1.0° rms, referred to symbol period	
Spurious Components (below 140MHz)	DAC Aliasing Component (15Mbaud to 17.5Mbaud, 29.75Mbaud to 35Mbaud)	-55dBc or better
	DAC Aliasing Component (other baud rates)	-65dBc or better
	Miscellaneous Spurious Components	
Spurious Outputs (above 140MHz)	Less than -80dBc	

Modulator Input Requirements

ITEM	DESCRIPTION
Input Data Byte Clock Phase Noise EVM and BER may be degraded if this parameter is exceeded.	$< (2.0 \times \frac{F_{BYTE}}{F_{BAUD}})^{\circ}$ rms, when integrated from 300Hz to $\frac{F_{BYTE}}{2}$ When integrated over an offset bandwidth of 500Hz to half the byte rate frequency, then scaled proportionally to the symbol rate frequency.

Modulator Output Electrical Specifications

ITEM	DESCRIPTION
Output Signal Type	Fully balanced differential, AC Coupled
Baseband Output Level into recommended load[1]	Nominal: 1.9V p-p. Maximum: 2.2V p-p
Baseband Output Adjust/Resolution[1]	Programmable -4dB to +1.5dB, in approximately 0.04dB steps.
Baseband Offset Trim[1]	Programmable ± 31mV in 0.244mV steps into 1.2kΩ load at +2.5V bias (Offset adjustment of 0VDC to +5VDC through 95kΩ connected to output). For details, see the Programmer's Reference AN9935.
Load Impedance (Required)	1.20kΩ ± 20%, < 20pF, each leg to ground
The modulator pulse shaping, interpolation, and analog anti-alias filtering have been designed to meet the requirements of applicable FCC, IC, ITU, and ETSI standard spectral masks.	Applicable Standards: FCC 47CFR 101.111; ETSI EN 300-197, 198, 430, and 431; ETSI EN 301-128.

[1] Output levels are not guaranteed when using the modulator tuner.

Demodulator Input Requirements

ITEM	DESCRIPTION
Symbol Frequency Error	± 200 ppm of symbol rate
Spectral Slope Error	Up to ± 2dB average tilt across passband
Average I/Q Group Delay Imbalance	< 6% of symbol period, up to 40Mbaud < 1.5ns for 40Mbaud to 42.5Mbaud
I/Q Group Delay Response Flatness (p-p delay variation across 3dB spectrum)	
Carrier Leakage Component	-30dBc or better for QPSK, 8PSK, 16QAM -35dBc or better for 32QAM, 64QAM, 128QAM (64QAM and 128QAM available in ISL83740 only)
Baseband Source Amplitude Error	< 1.0dB maximum
Baseband Source Phase Imbalance	< 5° maximum

Demodulator Input Electrical Specifications

ITEM	DESCRIPTION
Input Signal Type	Balanced differential, DC Coupled
Input Impedance	Balanced: 1.00kΩ differential Unbalanced: 1.00kΩ In unbalanced mode, source impedances of both legs should be approximately equal to avoid DC offset at the ADCs. Matched source impedances of < 100Ω are recommended.
Baseband Input Level	1.00V p-p for full scale at ADC
Baseband Input Bias	Current: Source outputs must sink 0.4mA for 0.00VDC input source, each leg Offset: < 10µA
Open Circuit Input Bias Voltage	600mVDC (baseband loopback off)
Input Overload Level	Approximately 2.5V p-p

Demodulator Performance Specifications

ITEM	DESCRIPTION
Rx Carrier Tracking Range[1]	± 400kHz
Rx Carrier Acquisition Range[1]	Programmable from 50kHz to 400kHz in increments of 1kHz. For details, see the Programmer's Reference AN9935.

[1]The maximum Acquisition and Tracking Rate Range is less than 400kHz when the baud rate is less than 6.6Mbaud, as shown in FIGURE 4.

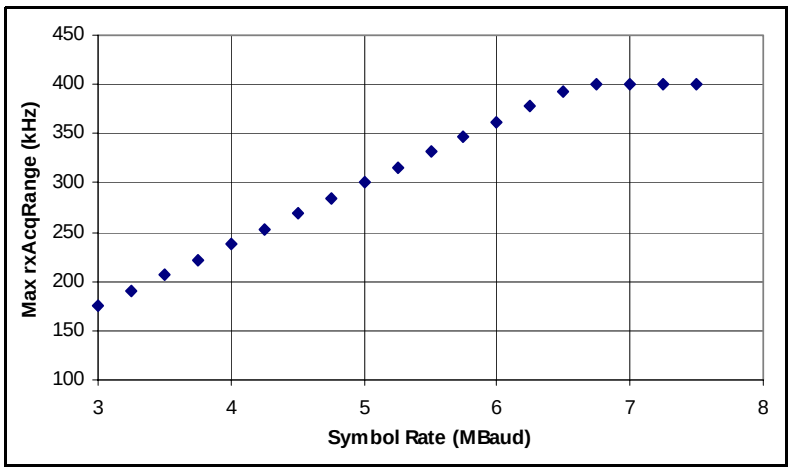


FIGURE 4 Acquisition/Tracking Range at Low Baud Rates

BER Performance (Typical)

PARAMETERS				
BER	MODULATION TYPE	INNER CODE RATE	Eb/No	CONDITIONS
1.0E-8 BER	QPSK	1	8.1dB	• Standard setup using low-cost VHF IF interface loopback[1]
	8PSK,	1	11.6dB	
	16QAM	1	12.2dB	
	32QAM	1	14.8dB	
	64QAM	1	18.7dB	
1.0E-10 BER	16QAM	3/4	7.8dB	
		7/8	9.0dB	
	32QAM	4/5	9.7dB	
		9/10	11.4dB	
	64QAM	5/6	12.7dB	
		11/12	15.0dB	
	128QAM	6/7	17.2dB	
Residual BER, FEC disabled	32QAM	1	BER < 1.0E-11	• Standard setup using low-cost VHF IF interface loopback[1] • No added noise
			0	• Baseband loopback, no noise

64QAM and 128QAM available in ISL83740 only.

[1] Performance is based on a standard setup using the Evaluation Platform's VHF interface under typical operating conditions at baud rates > 10Mbaud as defined in **Demodulator Input Requirements on page 9**. All loop bandwidths are set by default to accommodate severe multipath distortions. Performance can be increased significantly by adjusting loop bandwidths for a less severe environment. Performance is 0.5dB to 1dB better when using the Evaluation Platform's high performance L-band interface.

Controller Parameters

ITEM	DESCRIPTION
Monitor and Control (M&C) Port	• TTL Level UART, RXD, TXD only, no handshake • 115.2kBaud • 8 bits • No Parity • 1 Stop Bit
FPGA Configuration Update	• Can be performed via M&C port • Independent of Application Code Update • Cannot be done during modem operation • On-board FLASH memory holds up to four Decimating Matched Filter configurations
Application Code Update	• Can be performed via M&C port • Independent of FPGA Configuration Update • Cannot be done during modem operation • Boot-loader write protected to ensure unconditional recovery.
Reset Time from Power Up	• 8 seconds

Environmental & Physical Specifications

Reliability

MTBF 457,000 hours (52 years) per Bellcore Standard TR-332

Power Supply Requirements

VOLTAGE	CURRENT
+5VDC ± 5%	100mA
+3.3VDC ± 5%	5A
-8.75VDC to -12VDC	100mA
+8.75VDC to +12VDC	100mA

Temperature and Humidity Tolerances

ENVIRONMENT	OPERATING	STORAGE
Temperature	-40°C to 85°C	-50°C to 150°C
Humidity (non-condensing)	<95% Operating humidity tolerance can be increased by conformal coating.	99%

Board Size and Weight

(Excluding connectors)

Length and Width	6” X 6”
Height on Top	0.3” plus heatsink
Height on Bottom	0.11”
Weight	5 oz.

Demodulator ASSP Airflow Requirements

AAVID HEATSINK	HEATSINK HEIGHT	FOR 85°C OPERATION (4.3°C/W REQUIRED)	FOR 70°C OPERATION (6.1°C/W REQUIRED)	UNIT
372024	1.100”	≥ 125	0	linear feet per minute
371924[1]	0.550”	≥ 265	≥ 165	
372824	0.230”	≥ 400	≥ 300	

[1] Included in ISL83740EVAL/ISL83700EVAL Evaluation Platform configurations.

Physical Interface Definition

The following figure highlights the board connectors:

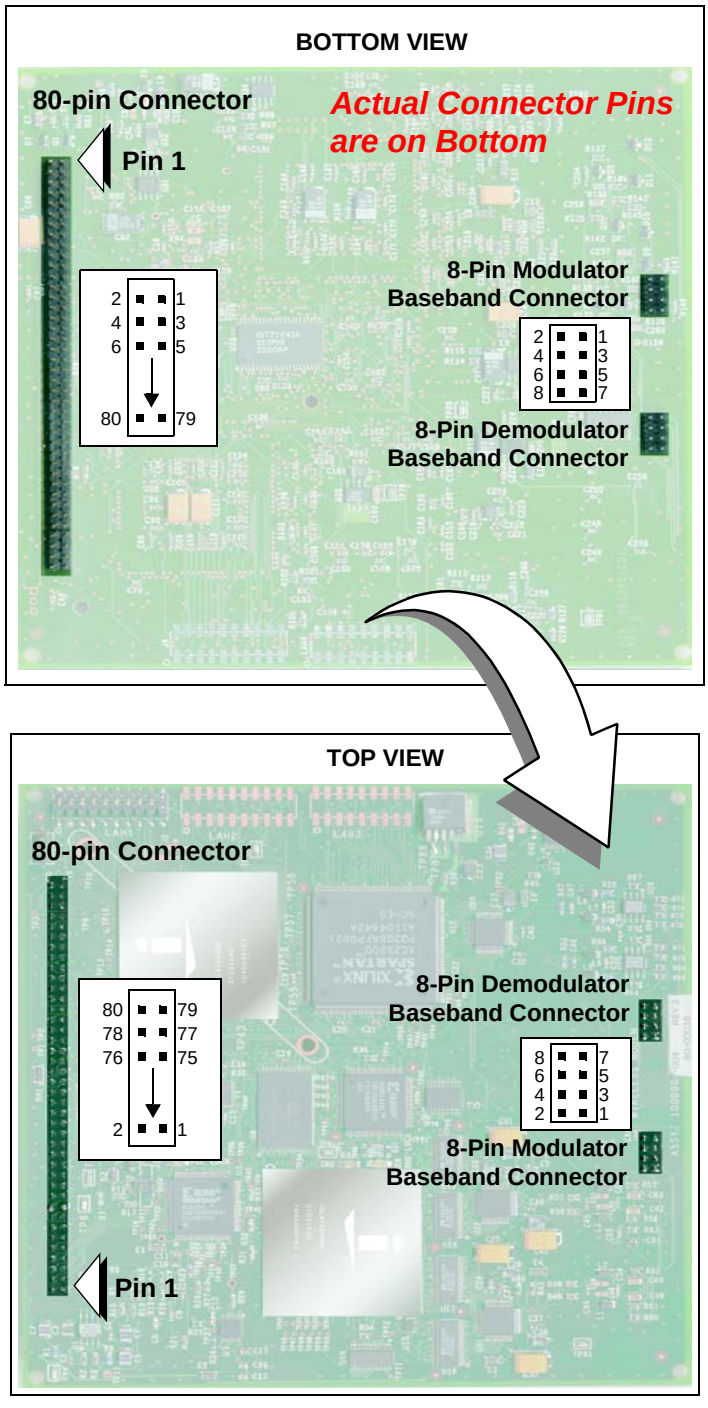


FIGURE 5 Modem PCBA Connectors

80-Pin Digital/Power Connector

Modem Connector Part #: Samtec TSW-140-07-T-D
Suggested Mating Connector: SAMTEC SSW-140-22-T-D

The following figure shows the pin configuration for the 80-pin digital/power connector. For additional details, see the following pages.

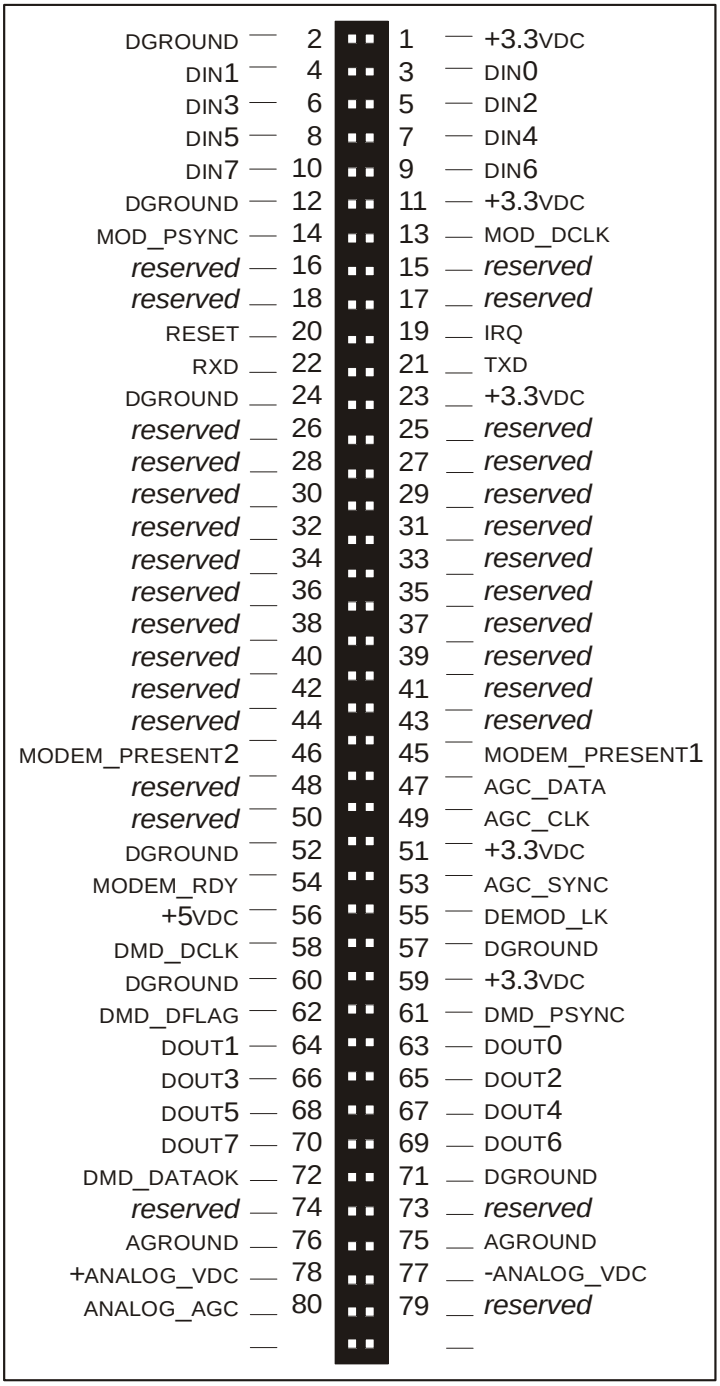


FIGURE 6 Digital/Power Connector Pin Configuration

Power Supply Signals

PIN(S)	SIGNAL NAME	DESCRIPTION	CHARACTERISTIC
78	+ANALOG_VDC	Positive Analog Voltage	+8.75VDC to +12VDC
77	-ANALOG_VDC	Negative Analog Voltage	-8.75VDC to -12VDC
1 11 23 51 59	+3.3VDC	Digital Voltage	± 5%
56	+5VDC		
75 76	AGROUND	Analog Ground	
2 12 24 52 57 60 71	DGROUND	Digital Ground	

M&C Port Signals

PIN(S)	SIGNAL NAME	DESCRIPTION	CHARACTERISTIC
22	RXD	Status data from modem (output)	TTL V_{OH} = 2.4V minimum V_{OL} = 0.6V maximum
21	TXD	Control data to modem (input)	TTL V_{IH} = 2.3V minimum V_{IL} = 0.8V maximum

Modulator Data Interface Signals

PIN(S)	SIGNAL NAME	DESCRIPTION	CHARACTERISTIC
3	DIN0	Data input LSB	TTL V_{IH} = 2.3V minimum V_{IL} = 0.8V maximum
4	DIN1	Data Input	
5	DIN2		
6	DIN3		
7	DIN4		
8	DIN5		
9	DIN6		
10	DIN7	Data input MSB	
13	MOD_DCLK	Byte rate input clock. Data sampled on rising edge.	
14	MOD_PSYNC	When in external sync byte mode, active high flag indicates sync byte location in input transport stream. When not used leave open or tie low.	

Demodulator Data Interface Signals

PIN(S)	SIGNAL NAME	DESCRIPTION	CHARACTERISTIC
63	DOUT0	Data output LSB	TTL $V_{OH} \geq 2.4V$ minimum $V_{OL} \leq 0.4V$ maximum
64	DOUT1	Data Output	
65	DOUT2		
66	DOUT3		
67	DOUT4		
68	DOUT5		
69	DOUT6		
70	DOUT7	Data output MSB	
61	DMD_PSYNC	Active high signal indicates sync byte is available on bus.	
62	DMD_DFLAG	Active high signal indicates valid data is available on bus. Low indicates Reed Solomon Parity or sync byte is on bus.	
58	DMD_DCLK	Byte output clock. Data transitions on falling edge. This clock is ASSP Process Clock gated when valid data is output from the ASSP. Valid data includes sync and parity bytes.	
72	DMD_DATAOK	Active high signal indicates presence of RS-correctable packet. Indicates the current output packet contains no errors.	
80	ANALOG_AGC	A voltage representative of the digital value calculated by the ASSP. The ASSP averages the magnitude of the input baseband signal, subtracts that from a target value, and accumulates the results.	Range: 0VDC to 3.0VDC Impedance: 100Ω Current: ± 3mA maximum Update Rate: approximately every 2,000 symbols
49	AGC_CLK	Serial clock output. Data transitions on rising edge, should be stored on the falling edge.	TTL $V_{OH} \geq 2.4V$ minimum $V_{OL} \leq 0.4V$ maximum
53	AGC_SYNC	Active low signal used to bound valid data out.	
47	AGC_DATA	Serial data, 12 bits AGC, 4 bits padding. Data transitions on rising edge of AGC_CLK. See AGC Timing on page 21.	

Miscellaneous Signals

PIN(S)	SIGNAL NAME	DESCRIPTION	CHARACTERISTIC
20	RESET	Active low hard reset. Resets processor and ASSPs to their initial conditions. This signal is extended by 350ms by a device used to monitor VCC and the state of the reset signal.	Open Drain $V_{IH} \geq 2.0V$ minimum $V_{IL} \leq 0.8V$ maximum 5k pullup to 3.3V on modem
19	IRQ	Active low interrupt request indicates modem requires attention. When enabled this signal asserts, indicating that a fault condition exists on the modem.	TTL $V_{OH} \geq 2.4V$ minimum $V_{OL} \leq 0.4V$ maximum
55	DEMOD_LK	Demodulator lock indicator. low = lock	
54	MODEM_RDY	Active high indicates modem is Ready. Indicates modem is available after power up or reset. Typical time is less than 8 seconds after valid 3.3V or RESET.	
45 OR 46	MODEM_PRESENT1 MODEM_PRESENT2	4.7k pullup to 3.3V **Use either 45 or 46; do not tie together.**	Can be used for modem presence detect.

Reserved

PIN(S)	DESCRIPTION
15-18 25-44 48 50 73-74 79	Leave all unused pins unconnected. Some are used for test and some are reserved for future expansion.

8-Pin Baseband Connectors

Modem Connector Part Number: Samtec TSW-104-07-T-D

Modulator Analog Baseband Connector

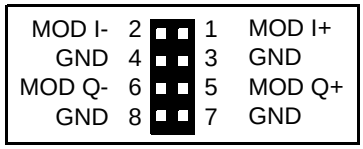


FIGURE 7 Modulator Connector Pin Configuration

PIN(S)	SIGNAL NAME	DESCRIPTION	CHARACTERISTIC
1	MOD I+	I Baseband Analog Output	1.9V p-p differential with 1.2kΩ, < 20pF load
2	MOD I-		
5	MOD Q+	Q Baseband Analog Output	
6	MOD Q-		
3 4 7 8	GND	Ground	

Demodulator Analog Baseband Connector

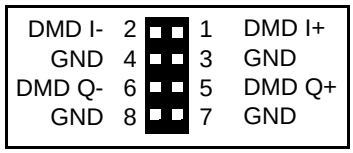


FIGURE 8 Demodulator Connector Pin Configuration

PIN(S)	SIGNAL NAME	DESCRIPTION	CHARACTERISTIC
1	DMD I+	I Baseband Analog Input	1.0V p-p nominal 1.0kΩ, < 25pF load
2	DMD I-		
5	DMD Q+	Q Baseband Analog Input	
6	DMD Q-		
3 4 7 8	GND	Ground	

Data Timing and Packet Definition

Modulator Data Input Timing

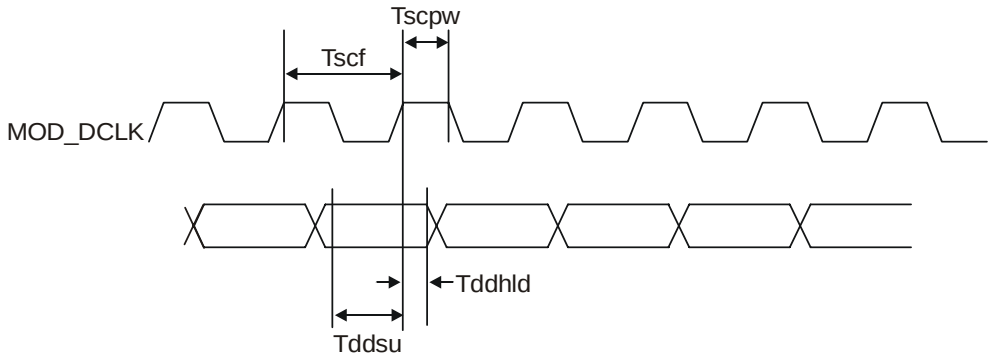
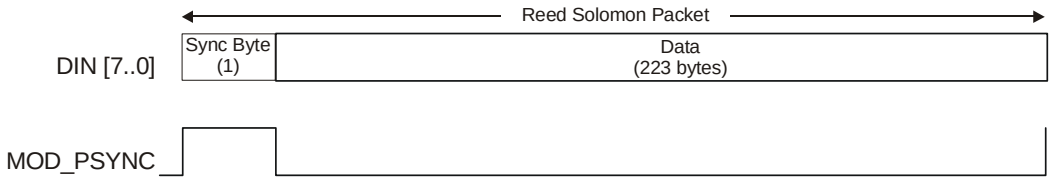


FIGURE 9 Modulator Data Input Timing

SYMBOL	DESCRIPTION	MIN	UNITS
Tscf	Shift_Clk Clock Period	50.0	nsec
Tscpw	Shift_Clk Pulse Width	8.0	
Tddsu	Data Setup Time	12.0	
Tddhld	Data Hold Time	1.0	

Modulator Packet Definition

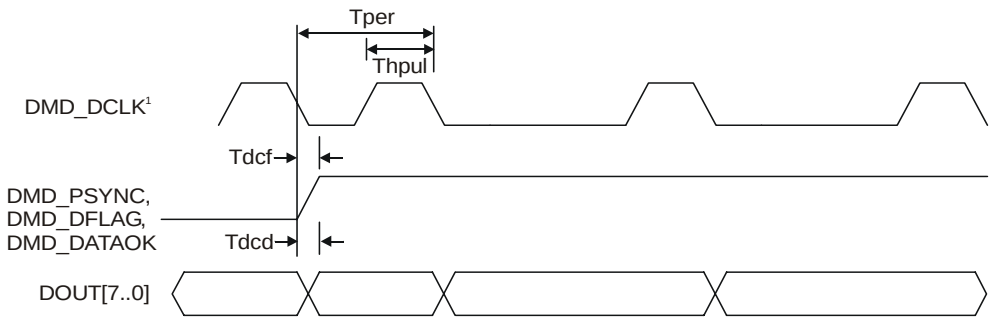


External Sync Byte Mode.[1]

FIGURE 10 Modulator Packet Definition

[1] When using Internal Sync Byte Mode, byte-wide data is input to the modulator at a constant rate defined by the configured data rate. Reed Solomon packetization is transparent to the input interface.

Demodulator Data Output Timing

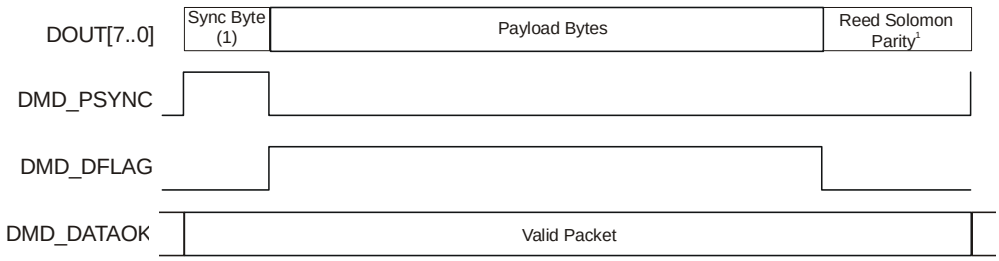


[1]The DMD_DCLK is asynchronous to the output data rate and is a gated version of the demodulator's process clock. Its periodicity varies significantly based on Symbol Rate and Decimating Filter configurations. If a continuous output clock is desired, the user must provide some form of "elastic buffer" external to the modem.

FIGURE 11 Demodulator Data Output Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
Tper	DMD_DCLK Clock Period Note: Worst case, assumes consecutive pulses are gated by the demodulator.	11.76	N/A	nsec
Thpul	DMD_DCLK High Width	3.7	N/A	
Tdcf	Delay Clock to DMD_DFLAG, DMD_PSYNC	-.05	2	
Tdcd	Delay Clock to DOUT			

Demodulator RS Data Packet Definition



[1]Sixteen Reed Solomon parity bytes are output whether encoding is enabled or disabled.

FIGURE 12 Demodulator Data Packet Definition

Reed Solomon (RS) packet size is calculated as follows:

- RS Packet Size = 1 Sync Byte + Payload Bytes + 16 RS Parity Bytes
  - Sync byte: (external sync mode) supplied by the host connected to the transmitting modem, (internal sync mode) supplied internally by the transmitting modem
  - Payload bytes: supplied by the host connected to the transmitting modem
  - RS parity bytes: supplied internally by the transmitting modem
- An RS packet length of 240 = 1 Sync Byte + 223 Payload Bytes + 16 RS Parity Bytes. Supported by External Sync Mode only.
- An RS packet length of 255 = 1 Sync Byte + 238 Payload Bytes + 16 RS Parity Bytes. Supported by Internal Sync Mode only.

AGC Timing

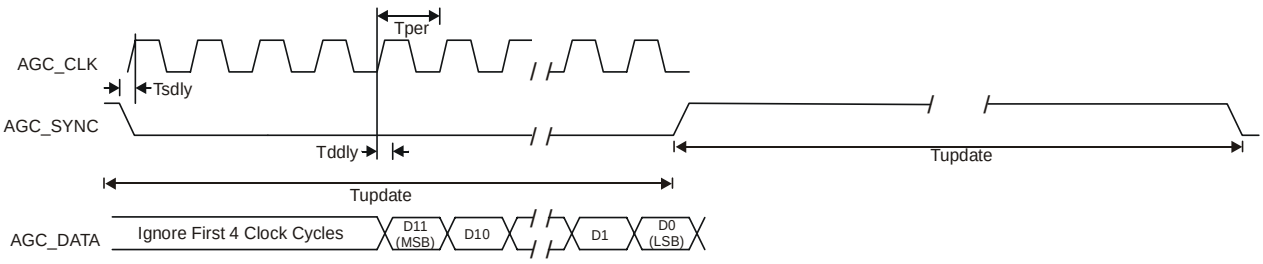


FIGURE 13 AGC Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
Tper	AGC_CLK Clock Period, 50% ± 5% Duty Cycle	200	N/A	nsec
Tsdly	AGC_SYNC delay from AGC_CLK	0	5	
Tddly	AGC_DATA delay from AGC_CLK	0	10	
Tupdate	Delay between updates	3.2 Typical		µs

Mechanical Drawings

Measurements are in inches.

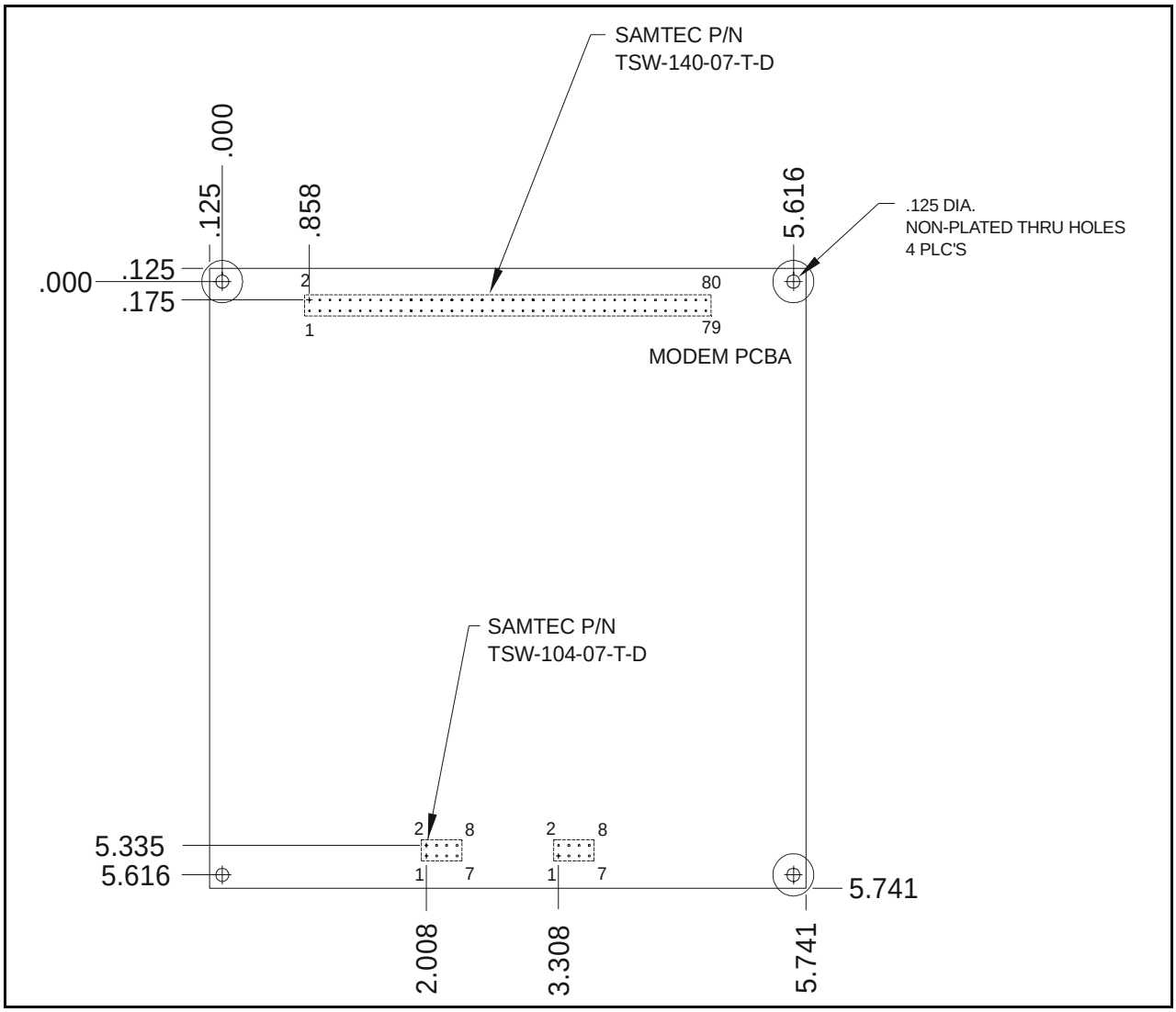


FIGURE 14 Modem PCBA Mechanical Dimensions (Top View)

Applications

Suggested Baseband Interfaces to the Modem

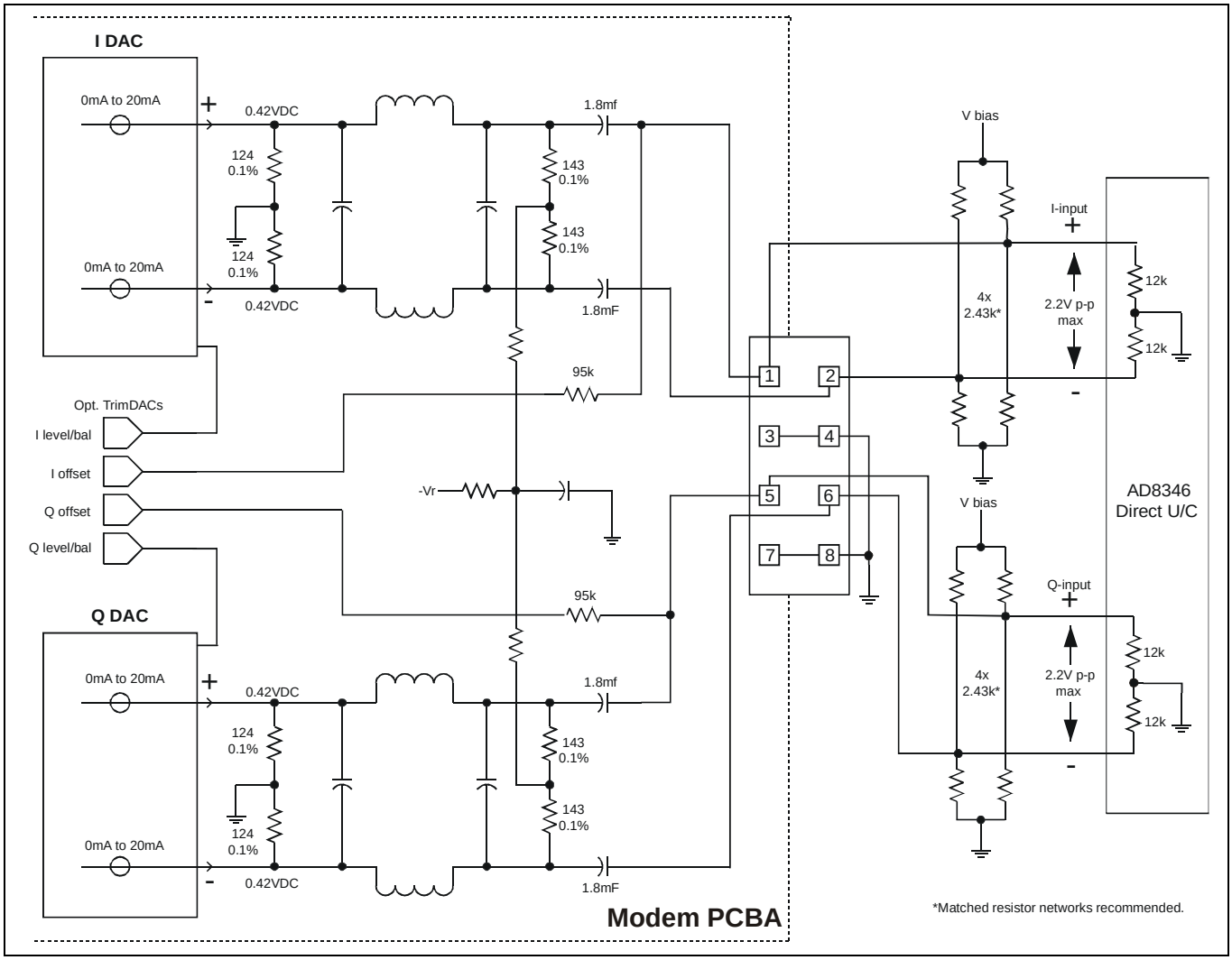


FIGURE 15 Modulator Baseband Interface to ISL83740EVAL/ISL83700EVAL Platform

This figure shows an IF interface to an L-band daughterboard (included with the Evaluation Platform).

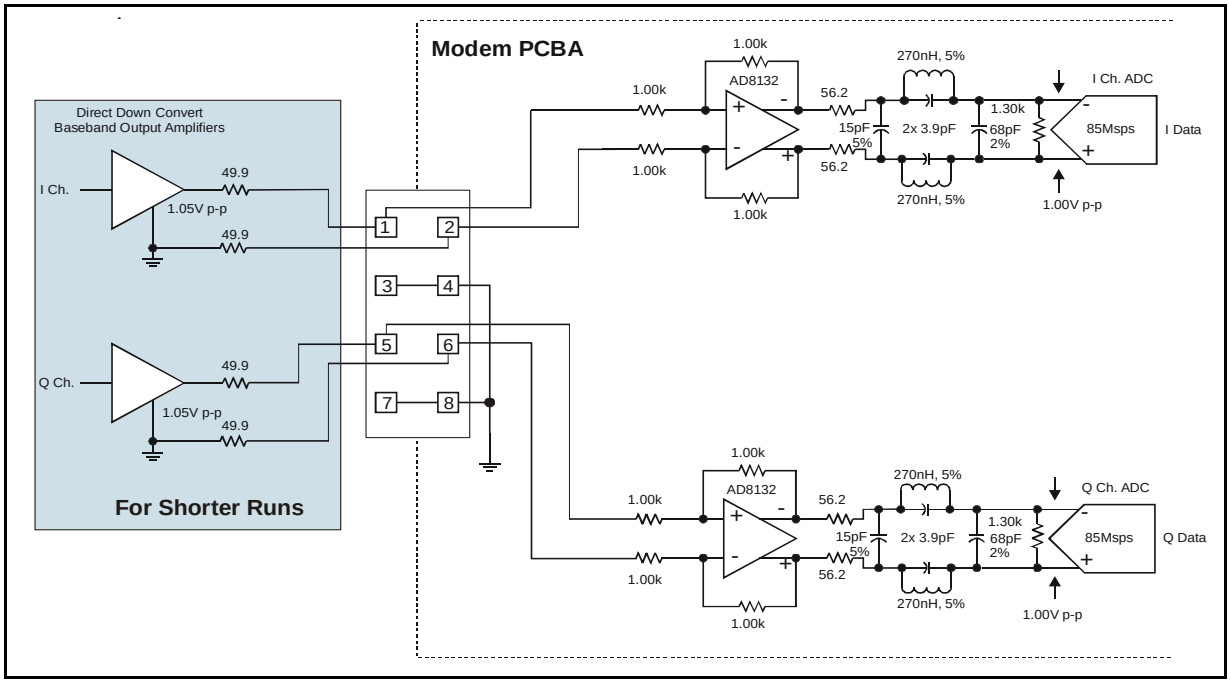


FIGURE 16 Unbalanced Demodulator Baseband Interface, Shorter Runs

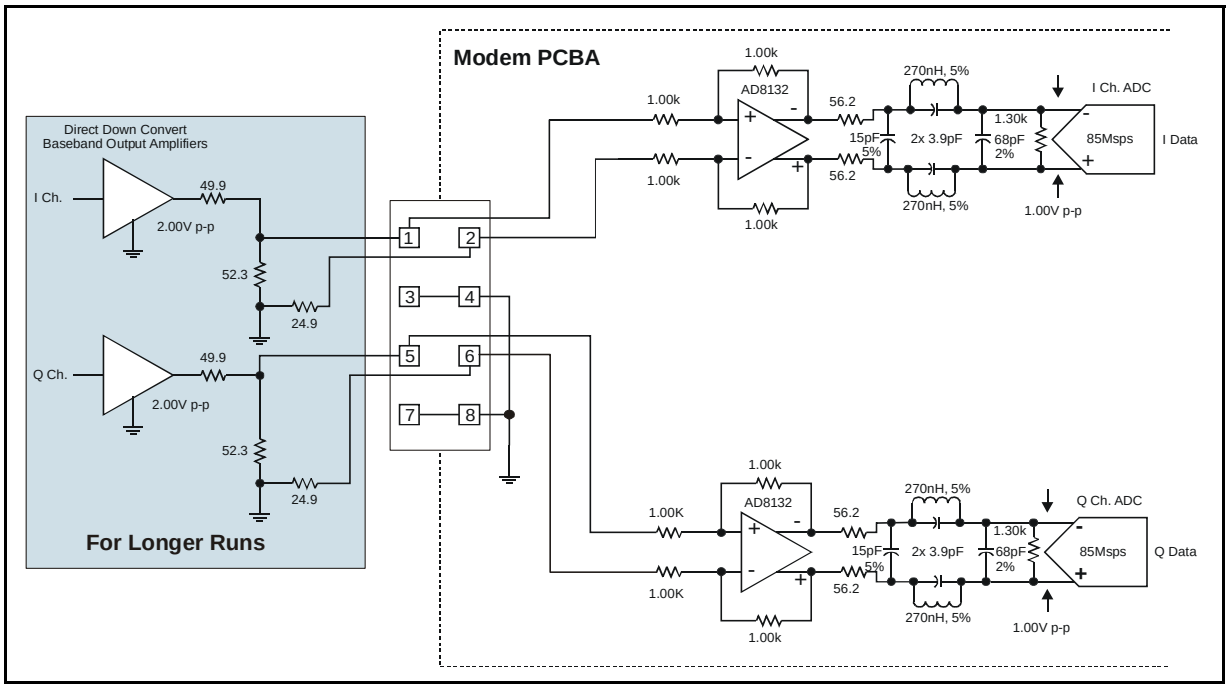


FIGURE 17 Unbalanced Demodulator Baseband Interface, Longer Runs

Support

Note: In some cases, users may enter parameters outside of ranges listed in this document; however, only listed ranges are supported.

Related Documentation

For a list and description of documentation included with Intersil CommLink Broadband products, see the ReadMeFirst Application Note (AN9940).

Additional documentation, product information, and press releases may be posted on the Intersil web page: www.intersil.com/design/commlink/broadbandmodem.asp.

Release Notes

ISL83740	Rev 5	The following is a change to the documentation to make it match the system. Changed Binary modulation type for 128QAM to 8 (was 7). See **Modulation, Inner Code Rates, and Ranges on page 7**.
ISL837030 and ISL83740	Rev 4	Added support for ISL83740 functionality, higher data rates. See **Modulation, Inner Code Rates, and Ranges on page 7**. Manual updated in other places where rates are listed to show which rates apply to ISL83740 and ISL837030. Changed Baseband Output Level into recommended load: Nominal 1.9V p-p (was 1.95V p-p), Maximum 2.2V p-p (was 2.45V p-p). Changed Baseband Output Adjust Resolution: Programmable +1.5dB to -4dB (was +2dB to -4dB). See **Modulator Output Electrical Specifications on page 8**, **FIGURE 7 Modulator Connector Pin Configuration on page 18** (configuration), and **FIGURE 15 Modulator Baseband Interface to ISL83740EVAL/ISL83700EVAL Platform on page 23**. Updated BER performance table to add new data rates/related information. See **BER Performance (Typical) on page 10**. Changed ANALOG_AGC current to be ± 3mA maximum (was ± 6mA maximum). See **ANALOG_AGC on page 16.** Added Acquisition and Tracking Range chart. See **Demodulator Performance Specifications on page 10.** A reference to baud rates being > 10Mbaud added to note under BER performance. See **BER Performance (Typical) on page 10**. Added support for mdleaver command (ISL83740 only). See Programmer's Reference AN9935.
ISL837030	Rev 3	Added Tupdate to AGC Timing Diagram. Changed Tper MIN to be 200 (was 100). See **AGC Timing on page 21**.
	Rev 2	Corrected Thpul minimum from 5.29 to 3.7. **, page 20**. Updated Demodulator Airflow Requirements. **Demodulator ASSP Airflow Requirements on page 12.** Corrected MTBF. **Reliability on page 12**
	Rev 1	Initial Release

Customer Support

Intersil CommLink Broadband creates reference designs and related products for broadband wireless digital communications. If you have questions, comments, or suggestions concerning the product or this manual, please contact Intersil Customer Support at www.intersil.com.