

Dual LDO with Low Noise, Low I_Q , and High PSRR

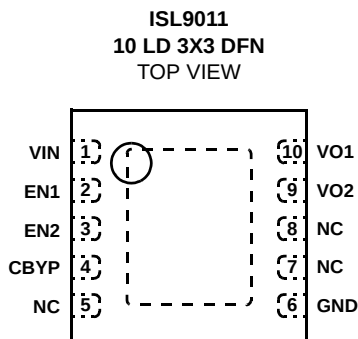
ISL9011 is a high performance dual LDO capable of sourcing 150mA current from channel 1 and 300mA from channel 2. The device has a low standby current and high-PSRR and is stable with output capacitance of 1 μ F to 10 μ F with ESR of up to 200m Ω .

A reference bypass pin allows an external capacitor for adjusting a noise filter for low noise and high PSRR applications.

The quiescent current is typically only 45 μ A with both LDO's enabled and active. Separate enable pins control each individual LDO output. When both enable pins are low, the device is in shutdown, typically drawing less than 0.1 μ A.

Several combinations of voltage outputs are standard. Others are available on request. Output voltage options for each LDO range from 1.2V to 3.6V.

Pinout



Features

- Integrates two high performance LDOs
 - VO1 - 150mA output
 - VO2 - 300mA output
- Excellent transient response to large current steps
- Excellent load regulation:
 - <1% voltage change across full range of load current
- High PSRR: 70dB @ 1kHz
- Wide input voltage capability: 2.3V - 6.5V
- Extremely low quiescent current: 45 μ A (both LDOs active)
- Low dropout voltage: typically 120mV @ 150mA
- Low output noise: typically 30 μ Vrms @ 100 μ A (1.5V)
- Stable with 1-10 μ F ceramic capacitors
- Separate enable pins for each LDO
- Soft-start to limit input current surge during enable
- Current limit and overheat protection
- $\pm 1.8\%$ accuracy over all operating conditions
- Tiny 10 Ld 3x3mm DFN package
- -40°C to +85°C operating temperature range
- Pin compatible with Micrel MIC2211
- Pb-free plus anneal available (RoHS compliant)

Applications

- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Handheld Devices including Medical Handhelds

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	VO1 VOLTAGE (V)	VO2 VOLTAGE (V)	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL9011IRNNZ	DAAM	3.3	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRNJZ	DTAA	3.3	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRNFZ	DVAA	3.3	2.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRNCZ	DAAN	3.3	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRMNZ	DAAP	3.0	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRMMZ	DANA	3.0	3.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRMGZ	DAAS	3.0	2.7	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRLLZ	DAMA	2.9	2.9	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRKNZ	DAAW	2.85	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRKKZ	DWAA	2.85	2.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRKJZ	DYAA	2.85	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRKFZ	DABA	2.85	2.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRKPZ	DDHA	2.85	1.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRKCZ	DAEA	2.85	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRJNZ	DAAY	2.8	3.3	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRJMZ	DALA	2.8	3.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRJRZ	DAKA	2.8	2.6	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRJCZ	DAJA	2.8	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRJBZ	DACA	2.8	1.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRGPZ	DDGA	2.7	1.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRGCZ	DAHA	2.7	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRFJZ	DADA	2.5	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRFDZ	DCRA	2.5	2.0	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRFCZ	DBMA	2.5	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRPLZ	DAGA	1.85	2.9	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRPPZ	DDDA	1.85	1.85	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRCJZ	DBVA	1.8	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRCCZ	DCSA	1.8	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRBLZ	DBBF	1.5	2.9	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRBJZ	DAFA	1.5	2.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRBCZ	DBBH	1.5	1.8	-40 to +85	10 Ld 3x3 DFN	L10.3x3C
ISL9011IRBBZ	DDEA	1.5	1.5	-40 to +85	10 Ld 3x3 DFN	L10.3x3C

NOTES:

1. Add -T to part number for tape and reel.
2. For availability and lead time of devices with voltage combinations not listed in the table, contact Intersil Marketing.
3. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage (VIN) +7.1V
 All Other Pins -0.3 to (VIN+0.3)V

Recommended Operating Conditions

Ambient Temperature Range (TA) -40°C to 85°C
 Supply Voltage (VIN) 2.3V to 6.5V

Thermal Information

Thermal Resistance (Notes 4, 5) θ_{JA} (°C/W) θ_{JC} (°C/W)
 3x3 DFN Package 50 10
 Junction Temperature Range -40°C to +125°C
 Operating Temperature Range -40°C to +85°C
 Storage Temperature Range -65°C to +150°C
 Maximum Lead Temperature (Soldering 10s) +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- θ_{JC} , "case temperature" location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$; $V_{IN} = (V_O + 1.0\text{V})$ to 6.5V with a minimum V_{IN} of 2.3V; $C_{IN} = 1\mu\text{F}$; $C_O = 1\mu\text{F}$; $C_{BYP} = 0.01\mu\text{F}$

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Supply Voltage	V_{IN}		2.3		6.5	V
Ground Current		Quiescent condition: $I_{O1} = 0\mu\text{A}$; $I_{O2} = 0\mu\text{A}$				
	I_{DD1}	One LDO active		25	40	μA
	I_{DD2}	Both LDO active		45	60	μA
Shutdown Current	I_{DDS}	@25°C		0.1	1.0	μA
UVLO Threshold	V_{UV+}		1.9	2.1	2.3	V
	V_{UV-}		1.6	1.8	2.0	V
Regulation Voltage Accuracy		Variation from nominal voltage output, $V_{IN} = V_O + 0.5$ to 5.5V, $T_J = -40^\circ\text{C}$ to 125°C	-1.8		+1.8	%
Line Regulation		$V_{IN} = (V_{OUT} + 1.0\text{V})$ relative to highest output voltage) to 5.5V	-0.2	0	0.2	%/V
Load Regulation		$I_{OUT} = 100\mu\text{A}$ to 150mA (VO1 and VO2)		0.1	0.7	%
		$I_{OUT} = 100\mu\text{A}$ to 300mA (VO2)			1.0	%
Maximum Output Current	I_{MAX}	VO1: Continuous	150			mA
		VO2: Continuous	300			mA
Internal Current Limit	I_{LIM}		350	475	600	mA
Dropout Voltage (Note 6)	V_{DO1}	$I_O = 150\text{mA}$; $V_O > 2.1\text{V}$ (VO1)		125	200	mV
	V_{DO2}	$I_O = 300\text{mA}$; $V_O < 2.5\text{V}$ (VO2)		300	500	mV
	V_{DO3}	$I_O = 300\text{mA}$; $2.5\text{V} \leq V_O \leq 2.8\text{V}$ (VO2)		250	400	mV
	V_{DO4}	$I_O = 300\text{mA}$; $V_O > 2.8\text{V}$ (VO2)		200	325	mV
Thermal Shutdown Temperature	T_{SD+}			145		°C
	T_{SD-}			110		°C
AC CHARACTERISTICS						
Ripple Rejection		$I_O = 10\text{mA}$, $V_{IN} = 2.8\text{V}(\text{min})$, $V_O = 1.8\text{V}$, $C_{BYP} = 0.1\mu\text{F}$				
		@ 1kHz		70		dB
		@ 10kHz		55		dB
		@ 100kHz		40		dB
Output Noise Voltage		$I_O = 100\mu\text{A}$, $V_O = 1.5\text{V}$, $T_A = 25^\circ\text{C}$, $C_{BYP} = 0.1\mu\text{F}$ BW = 10Hz to 100kHz		30		μV_{rms}

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the operational supply voltage and temperature range of the device as follows:

$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$; $V_{IN} = (V_O + 1.0\text{V})$ to 6.5V with a minimum V_{IN} of 2.3V ; $C_{IN} = 1\mu\text{F}$; $C_O = 1\mu\text{F}$;
 $C_{BYP} = 0.01\mu\text{F}$ **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DEVICE START-UP CHARACTERISTICS						
Device Enable Time	T_{EN}	Time from assertion of the ENx pin to when the output voltage reaches 95% of the $V_O(\text{nom})$		250	500	μs
LDO Soft-Start Ramp Rate	T_{SSR}	Slope of linear portion of LDO output voltage ramp during start-up		30	60	$\mu\text{s/V}$
EN1, EN2 PIN CHARACTERISTICS						
Input Low Voltage	V_{IL}		-0.3		0.5	V
Input High Voltage	V_{IH}		1.4		$V_{IN} + 0.3$	V
Input Leakage Current	I_{IL}, I_{IH}				0.1	μA
Pin Capacitance	C_{PIN}	Informative		5		pF

NOTE:

6. $VO_x = 0.98 * VO_x(\text{NOM})$; Valid for VO_x greater than 1.85V .

Typical Performance Curves

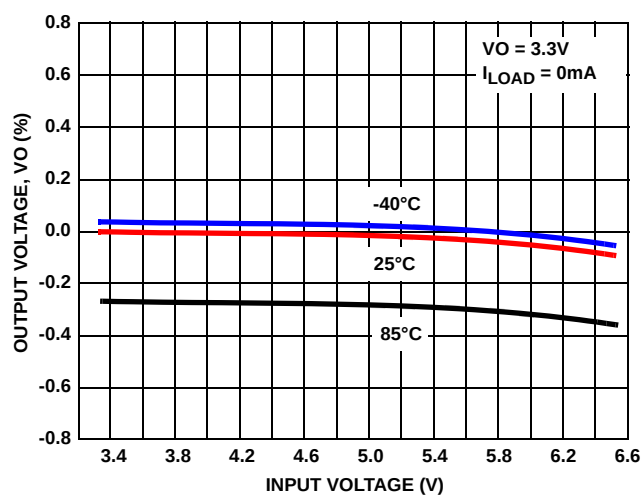


FIGURE 1. OUTPUT VOLTAGE vs INPUT VOLTAGE (3.3V OUTPUT)

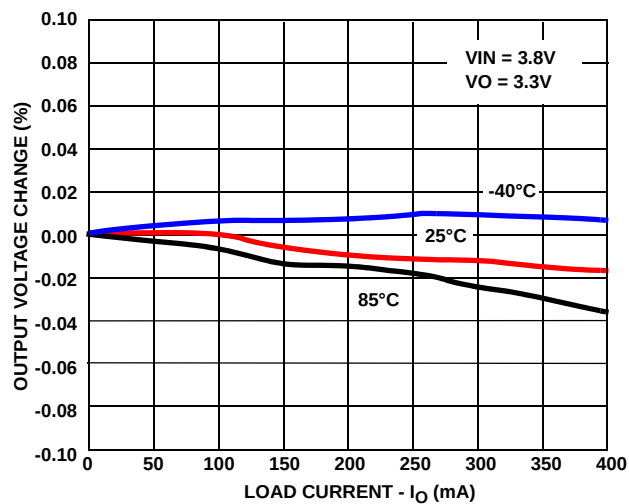


FIGURE 2. OUTPUT VOLTAGE CHANGE vs LOAD CURRENT

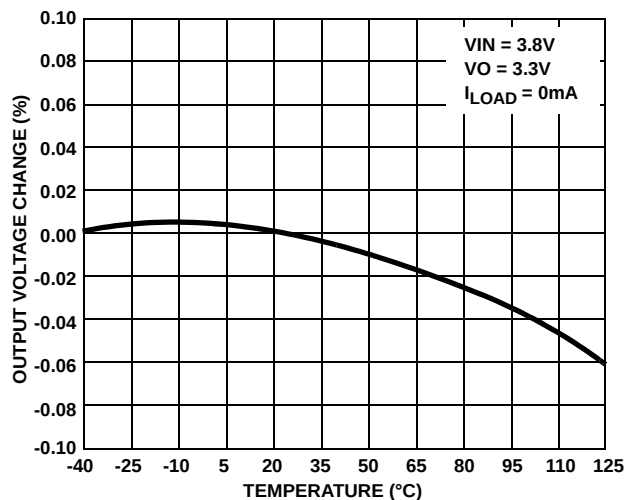


FIGURE 3. OUTPUT VOLTAGE CHANGE vs TEMPERATURE

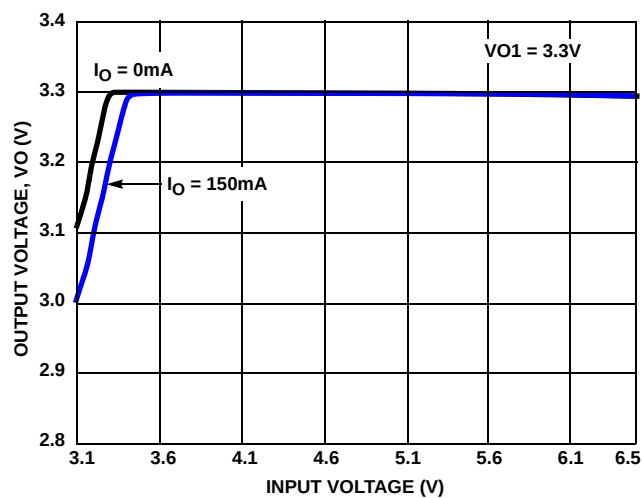


FIGURE 4. OUTPUT VOLTAGE vs INPUT VOLTAGE (VO1 = 3.3V)

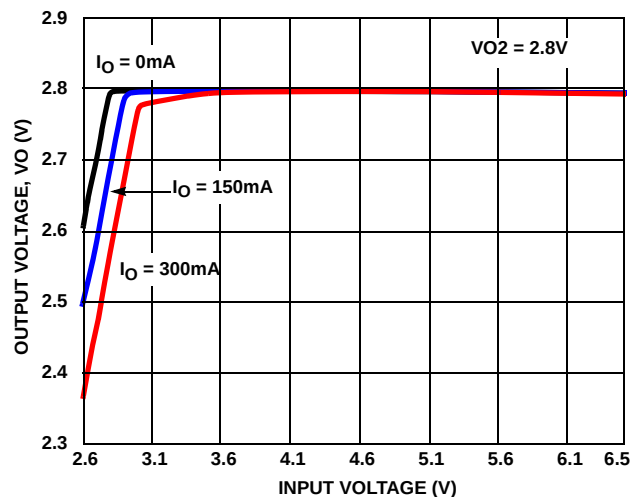


FIGURE 5. OUTPUT VOLTAGE vs INPUT VOLTAGE (VO2 = 2.8V)

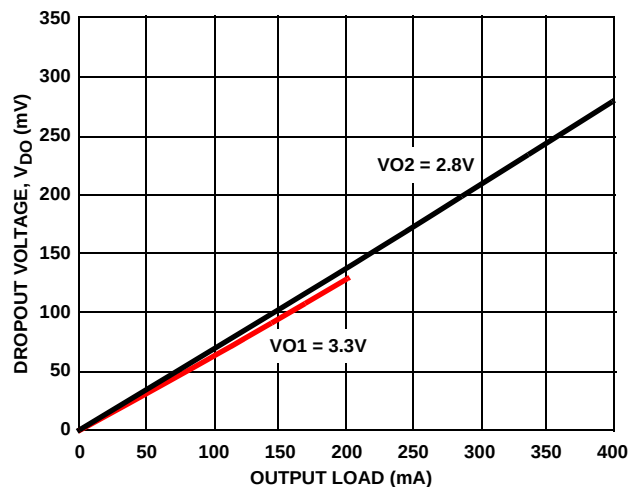


FIGURE 6. DROPOUT VOLTAGE vs LOAD CURRENT

Typical Performance Curves (Continued)

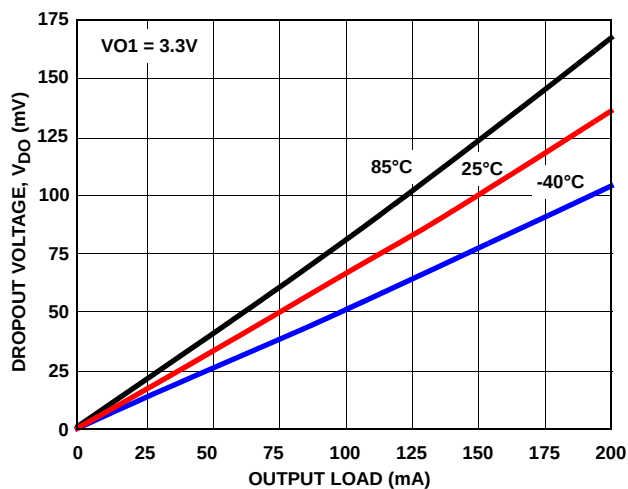


FIGURE 7. VO1 DROPOUT VOLTAGE vs LOAD CURRENT

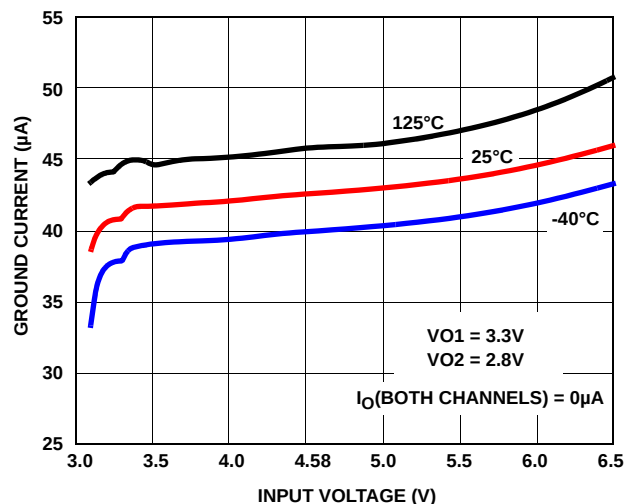


FIGURE 8. GROUND CURRENT vs INPUT VOLTAGE

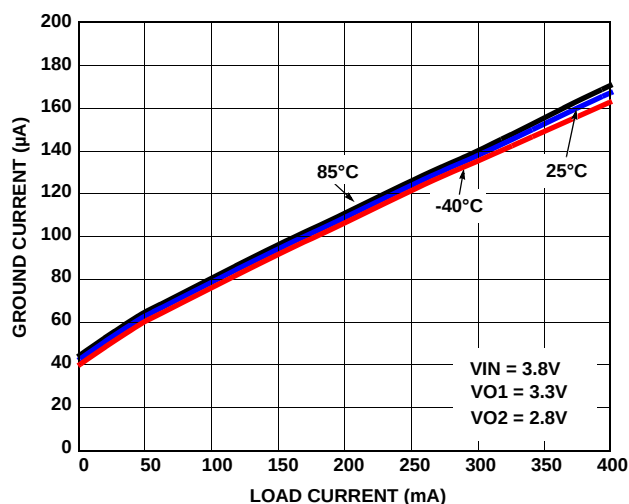


FIGURE 9. GROUND CURRENT vs LOAD

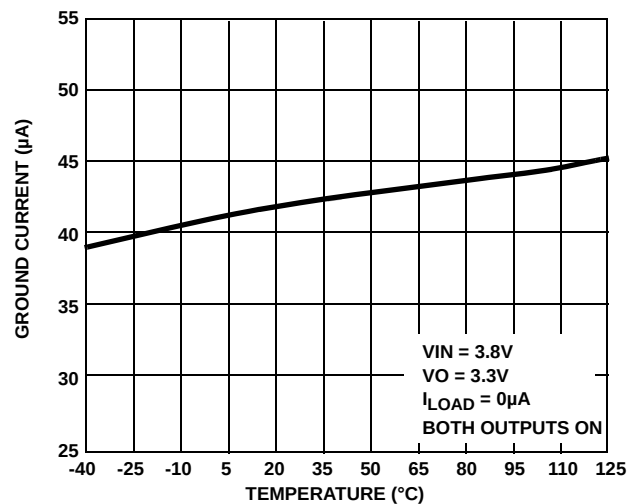


FIGURE 10. GROUND CURRENT vs TEMPERATURE

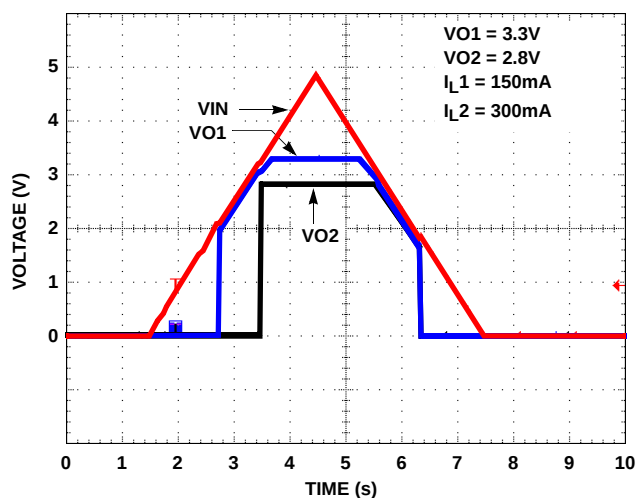


FIGURE 11. POWER-UP/POWER-DOWN

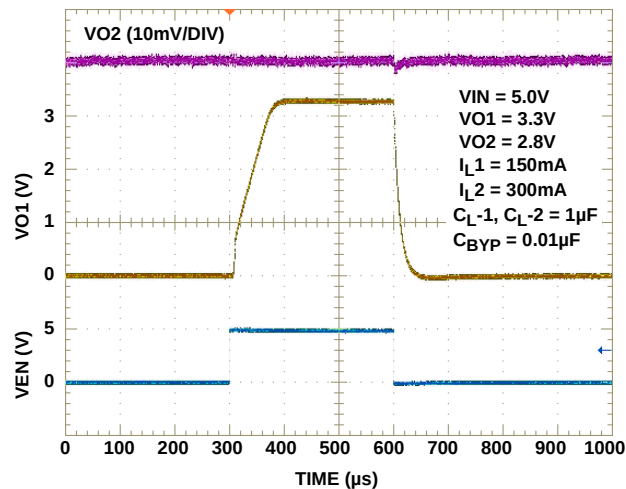


FIGURE 12. TURN-ON/TURN-OFF RESPONSE

Typical Performance Curves (Continued)

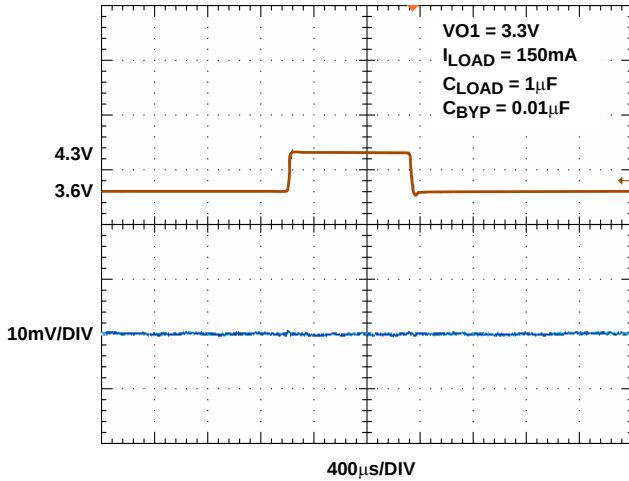


FIGURE 13. LINE TRANSIENT RESPONSE, 3.3V OUTPUT

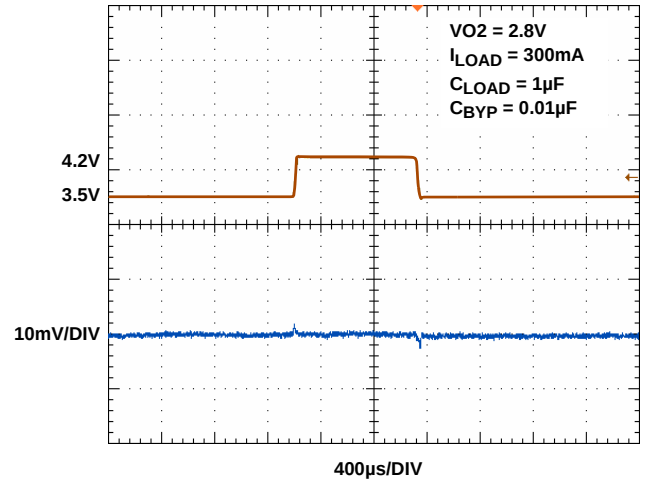


FIGURE 14. LINE TRANSIENT RESPONSE, 2.8V OUTPUT

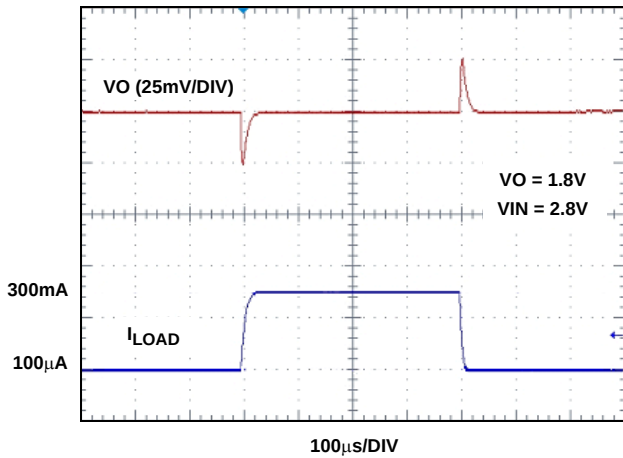


FIGURE 15. LOAD TRANSIENT RESPONSE

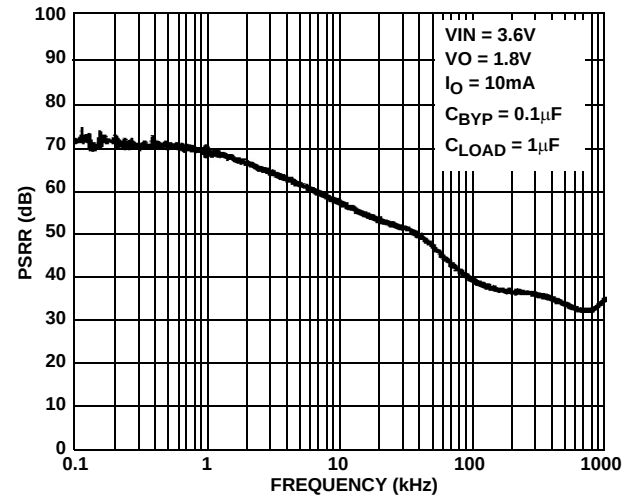


FIGURE 16. PSRR vs FREQUENCY

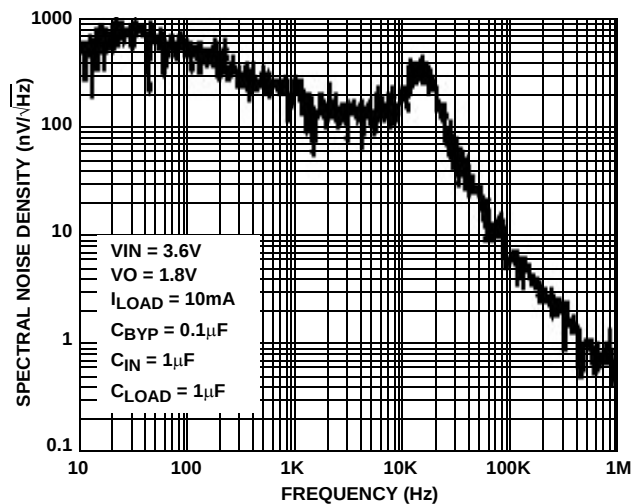
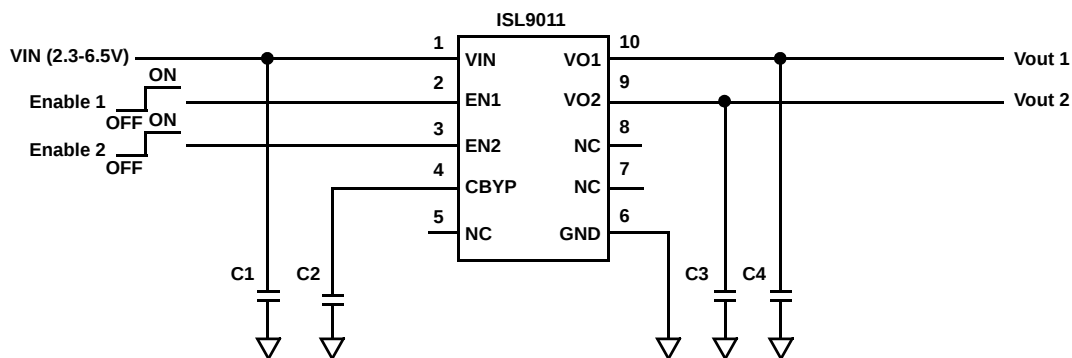


FIGURE 17. SPECTRAL NOISE DENSITY vs FREQUENCY

Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	VIN	Analog I/O	Supply Voltage / LDO Input: Connect a 1 μ F capacitor to GND.
2	EN1	Low Voltage Compatible CMOS Input	LDO-1 Enable.
3	EN2	Low Voltage Compatible CMOS Input	LDO-2 Enable.
4	CBYP	Analog I/O	Reference Bypass Capacitor Pin: Optionally connect capacitor of value 0.01 μ F to 1 μ F between this pin and GND to tune in the desired noise and PSRR performance.
5, 7, 8	NC	NC	No Connection
6	GND	Ground	GND is the connection to system ground. Connect to PCB Ground plane.
9	VO2	Analog I/O	LDO-2 Output: Connect capacitor of value 1 μ F to 10 μ F to GND (1 μ F recommended).
10	VO1	Analog I/O	LDO-1 Output: Connect capacitor of value 1 μ F to 10 μ F to GND (1 μ F recommended).

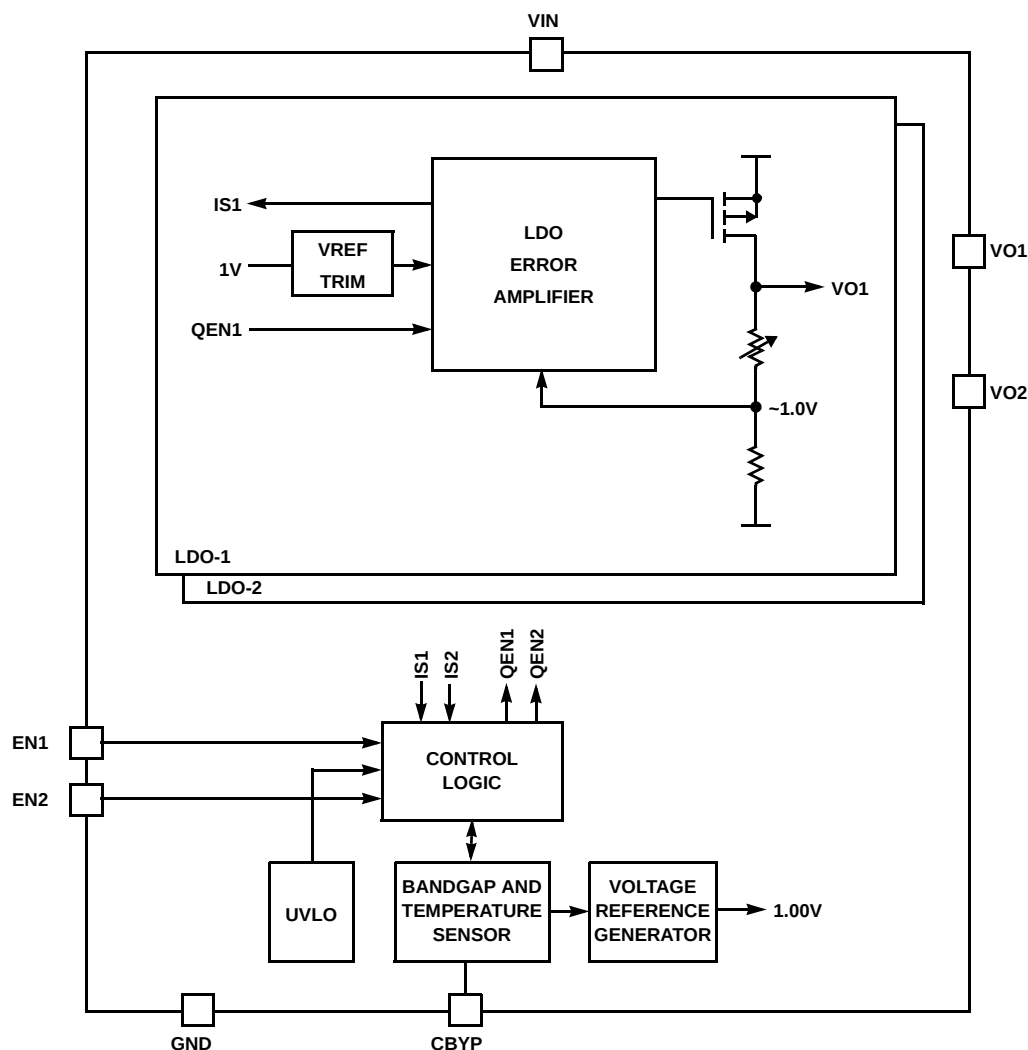
Typical Application



C1, C3, C4: 1 μ F X5R ceramic capacitor

C2: 0.1 μ F X5R ceramic capacitor

Block Diagram



Functional Description

The ISL9011 contains all circuitry required to implement two high performance LDO's. High performance is achieved through a circuit that delivers fast transient response to varying load conditions. In a quiescent condition, the ISL9011 adjusts its biasing to achieve the lowest standby current consumption.

The device also integrates current limit protection, smart thermal shutdown protection, staged turn-on and soft-start. Smart Thermal shutdown protects the device against overheating. Staged turn-on and soft-start minimize start-up input current surges without causing excessive device turn-on time.

Power Control

The ISL9011 has two separate enable pins, EN1 and EN2, to individually control power to each of the LDO outputs. When both EN1 and EN2 are low, the device is in shutdown

mode. During this condition, all on-chip circuits are off, and the device draws minimum current, typically less than 0.1 μ A. When one or both of the enable pins are asserted, the device first polls the output of the UVLO detector to ensure that VIN voltage is at least about 2.1V. Once verified, the device initiates a start-up sequence. During the start-up sequence, trim settings are first read and latched. Then, sequentially, the bandgap, reference voltage and current generation circuitry power-up. Once the references are stable, a fast-start circuit quickly charges the external reference bypass capacitor (connected to the CBYP pin) to the proper operating voltage. After the bypass capacitor has been charged, the LDO's power-up.

If EN1 is brought high, and EN2 goes high before the VO1 output stabilizes, the ISL9011 delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high, and EN1 goes high before VO2 starts its output ramp, then VO1 turns on first and the ISL9011 delays the VO2 turn-on until the VO1 output reaches its target level.

If EN2 is brought high, and EN1 goes high after VO2 starts its output ramp, then the ISL9011 immediately starts to ramp up the VO1 output.

If both EN1 and EN2 are brought high at the same time, the VO1 output has priority, and is always powered up first.

During operation, whenever the VIN voltage drops below about 1.8V, the ISL9011 immediately disables both LDO outputs. When VIN rises back above 2.1V, the device re-initiates its start-up sequence and LDO operation will resume automatically.

Reference Generation

The reference generation circuitry includes a trimmed bandgap, a trimmed voltage reference divider, a trimmed current reference generator, and an RC noise filter. The filter includes the external capacitor connected to the CBYP pin. A 0.01 μ F capacitor connected CBYP implements a 100Hz lowpass filter, and is recommended for most high performance applications. For the lowest noise application, a 0.1 μ F or greater CBYP capacitor should be used. This filters the reference noise to below the 10Hz – 1kHz frequency band, which is crucial in many noise-sensitive applications.

The bandgap generates a zero temperature coefficient (TC) voltage for the reference divider. The reference divider provides the regulation reference and other voltage references required for current generation and over-temperature detection.

The current generator outputs references required for adaptive biasing as well as references for LDO output current limit and thermal shutdown determination.

LDO Regulation and Programmable Output Divider

The LDO Regulator is implemented with a high-gain operational amplifier driving a PMOS pass transistor. The design of the ISL9011 provides a regulator that has low quiescent current, fast transient response, and overall stability across all operating and load current conditions. LDO stability is guaranteed for a 1 μ F to 10 μ F output capacitor that has a tolerance better than 20% and ESR less than 200m Ω . The design is performance-optimized for a 1 μ F capacitor. Unless limited by the application, use of an output capacitor value above 4.7 μ F is not recommended as LDO performance improvement is minimal.

Soft-start circuitry integrated into each LDO limits the initial ramp-up rate to about 30 μ s/V to minimize current surge. The ISL9011 provides short-circuit protection by limiting the output current to about 475mA.

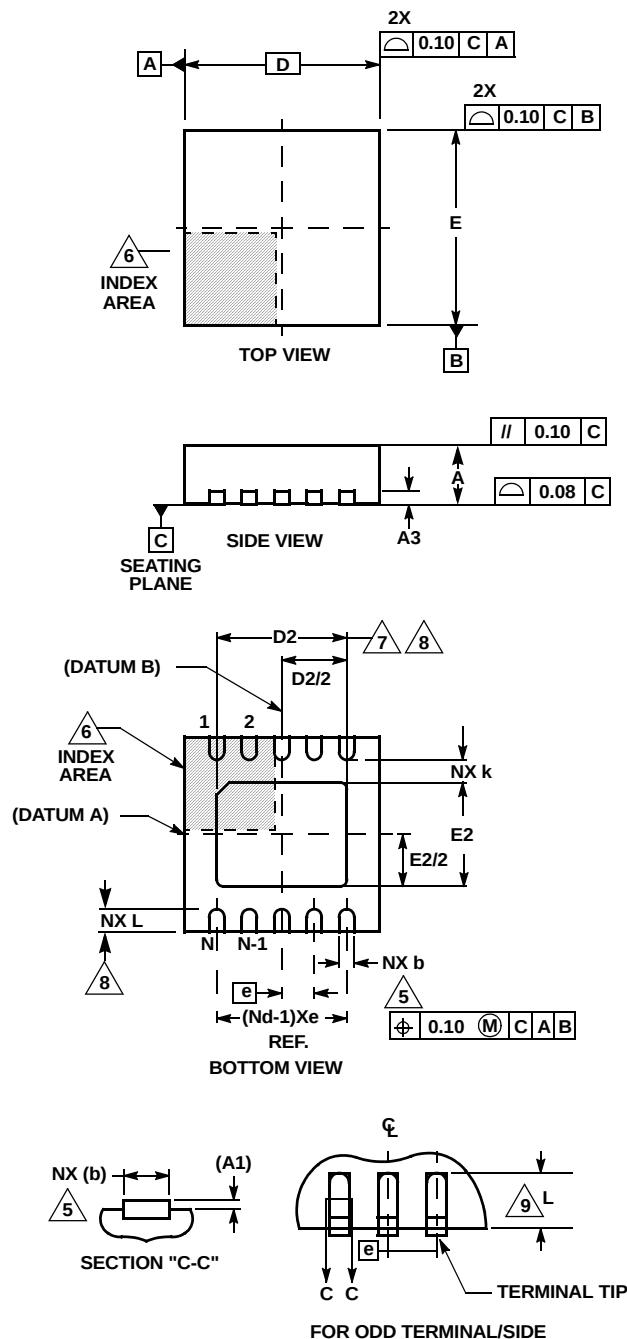
Each LDO uses an independently trimmed 1V reference. An internal resistor divider drops the LDO output voltage down

to 1V. This is compared to the 1V reference for regulation. The resistor division ratio is programmed in the factory.

Overheat Detection

The bandgap outputs a proportional-to-temperature current that is indicative of the temperature of the silicon. This current is compared with references to determine if the device is in danger of damage due to overheating. When the die temperature reaches about 145°C, one or both of the LDO's momentarily shut down until the die cools sufficiently. In the overheat condition, only the LDO sourcing more than 50mA will be shut off. This does not affect the operation of the other LDO. If both LDOs source more than 50mA and an overheat condition occurs, both LDO outputs are disabled. Once the die temperature falls back below about 110°C, the disabled LDO(s) are re-enabled and soft-start automatically takes place.

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3C

10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.85	0.90	0.95	-
A1	-	-	0.05	-
A3	0.20 REF			-
b	0.20	0.25	0.30	5, 8
D	3.00 BSC			-
D2	2.33	2.38	2.43	7, 8
E	3.00 BSC			-
E2	1.59	1.64	1.69	7, 8
e	0.50 BSC			-
k	0.20	-	-	-
L	0.35	0.40	0.45	8
N	10			2
Nd	5			3

Rev. 1 4/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-WEED-3 except for dimensions E2 & D2.

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