Digitally Controlled Potentiometer (XDCP™)

The Intersil ISL90727 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, and a control section. The wiper position is controlled by an I^2C interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the SDA and SCL inputs.

The device can be used in a wide variety of applications including:

- Mechanical potentiometer replacement
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- RF amplifier biasing
- LCD brightness and contrast adjustment
- Gain control and offset adjustment

Ordering Information

PART NUMBER (See Note)	RESISTANCE OPTION (Ω)	TEMP RANGE (°C)	PACKAGE (Pb-Free)
ISL90727WIE6Z	10K	-40 to +85	6-Pin SC-70
ISL90727UIE6Z	50K	-40 to +85	6-Pin SC-70
ISL90727WIE6Z-TK	10K	-40 to +85	6-Pin SC-70
ISL90727UIE6Z-TK	50K	-40 to +85	6-Pin SC-70

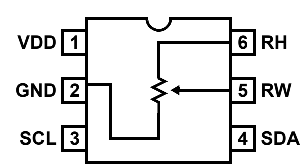
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Volatile Solid-State Potentiometer
- I^2C Serial Bus Interface
- DCP Terminal Voltage, 2.7V to 5.5V
- Low Tempco
  - Rheostat - 45 ppm/°C typical @ 25°C
  - Divider - 15 ppm/°C typical @ 25°C
- 128 Wiper Tap Points
  - Wiper resistance 70Ω typ at V_{CC} = 3.3V
- Low Power CMOS
  - Active current, 200μA max
  - Standby current, 500nA max
- Available R_{TOTAL} Values = 50kΩ, 10kΩ
- Power on Preset to Midscale
- Direct replacement for AD5247
- Packaging
  - 6 Ld SC70
- Pb-free plus anneal available (RoHS compliant)

Pinout

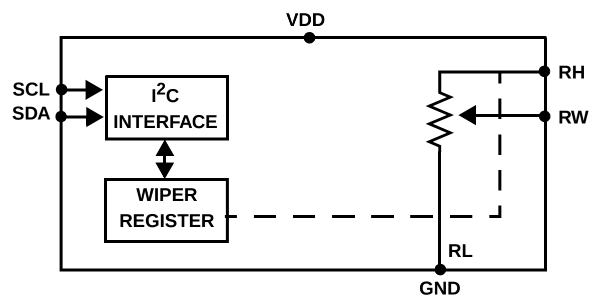
ISL90727
(6-PIN SC70)
TOP VIEW



Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1	VDD	Supply Voltage
2	GND	Ground
3	SCL	Serial Clock
4	SDA	Serial Data
5	RW	Potentiometer Wiper Terminal
6	RH	Potentiometer High Terminal

Block Diagram



Absolute Maximum Ratings

Storage temperature . . . . -65°C to +150°C
Voltage at any digital interface pin
with respect to V_{SS} . . . . -0.3V to V_{CC}+0.3
V_{CC} . . . . -0.3V to +7V
Voltage at any DCP pin with
respect to V_{SS} . . . . -0.3V to V_{CC}
Lead temperature (soldering, 10s). . . . . 300°C
I_W (10s) . . . . ±6mA
Latchup . . . . Class II, Level B at 85°C
ESD . . . . >2kV Human Body Model

Recommended Operating Conditions

Industrial . . . . -40°C to +85°C
V_{CC} . . . . 2.7V to 5.5V
Power rating of each DCP 5mW

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Analog Specifications

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
R_{TOTAL}	R_H to R_L resistance	W, U versions respectively		10, 50		kΩ
	R_H to R_L resistance tolerance		-20		+20	%
R_W	Wiper resistance	V_{CC} = 3.3V @ 25°C		85	200	Ω
$C_H/C_L/C_W$ (Note 10)	Potentiometer Capacitance			10/10/ 25		pF
I_{LkgDCP}	Leakage on DCP pins (Note 10)	Voltage at pin from GND to V_{CC}		0.1		µA
VOLTAGE DIVIDER MODE						
INL	Integral non-linearity		-1	±0.2	1	LSB (Note 2)
DNL	Differential non-linearity	Monotonic over all tap positions — W option	-1	±0.1	1	LSB (Note 2)
		U option	-1	±0.1	1	LSB (Note 2)
ZSerror (Note 3)	Zero-scale error	W option	0	1	3	LSB (Note 2)
		U option	0	0.5	1	
FSerror (Note 4)	Full-scale error	W option	-3	-1	0	LSB (Note 2)
		U option	-1	-0.5	0	
TC_V (Note 10)	Ratiometric Temperature Coefficient	DCP Register set to 80 hex		±15		ppm/°C
RESISTOR MODE						
RINL (Note 8)	Integral non-linearity	DCP register set between 20 hex and FF hex. Monotonic over all tap positions	-2	±0.25	2	MI (Note 5)
RDNL (Note 7)	Differential non-linearity	DCP register set between 20 hex and FF hex. Monotonic over all tap positions — W option	-1	±0.1	1	MI (Note 5)
		U option	-1	±0.1	1	MI (Note 5)
Roffset (Note 6)	Offset	W option	0	1	3	MI (Note 5)
		U option	0	0.5	1	MI (Note 5)
TC_R (Notes 9, 10)	Resistance Temperature Coefficient	DCP register set between 20 hex and FF hex		±45		ppm/°C

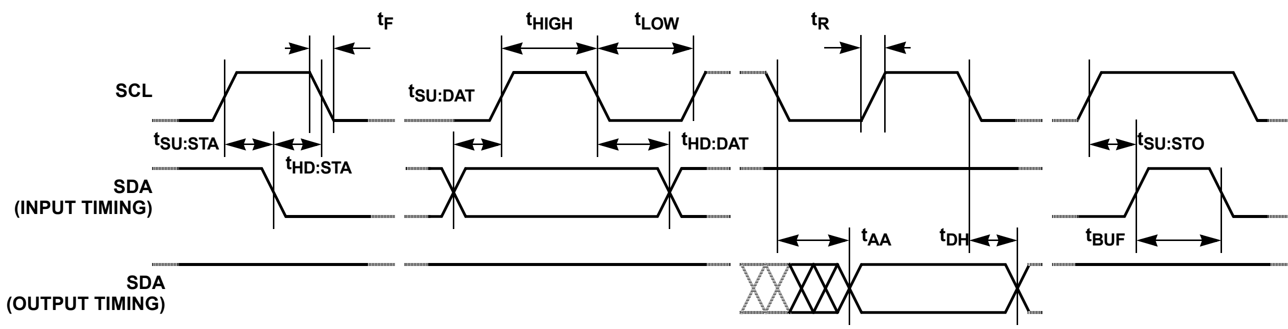
Operating Specifications

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
I_{CC1}	V_{CC} supply current (Volatile write/read)	f_{SCL} = 400kHz; SDA = Open; (for I^2C, Active, Read and Volatile Write States only)			200	µA
I_{SB}	V_{CC} current (standby)	V_{CC} = +5.5V, I^2C Interface in Standby State			500	nA
I_{ComLkg}	Common-Mode Leakage	Voltage at SDA pin to GND or V_{CC}			3	µA
t_{DCP} (Note 10)	DCP wiper response time	SCL falling edge of last bit of DCP Data Byte to wiper change		500		ns
V_{CC}Ramp	V_{CC} ramp rate		0.2			V/ms
t_D	Power-up delay	V_{CC} above Vpor, to DCP Initial Value Register recall completed, and I^2C Interface in standby state			3	ms
SERIAL INTERFACE SPECIFICATIONS						
V_{IL}	SDA, and SCL input buffer LOW voltage		-0.3		0.3* V_{CC}	V
V_{IH}	SDA, and SCL input buffer HIGH voltage		0.7* V_{CC}		V_{CC}+ 0.3	V
Hysteresis	SDA and SCL input buffer hysteresis		0.05* V_{CC}			V
V_{OL}	SDA output buffer LOW voltage, sinking 4mA		0		0.4	V
Cpin (Note 12)	SDA, and SCL pin capacitance				10	pF
f_{SCL}	SCL frequency				400	kHz
t_{IN}	Pulse width suppression time at SDA and SCL inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t_{AA}	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V_{CC}, until SDA exits the 30% to 70% of V_{CC} window.			900	ns
t_{BUF}	Time the bus must be free before the start of a new transmission	SDA crossing 70% of V_{CC} during a STOP condition, to SDA crossing 70% of V_{CC} during the following START condition.	1300			ns
t_{LOW}	Clock LOW time	Measured at the 30% of V_{CC} crossing.	1300			ns
t_{HIGH}	Clock HIGH time	Measured at the 70% of V_{CC} crossing.	600			ns
$t_{SU:STA}$	START condition setup time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{CC}.	600			ns
$t_{HD:STA}$	START condition hold time	From SDA falling edge crossing 30% of V_{CC} to SCL falling edge crossing 70% of V_{CC}.	600			ns
$t_{SU:DAT}$	Input data setup time	From SDA exiting the 30% to 70% of V_{CC} window, to SCL rising edge crossing 30% of V_{CC}	100			ns
$t_{HD:DAT}$	Input data hold time	From SCL rising edge crossing 70% of V_{CC} to SDA entering the 30% to 70% of V_{CC} window.	0			ns
$t_{SU:STO}$	STOP condition setup time	From SCL rising edge crossing 70% of V_{CC}, to SDA rising edge crossing 30% of V_{CC}.	600			ns
$t_{HD:STO}$	STOP condition hold time for read, or volatile only write	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{CC}.	600			ns
t_{DH}	Output data hold time	From SCL falling edge crossing 30% of V_{CC}, until SDA enters the 30% to 70% of V_{CC} window.	0			ns
t_R (Note 12)	SDA and SCL rise time	From 30% to 70% of V_{CC}	20 + 0.1 * Cb		250	ns

Operating Specifications (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
t_F (Note 12)	SDA and SCL fall time	From 70% to 30% of V_{CC}	20 + 0.1 * Cb		250	ns
Cb (Note 12)	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
Rpu (Note 12)	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2~2.5kΩ. For Cb = 40pF, max is about 15~20kΩ	1			kΩ

SDA vs SCL Timing



NOTES:

1. Typical values are for T_A = 25°C and 3.3V supply voltage.
2. LSB: $[V(R_W)_{127} - V(R_W)_0]/127$. $V(R_W)_{127}$ and $V(R_W)_0$ are $V(R_W)$ for the DCP register set to FF hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
3. ZS error = $V(R_W)_0$/LSB.
4. FS error = $[V(R_W)_{127} - V_{CC}]$/LSB.
5. MI = $|R_{127} - R_0|/127$. R_{127} and R_0 are the measured resistances for the DCP register set to FF hex and 00 hex respectively. Roffset = R_0/MI, when measuring between R_W and R_L.
6. Roffset = R_{127}/MI, when measuring between R_W and R_H.
7. RDNL = $(R_i - R_{i-1})$/MI, for i = 32 to 127.
8. RINL = $[R_i - (MI \cdot i) - R_0]$/MI, for i = 32 to 127.
9. $TC_R = \frac{[Max(Ri) - Min(Ri)]}{[Max(Ri) + Min(Ri)]/2} \times \frac{10^6}{125°C}$ for i = 32 to 127, T = -40°C to 85°C. Max( ) is the maximum value of the resistance and Min ( ) is the minimum value of the resistance over the temperature range.
10. This parameter is not 100% tested.
11. V_{IL} = 0V, $V_{IH} = V_{CC}$.
12. These are I^2C-specific parameters and are not directly tested. However, they are used in the device testing to validate specifications.

Principles of Operation

The ISL90727 is an integrated circuit incorporating one DCP with its associated registers and an I^2C serial interface providing direct communication between a host and the potentiometer.

DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The R_W pin of the DCP is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal within the DCP is controlled by a 7-bit volatile Wiper Register (WR). The DCP has its own WR. When the WR of the DCP contains all zeroes (WR<6:0>= 00h), its wiper terminal (R_W) is closest to its “Low” terminal (R_L). When the WR of the DCP contains all ones (WR<6:0>=7Fh), its wiper terminal (R_W) is closest to its “High” terminal (R_H). As the value of the WR increases from all zeroes (00h) to all ones (127 decimal), the wiper moves monotonically from the position closest to R_L to the position closest to R_H. At the same time, the resistance between R_W and R_L increases monotonically, while the resistance between R_H and R_W decreases monotonically. R_L is connected to the GND pin of the device, so the wiper movement will always be relative to R_L.

While the ISL90727 is being powered up, the WR is reset to 20h (64 decimal), which locates R_W roughly at the center between R_L and R_H.

The WR and IVR can be read or written directly using the I^{2}C serial interface as described in the following sections.

I^{2}C Serial Interface

The ISL90727 supports bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL90727 operates as slave device in all applications.

All communication over the I^{2}C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 1). On power-up of the ISL90727, the SDA pin is in the input mode.

All I^{2}C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL90727 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 1). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I^{2}C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 1).

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 2).

The ISL90727 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL90727 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

A valid Identification Byte contains 0101000 as the seven MSBs. The LSB in the Read/$\overline{\text{Write}}$ bit. Its value is “1” for a Read operation, and “0” for a Write operation (See Table 1).

TABLE 1. IDENTIFICATION BYTE FORMAT

0	1	0	1	0	0	0	$R/\overline{W}$
(MSB)							(LSB)

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL90727 responds with an ACK. At this time, the device enters its standby state (See Figure 3).

Data Protection

A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0, the Data Byte is transferred to the Wiper Register (WR) at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If an address other than 00h or an invalid slave address is sent, then the device will respond with no ACK.

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 4). The master initiates the operation issuing the following sequence: a START, the Identification byte with the $R/\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the $R/\overline{W}$ bit set to “1”. After each of the three bytes, the ISL90727 responds with an ACK. Then the ISL90727 transmits the Data Byte as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (See Figure 4).

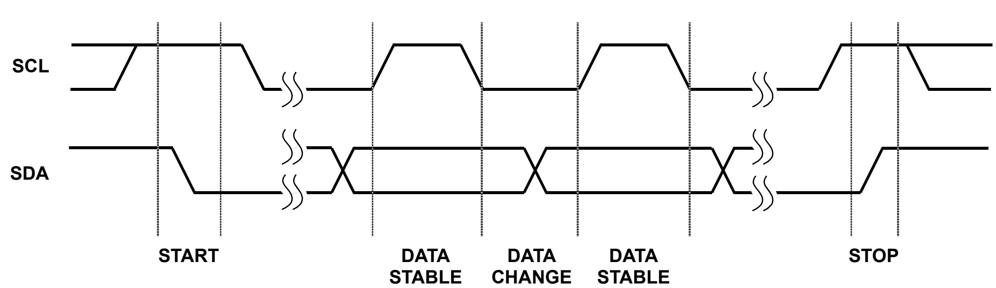


FIGURE 1. VALID DATA CHANGES, START, AND STOP CONDITIONS

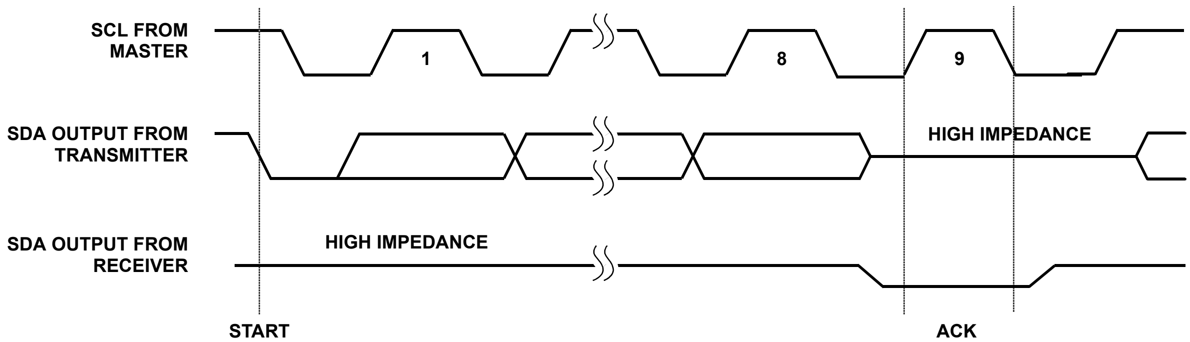


FIGURE 2. ACKNOWLEDGE RESPONSE FROM RECEIVER

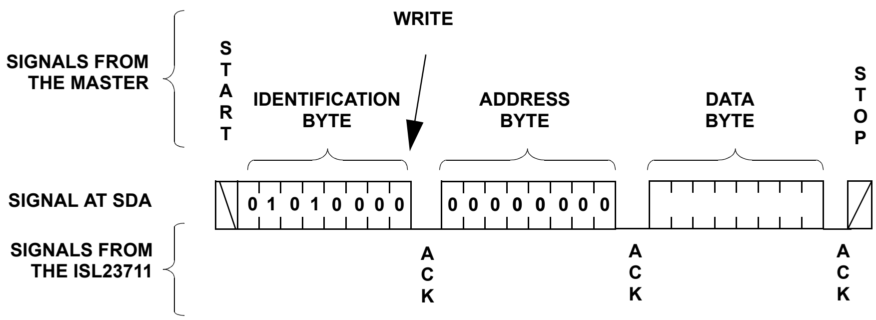


FIGURE 3. BYTE WRITE SEQUENCE

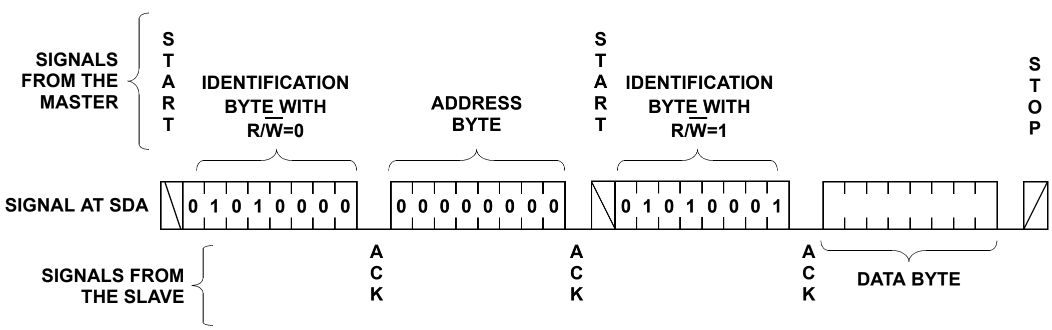
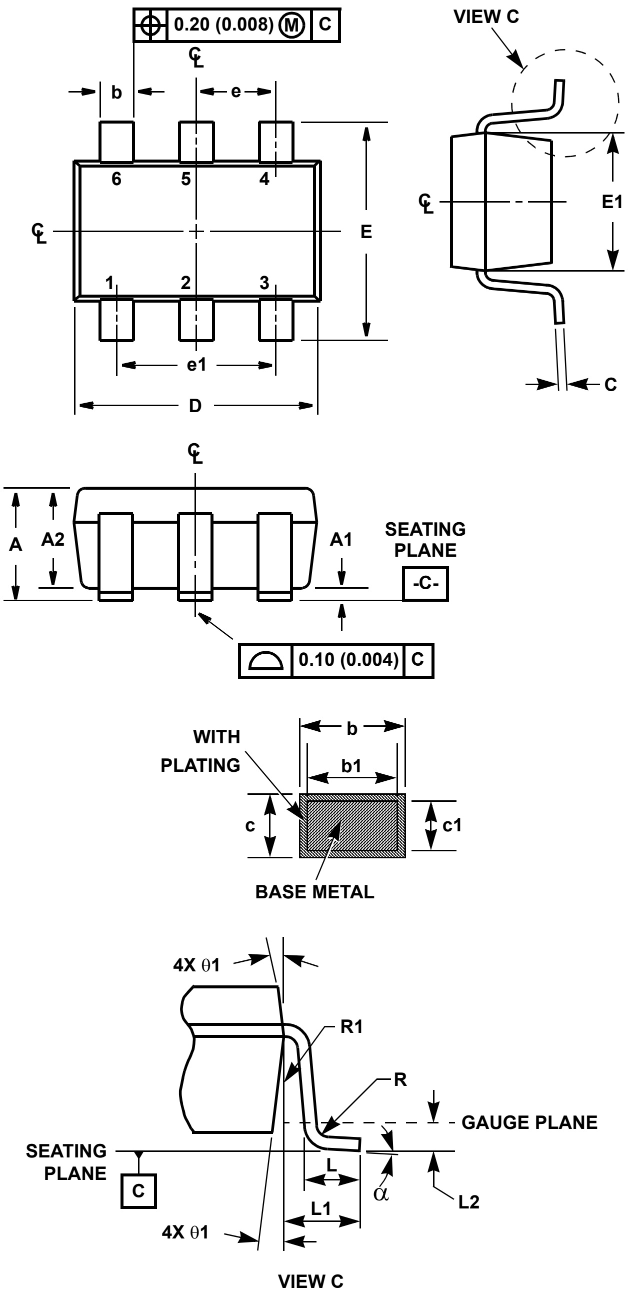


FIGURE 4. READ SEQUENCE

Small Outline Transistor Plastic Packages (SC70-6)



SC70-6

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.00	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.071	0.087	1.80	2.20	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		
L2	0.006 BSC		0.15 BSC		
N	6		6		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	
α	0°	8°	0°	8°	-

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO203AB.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

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