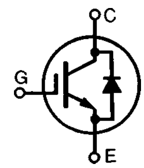
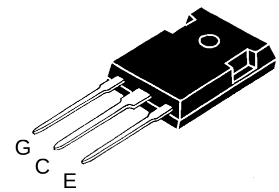
IXYS

Low $V_{CE(sat)}$ IGBT with Diode
High speed IGBT with Diode
Combi Packs

	V_{CES}	I_{C25}	$V_{CE(sat)}$
IXGH10N60U1	600 V	20 A	2.5 V
IXGH10N60AU1	600 V	20 A	3.0 V



TO-247 AD



G = Gate, C = Collector,
E = Emitter, TAB = Collector

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	T_J = 25°C to 150°C	600	V
V_{CGR}	T_J = 25°C to 150°C; R_{GE} = 1 MΩ	600	V
V_{GES}	Continuous	±20	V
V_{GEM}	Transient	±30	V
I_{C25}	T_C = 25°C	20	A
I_{C90}	T_C = 90°C	10	A
I_{CM}	T_C = 25°C, 1 ms	40	A
SSOA (RBSOA)	V_{GE}= 15 V, T_{VJ} = 125°C, R_G = 150 Ω Clamped inductive load, L = 300 µH	I_{CM} = 20 @ 0.8 V_{CES}	A
P_C	T_C = 25°C	100	W
T_J		-55 ... +150	°C
T_{JM}		150	°C
T_{stg}		-55 ... +150	°C
M_d	Mounting torque (M3)	1.13/10	Nm/lb.in.
Weight		6	g
Maximum lead temperature for soldering 1.6 mm (0.062 in.) from case for 10 s		300	°C

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
BV_{CES}	I_C = 750 µA, V_{GE} = 0 V		600			V
$V_{GE(th)}$	I_C = 500 µA, V_{CE} = V_{GE}		2.5		5.5	V
I_{CES}	V_{CE} = 0.8 • V_{CES} V_{GE} = 0 V	T_J = 25°C T_J = 125°C			260 2.5	µA mA
I_{GES}	V_{CE} = 0 V, V_{GE} = ±20 V				±100	nA
$V_{CE(sat)}$	I_C = I_{C90}, V_{GE} = 15 V	10N60U1 10N60AU1			2.5 3.0	V V

Features

- International standard package JEDEC TO-247 AD
- IGBT and anti-parallel FRED in one package
- 2nd generation HDMOS™ process
- Low $V_{CE(sat)}$
  - for low on-state conduction losses
- MOS Gate turn-on
  - drive simplicity
- Fast Recovery Epitaxial Diode FRED)
  - soft recovery with low I_{RM}

Applications

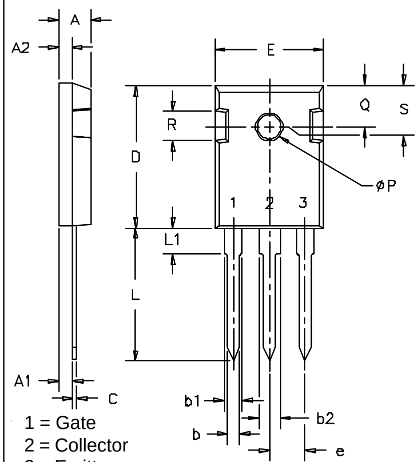
- AC motor speed control
- DC servo and robot drives
- DC choppers
- Uninterruptible power supplies (UPS)
- Switch-mode and resonant-mode power supplies

Advantages

- Space savings (two devices in one package)
- Easy to mount with 1 screw (isolated mounting screw hole)
- Reduces assembly time and cost

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
g_{fs}	$I_C = I_{C90}$; V_{CE} = 10 V, Pulse test, t ≤ 300 µs, duty cycle ≤ 2 %		4	8		S
C_{ies}	V_{CE} = 25 V, V_{GE} = 0 V, f = 1 MHz			750		pF
C_{oes}				125		pF
C_{res}				30		pF
Q_g	$I_C = I_{C90}$, V_{GE} = 15 V, V_{CE} = 0.5 V_{CES}			50	70	nC
Q_{ge}				15	25	nC
Q_{gc}				25	45	nC
$t_{d(on)}$	**Inductive load, T_J = 25°C**			100		ns
t_{ri}	$I_C = I_{C90}$, V_{GE} = 15 V, L = 100 µH			200		ns
E_{on}	V_{CE} = 0.8 V_{CES}, $R_G = R_{off}$ = 150 Ω			0.4		mJ
$t_{d(off)}$	Switching times may increase			600		ns
t_{fi}	for V_{CE} (Clamp) > 0.8 • V_{CES},	10N60AU1		300		ns
E_{off}	higher T_J or increased R_G	10N60AU1		0.6		mJ
$t_{d(on)}$				100		ns
t_{ri}	**Inductive load, T_J = 125°C**			200		ns
E_{on}	$I_C = I_{C90}$, V_{GE} = 15 V, L = 100 µH			1		mJ
$t_{d(off)}$	V_{CE} = 0.8 V_{CES}, $R_G = R_{off}$ = 150 Ω			900	1500	ns
t_{fi}		10N60U1		570	2000	ns
	Switching times may increase	10N60AU1		360	600	ns
E_{off}	for V_{CE} (Clamp) > 0.8 • V_{CES},	10N60U1		2.0		mJ
	higher T_J or increased R_G	10N60AU1		1.2		mJ
R_{thJC}					1.25	K/W
R_{thCK}				0.25		K/W

TO-247 AD Outline



1 = Gate
2 = Collector
3 = Emitter
Tab = Collector

SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.185	.209	4.7	5.3
A_1	.087	.102	2.2	2.54
A_2	.059	.098	2.2	2.6
b	.040	.055	1.0	1.4
b_1	.065	.084	1.65	2.13
b_2	.113	.123	2.87	3.12
C	.016	.031	.4	.8
D	.819	.845	20.80	21.46
E	.610	.640	15.75	16.26
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1		.177		4.50
øP	.140	.144	3.55	3.65
Q	.212	.244	5.4	6.2
R	.170	.216	4.32	5.49
S	.242 BSC		6.15 BSC	

Reverse Diode (FRED)

Symbol	Test Conditions		Characteristic Values (T_J = 25°C, unless otherwise specified) min.	typ.	max.	
V_F	$I_F = I_{C90}$, V_{GE} = 0 V, Pulse test, t ≤ 300 µs, duty cycle d ≤ 2 %				1.75	V
I_{RM}	$I_F = I_{C90}$, V_{GE} = 0 V, -di_F/dt = 64 A/µs			2.5		A
t_{rr}	V_R = 360 V	T_J = 100°C		165		ns
	I_F = 1 A; -di/dt = 50 A/µs; V_R = 30 V	T_J = 25°C		35	50	ns
R_{thJC}					2.5	K/W

Fig. 1 Saturation Characteristics

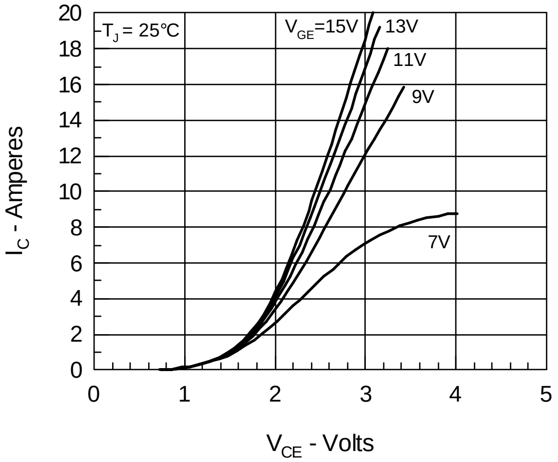


Fig. 2 Output Characterstics

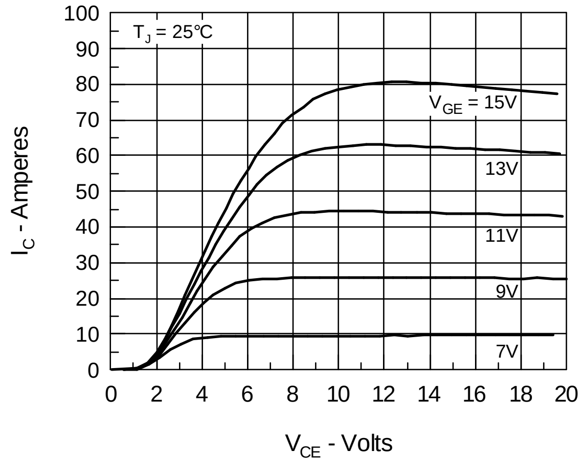


Fig. 3 Collector-Emitter Voltage vs. Gate-Emitter Voltage

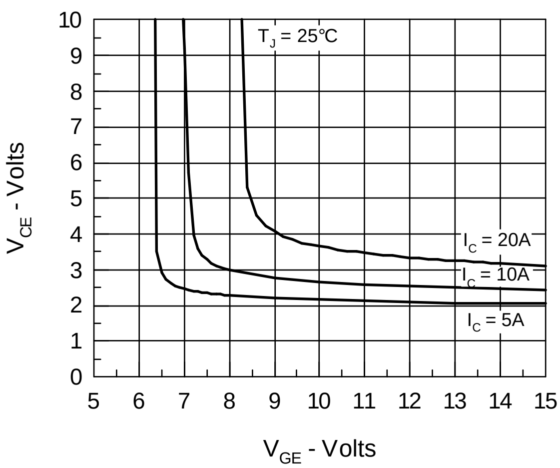


Fig. 4 Temperature Dependence of Output Saturation Voltage

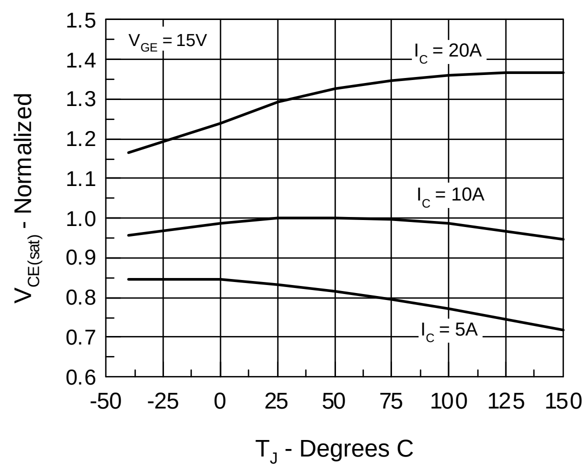


Fig. 5 Input Admittance

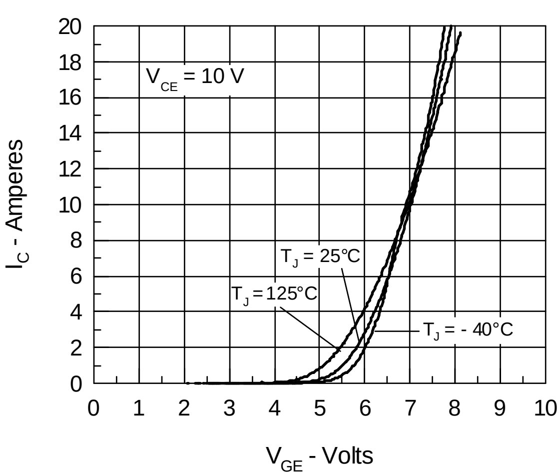


Fig. 6 Temperature Dependence of Breakdown and Threshold Voltage

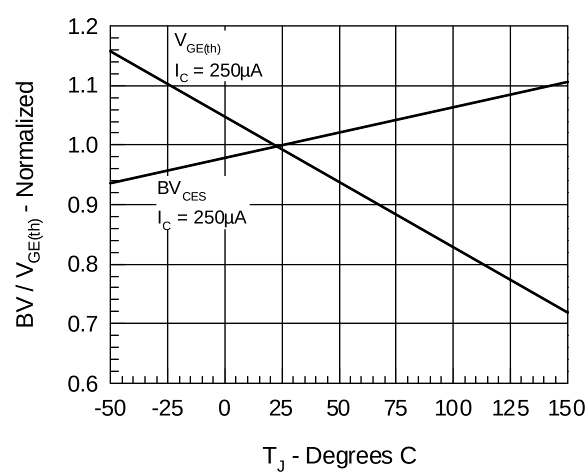


Fig.7 Gate Charge

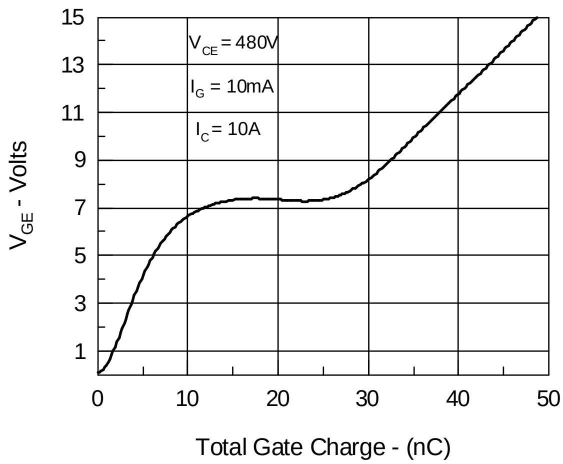


Fig.8 Turn-Off Safe Operating Area

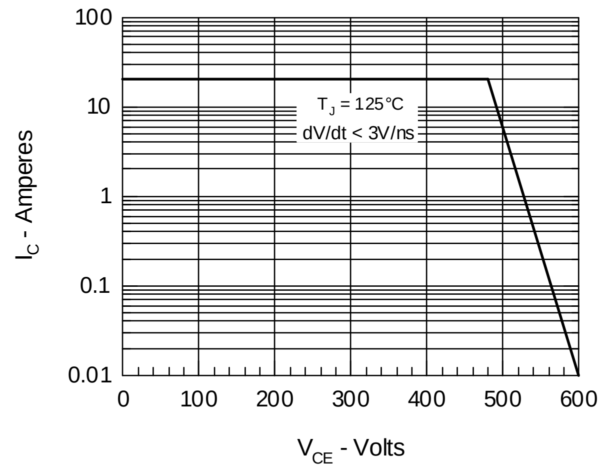


Fig.9 Capacitance Curves

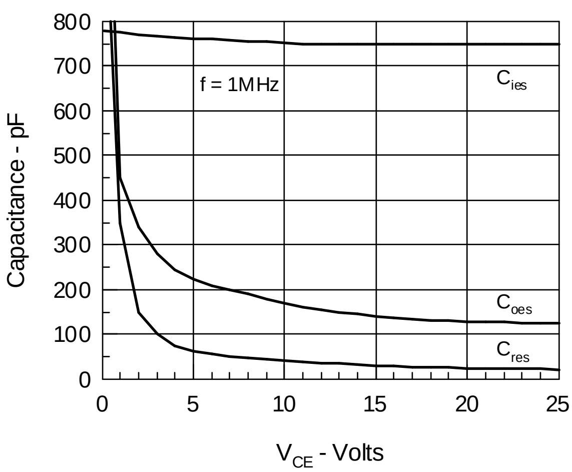


Fig.10 Transient Thermal Impedance

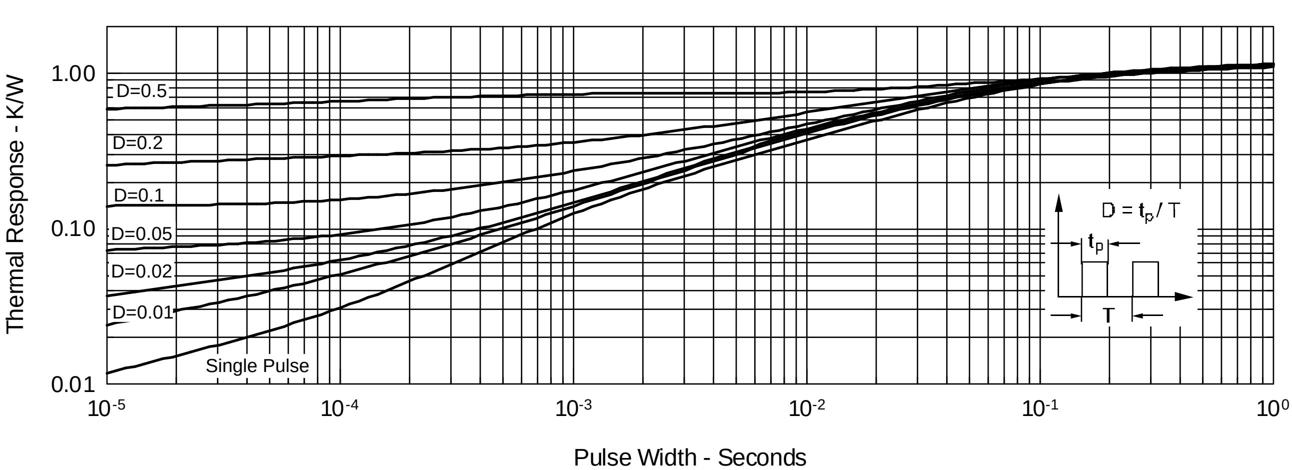


Fig.11 Maximum Forward Voltage Drop

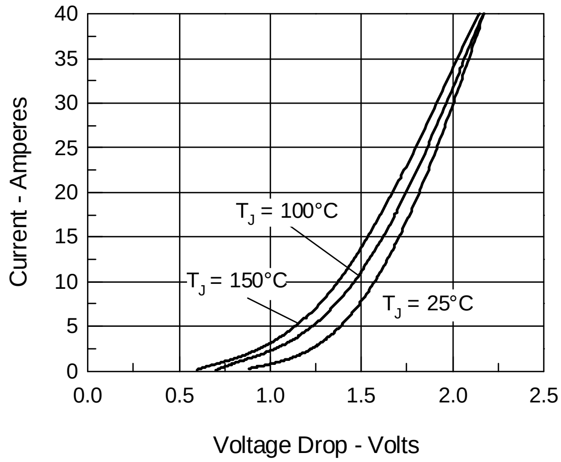


Fig.12 Peak Forward Voltage V_{FR} and Forward Recovery Time t_{FR}

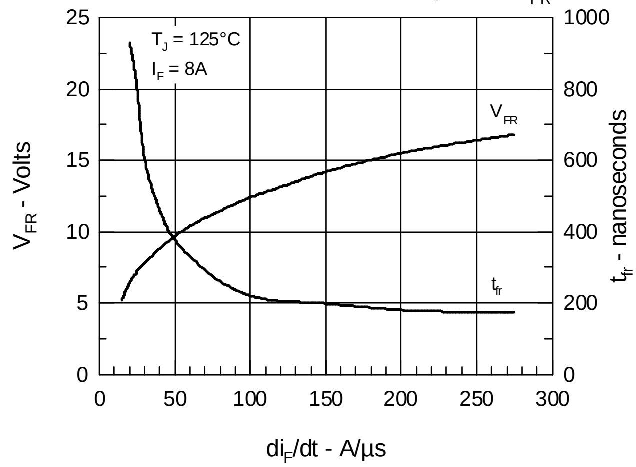


Fig.13 Junction Temperature Dependence off I_{RM} and Q_r

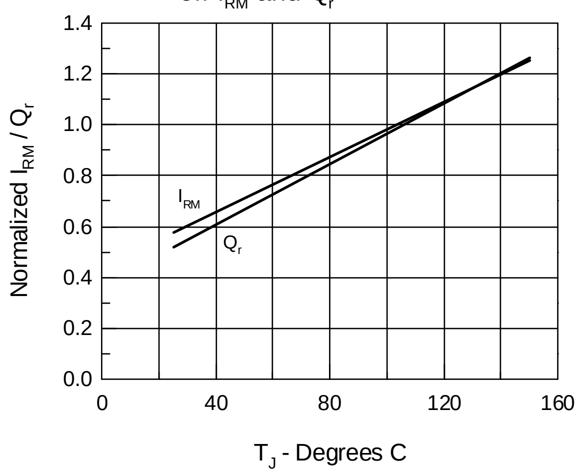


Fig.14 Reverse Recovery Charge

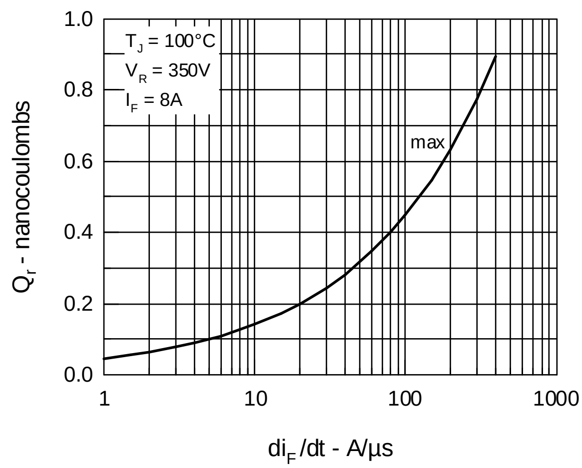


Fig.15 Peak Reverse Recovery Current

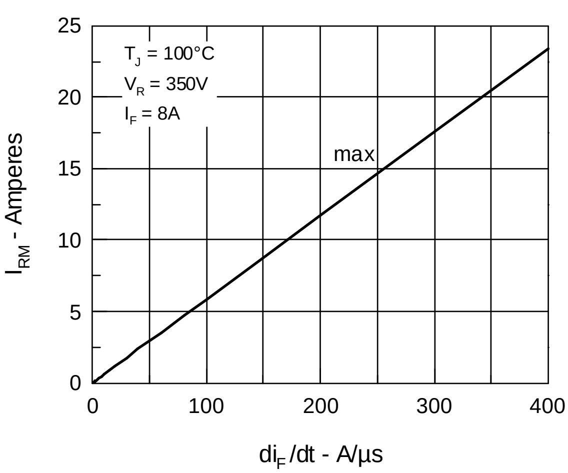


Fig.16 Reverse Recovery Time

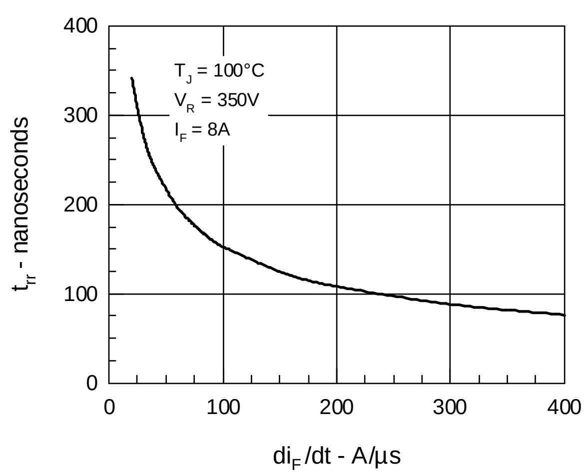


Fig.17 Diode Transient Thermal resistance junction to case