

# IN74LV244

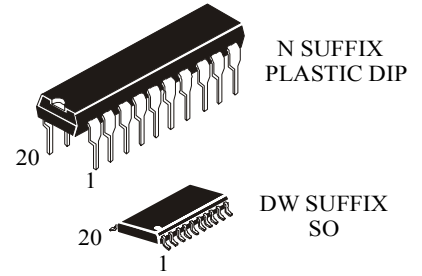
## OCTAL BUFFER/LINE DRIVER 3-STATE

The IN74LV244 is a low-voltage Si-gate CMOS device and is pin and function compatible with IN74HC/HCT244.

The IN74LV244 is an octal non-inverting buffer/line driver with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{1OE}$  and  $\overline{2OE}$ . A HIGH on  $\overline{nOE}$  causes the outputs to assume a high impedance OFF-state.

The IN74LV244 is identical to the IN74LV240 but has non-inverting outputs.

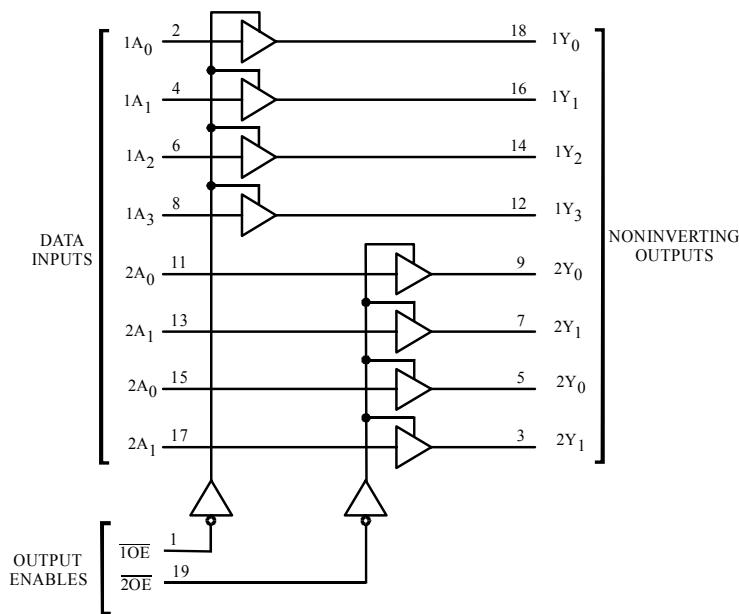
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 1.2 to 3.6 V
- Low Input Current: 1.0  $\mu$ A, 0.1  $\mu$ A at T = 25 °C
- Output Current: 8 mA at  $V_{CC} = 3.0$  V
- High Noise Immunity Characteristic of CMOS Devices



### ORDERING INFORMATION

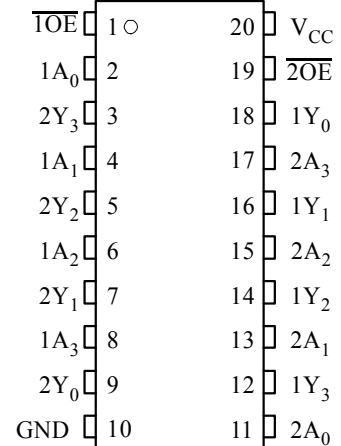
**IN74LV244N** Plastic DIP  
**IN74LV244DW** SOIC  
**IZ74LV244** chip  
 $T_A = -40^\circ$  to  $125^\circ$  C for all packages

### LOGIC DIAGRAM



PIN 20 =  $V_{CC}$   
 PIN 10 = GND

### PIN ASSIGNMENT



### FUNCTION TABLE

Input		OUTPUT
$\overline{nOE}$	nAn	nYn
L	L	L
L	H	H
H	X	Z

H= high level  
 L = low level  
 X = don't care  
 Z = high impedance

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### MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
$V_{CC}$	DC supply voltage	-0.5 to +5.0	V
$I_{IK}^{*1}$	DC Input diode current	$\pm 20$	mA
$I_{OK}^{*2}$	DC Output diode current	$\pm 50$	mA
$I_O^{*3}$	DC Output source or sink current	$\pm 35$	mA
$I_{CC}$	DC $V_{CC}$ current	$\pm 70$	mA
$I_{GND}$	DC GND current	$\pm 70$	mA
$P_D$	Power dissipation per package: <sup>*4</sup> Plastic DIP SO	750 500	mW
$T_{stg}$	Storage Temperature	-65 to +150	°C
$T_L$	Lead Temperature, 1.5 mm (Plastic DIP Package), 0.3 mm (SO Package) from Case for 4 Seconds	260	°C

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

\*<sup>1</sup>  $V_I < -0.5\text{ V}$  or  $V_I > V_{CC} + 0.5\text{ V}$ .

\*<sup>2</sup>  $V_O < -0.5\text{ V}$  or  $V_O > V_{CC} + 0.5\text{ V}$ .

\*<sup>3</sup>  $-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$ .

\*<sup>4</sup> Derating - Plastic DIP: - 12 mW/°C from 70° to 125°C

SO Package: : - 8 mW/°C from 70° to 125°C

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	1.2	3.6	V
$V_I$	Input Voltage	0	$V_{CC}$	V
$V_O$	Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-40	+125	°C
$t_r, t_f$	Input Rise and Fall Time (Figure 1)			
	$V_{CC} = 1.2\text{ V}$	0	1000	ns
	$V_{CC} = 2.0\text{ V}$	0	700	
	$V_{CC} = 3.0\text{ V}$	0	500	
	$V_{CC} = 3.6\text{ V}$	0	400	

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{IN}$  and  $V_{OUT}$  should be constrained to the range  $GND \leq (V_{IN} \text{ or } V_{OUT}) \leq V_{CC}$ .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

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## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test conditions	V <sub>CC</sub> V	Guaranteed Limit						Unit		
				25°C		-40°C to 85°C		125°C				
				min	max	min	max	min	max			
V <sub>IH</sub>	HIGH level input voltage		1.2	0.9	-	0.9	-	0.9	-	V		
			2.0	1.4	-	1.4	-	1.4	-			
			3.0	2.1	-	2.1	-	2.1	-			
			3.6	2.5	-	2.5	-	2.5	-			
V <sub>IL</sub>	LOW level input voltage		1.2	-	0.3	-	0.3	-	0.3	V		
			2.0	-	0.6	-	0.6	-	0.6			
			3.0	-	0.9	-	0.9	-	0.9			
			3.6	-	1.1	-	1.1	-	1.1			
V <sub>OH</sub>	HIGH level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -50 μA	1.2	1.1	-	1.0	-	1.0	-	V		
			2.0	1.92	-	1.9	-	1.9	-			
			3.0	2.92	-	2.9	-	2.9	-			
			3.6	3.52	-	3.5	-	3.5	-			
				V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = -8 mA	3.0	2.48	-	2.34	-	2.20	-	V
V <sub>OL</sub>	LOW level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 50 μA	1.2	-	0.09	-	0.1	-	0.1	V		
			2.0	-	0.09	-	0.1	-	0.1			
			3.0	-	0.09	-	0.1	-	0.1			
			3.6	-	0.09	-	0.1	-	0.1			
				V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> I <sub>O</sub> = 8 mA	3.0	-	0.33	-	0.4	-	0.5	V
I <sub>I</sub>	Input current	V <sub>I</sub> = V <sub>CC</sub> or 0 V	*	-	±0.1	-	±1.0	-	±1.0	μA		
I <sub>OZ</sub>	Three state leakage current	3-state outputs V <sub>I</sub> (01,19) = V <sub>IH</sub> V <sub>O</sub> = V <sub>CC</sub> or 0 V	1.2 *	-	±0.5	-	±5	-	±10	μA		
I <sub>CC</sub>	Supply current	V <sub>I</sub> = V <sub>CC</sub> or 0 V I <sub>O</sub> = 0 μA	*	-	8.0	-	80	-	160	μA		

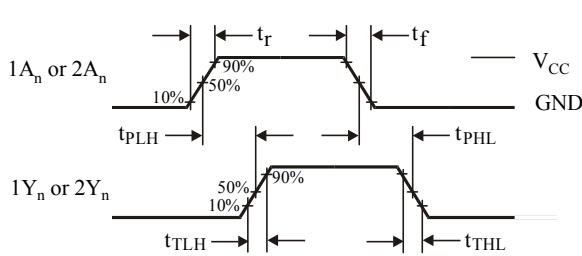
\* V<sub>CC</sub> = 3.3 ± 0.3 V

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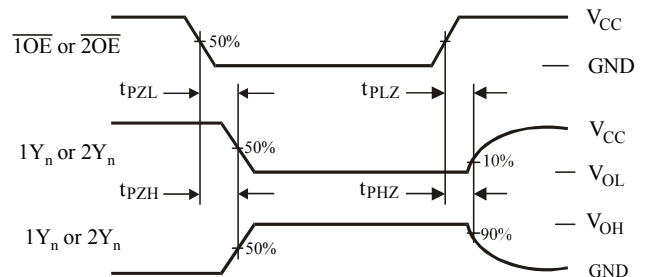
## AC ELECTRICAL CHARACTERISTICS ( $C_L=50$ pF, $t_r=t_f=6.0$ ns)

Symbol	Parameter	Test conditions	$V_{CC}$ V	Guaranteed Limit						Unit
				25°C		-40°C to 85°C		125°C		
				min	max	min	max	min	max	
$t_{PHL}, t_{PLH}$	Propagation delay, $1A_n$ to $1Y_n$ , $2A_n$ to $2Y_n$	$V_I = 0$ V or $V_{CC}$ Figure 1 and 3	1.2 2.0 *	- 100 -	100 24 15	- - -	125 30 19	- - -	150 36 23	ns
$t_{PHZ}, t_{PLZ}$	Propagation delay, $\overline{1OE}$ to $1Y_n$ , $\overline{2OE}$ to $2Y_n$	$V_I = 0$ V or $V_{CC}$ Figure 2 and 4	1.2 2.0 *	- 140 -	140 30 20	- - -	175 35 24	- - -	210 41 28	ns
$t_{PZH}, t_{PZL}$	Propagation delay, $\overline{1OE}$ to $1Y_n$ , $\overline{2OE}$ to $2Y_n$	$V_I = 0$ V or $V_{CC}$ Figure 2 and 4	1.2 2.0 *	- 140 -	140 32 20	- - -	175 40 25	- - -	210 48 30	ns
$t_{THL}, t_{TLH}$	Output Transition Time, Any Output	$V_I = 0$ V or $V_{CC}$ Figure 1 and 3	1.2 2.0 *	- 60 -	60 16 10	- - -	75 20 13	- - -	90 24 15	ns
$C_I$	Input capacitance		3.0	-	7.0	-	7.0	-	7.0	pF
$C_{PD}$	Power dissipation capacitance (per one channel)	$V_I = 0$ V or $V_{CC}$		-	50	-	-	-	-	pF

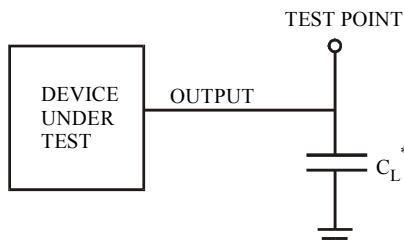
\*  $V_{CC} = 3.3 \pm 0.3$  V



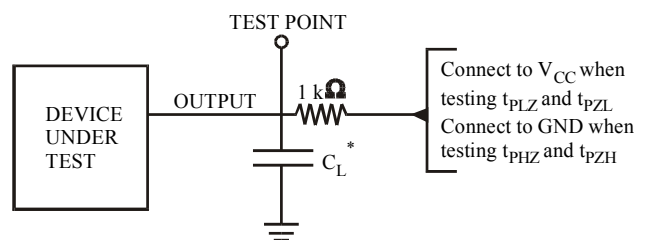
**Figure 1. Switching Waveforms**



**Figure 2. Switching Waveforms**



\* Includes all probe and jig capacitance  
**Figure 3. Test Circuit**



\* Includes all probe and jig capacitance  
**Figure 4. Test Circuit**