

Document Title

**64Kx16 Bit High-Speed CMOS Static RAM(5.0V Operating).
Operated at Commercial and Industrial Temperature Ranges.**

Revision History

<u>Rev.No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>										
Rev. 0.0	Initial release with preliminary.	Aug. 5. 1998	Preliminary										
Rev. 1.0	Relax DC characteristics.	Sep. 7. 1998	Preliminary										
	<table border="1"> <thead> <tr> <th>Item</th> <th>Previous</th> <th>Changed</th> </tr> </thead> <tbody> <tr> <td rowspan="3">Icc</td> <td>12ns</td> <td>90mA</td> </tr> <tr> <td>15ns</td> <td>88mA</td> </tr> <tr> <td>20ns</td> <td>85mA</td> </tr> </tbody> </table>	Item	Previous	Changed	Icc	12ns	90mA	15ns	88mA	20ns	85mA		
Item	Previous	Changed											
Icc	12ns	90mA											
	15ns	88mA											
	20ns	85mA											
Rev. 2.0	Add 48-fine pitch BGA.	Sep. 17. 1998	Preliminary										
Rev. 2.1	Changed device part name for FP-BGA.	Nov. 5. 1998	Final										
	<table border="1"> <thead> <tr> <th>Item</th> <th>Previous</th> <th>Changed</th> </tr> </thead> <tbody> <tr> <td>Symbol</td> <td>Z</td> <td>F</td> </tr> </tbody> </table> ex) K6R1016C1C-Z -> K6R1016C1C-F	Item	Previous	Changed	Symbol	Z	F						
Item	Previous	Changed											
Symbol	Z	F											
Rev. 2.2	Changed device ball name for FP-BGA.	Dec. 10. 1998	Final										
	<table border="1"> <thead> <tr> <th>Previous</th> <th>Changed</th> </tr> </thead> <tbody> <tr> <td>I/O1 ~ I/O8</td> <td>I/O9 ~ I/O16</td> </tr> <tr> <td>I/O9 ~ I/O16</td> <td>I/O1 ~ I/O8</td> </tr> </tbody> </table>	Previous	Changed	I/O1 ~ I/O8	I/O9 ~ I/O16	I/O9 ~ I/O16	I/O1 ~ I/O8						
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Rev. 3.0	Added Data Retention Characteristics.	Mar. 3. 1999	Final										
Rev. 3.1	Add 10ns part.	Mar. 3. 2000	Final										
Rev. 4.0	Delete 20ns speed bin	Sep.24. 2001	Final										

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

64K x 16 Bit High-Speed CMOS Static RAM

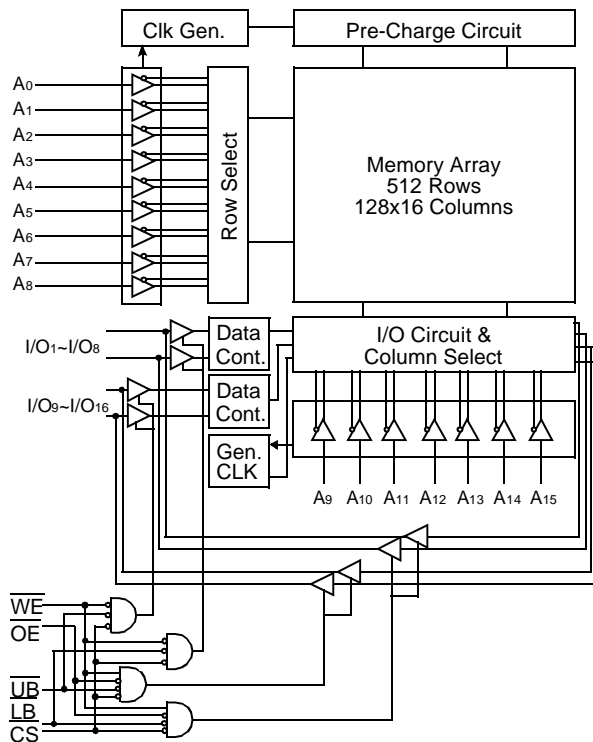
FEATURES

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
 - Standby (TTL) : 30mA(Max.)
 - (CMOS) : 5mA(Max.)
 - 0.5mA(Max.) L-ver. only
- Operating K6R1016C1C-10 : 105mA(Max.)
- K6R1016C1C-12 : 95mA(Max.)
- K6R1016C1C-15 : 93mA(Max.)
- Single 5.0V±10% Power Supply
- TTL Compatible Inputs and Outputs
- I/O Compatible with 3.3V Device
- Fully Static Operation
 - No Clock or Refresh required
- Three State Outputs
- 2V Minimum Data Retention: L-ver. only
- Center Power/Ground Pin Configuration
- Data Byte Control: \overline{LB} : I/O₁~ I/O₈, \overline{UB} : I/O₉~ I/O₁₆
- Standard Pin Configuration:
 - K6R1016C1C-J : 44-SOJ-400
 - K6R1016C1C-T : 44-TSOP2-400BF
 - K6R1016C1C-F : 48-Fine pitch BGA with 0.75 Ball pitch

GENERAL DESCRIPTION

The K6R1016C1C is a 1,048,576-bit high-speed Static Random Access Memory organized as 65,536 words by 16 bits. The K6R1016C1C uses 16 common input and output lines and has at output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control (\overline{UB} , \overline{LB}). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R1016C1C is packaged in a 400mil 44-pin plastic SOJ or TSOP2 forward or 48-Fine pitch BGA.

FUNCTIONAL BLOCK DIAGRAM



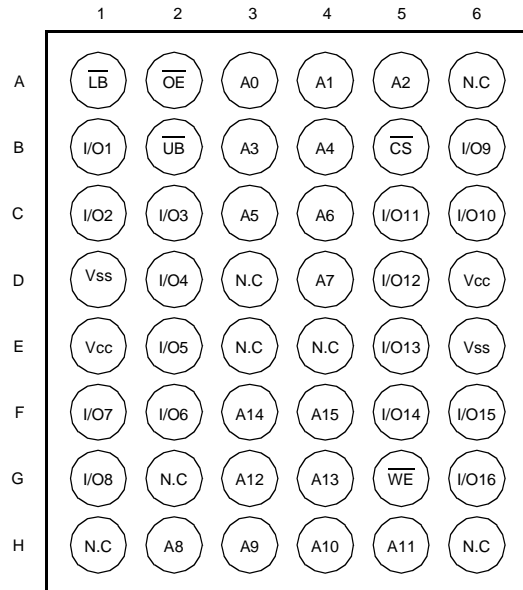
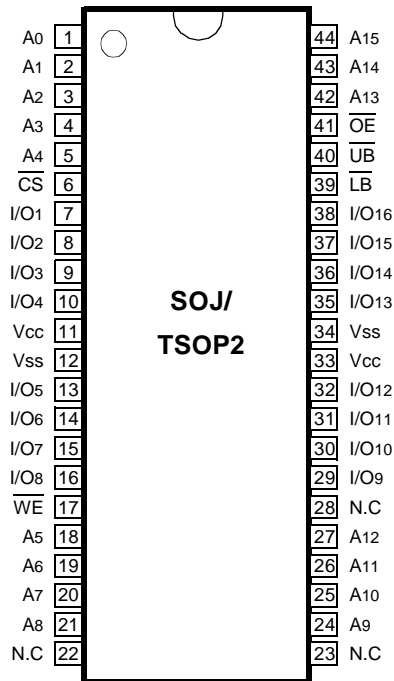
ORDERING INFORMATION

K6R1016C1C-C10/C12/C15	Commercial Temp.
K6R1016C1C-I10/I12/I15	Industrial Temp.

PIN FUNCTION

Pin Name	Pin Function
A ₀ - A ₁₅	Address Inputs
\overline{WE}	Write Enable
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{LB}	Lower-byte Control(I/O ₁ ~I/O ₈)
\overline{UB}	Upper-byte Control(I/O ₉ ~I/O ₁₆)
I/O ₁ ~ I/O ₁₆	Data Inputs/Outputs
V _{cc}	Power(+5.0V)
V _{ss}	Ground
N.C	No Connection

PIN CONFIGURATION(TOP VIEW)



48-CSP

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Rating	Unit	
Voltage on Any Pin Relative to Vss	V _{IN} , V _{OUT}	-0.5 to V _{CC} +0.5	V	
Voltage on V _{CC} Supply Relative to Vss	V _{CC}	-0.5 to 7.0	V	
Power Dissipation	P _d	1	W	
Storage Temperature	T _{STG}	-65 to 150	°C	
Operating Temperature	Commercial	T _A	0 to 70	°C
	Industrial	T _A	-40 to 85	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*(T_A= to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	-	V _{CC} +0.5***	V
Input Low Voltage	V _{IL}	-0.5**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.

** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

*** V_{IH}(Max) = V_{CC} + 2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS* (TA=0 to 70°C, VCC=5.0V±10%, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit	
Input Leakage Current	ILI	VIN=VSS to VCC	-2	2	μA	
Output Leakage Current	ILO	CS=VIH or OE=VIH or WE=VIL VOUT=VSS to VCC	-2	2	μA	
Operating Current	ICC	Min. Cycle, 100% Duty CS=VIL, VIN = VIH or VIL, IOUT=0mA	10ns	-	105	mA
			12ns	-	95	
			15ns	-	93	
Standby Current	ISB	Min. Cycle, CS=VIH	-	30	mA	
	ISB1	f=0MHz, CS ≥ VCC-0.2V, VIN ≥ VCC-0.2V or VIN ≤ 0.2V	Normal	5		mA
			L-Ver.	0.5		
Output Low Voltage Level	VOL	IOL=8mA	-	0.4	V	
Output High Voltage Level	VOH	Ioh=-4mA	2.4	-	V	
	VOH1**	Ioh1=-0.1mA	-	3.95	V	

* The above parameters are also guaranteed at industrial temperature range.

** VCC=5.0V±5%, Temp.=25°C

CAPACITANCE* (TA=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C _{I/O}	V _{I/O} =0V	-	8	pF
Input Capacitance	C _{IN}	V _{IN} =0V	-	6	pF

* Capacitance is sampled and not 100% tested.

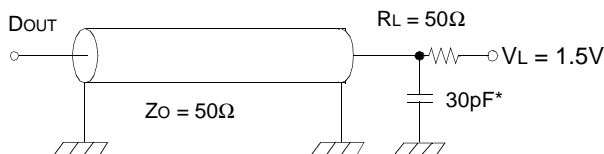
AC CHARACTERISTICS (TA=0 to 70°C, VCC=5.0V±10%, unless otherwise noted.)

TEST CONDITIONS*

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

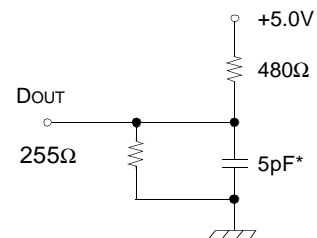
* The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



* Capacitive Load consists of all components of the test environment.

* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R1016C1C-10		K6R1016C1C-12		K6R1016C1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	10	-	12	-	15	ns
Chip Select to Output	t _{CO}	-	10	-	12	-	15	ns
Output Enable to Valid Output	t _{OE}	-	5	-	6	-	7	ns
\overline{UB} , \overline{LB} Access Time	t _{BA}	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t _{LZ}	3	-	3	-	3	-	ns
\overline{UB} , \overline{LB} Enable to Low-Z Output	t _{BLZ}	0	-	0	-	0	-	ns
Output Enable to Low-Z Output	t _{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t _{HZ}	0	5	0	6	-	7	ns
Output Disable to High-Z Output	t _{OZH}	0	5	0	6	-	7	ns
\overline{UB} , \overline{LB} Disable to High-Z Output	t _{BHZ}	0	5	0	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	ns
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	0	-	ns
Chip Selection to Power DownTime	t _{PD}	-	10	-	12	-	15	ns

* The above parameters are also guaranteed at industrial temperature range.

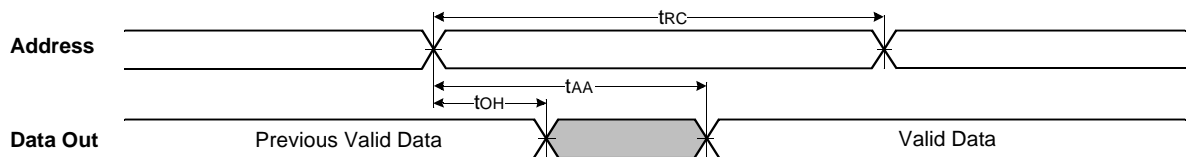
WRITE CYCLE*

Parameter	Symbol	K6R1016C10-12		K6R1016C1C-12		K6R1016C1C-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	10	-	12	-	15	-	ns
Chip Select to End of Write	t _{CW}	7	-	8	-	9	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t _{AW}	7	-	8	-	9	-	ns
Write Pulse Width(\overline{OE} High)	t _{WP}	7	-	8	-	9	-	ns
Write Pulse Width(\overline{OE} Low)	t _{WP1}	10	-	12	-	15	-	ns
\overline{UB} , \overline{LB} Valid to End of Write	t _{BW}	7	-	8	-	9	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t _{WHZ}	0	5	0	6	0	7	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	ns
Data Hold from Write Time	t _{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t _{OW}	3	-	3	-	3	-	ns

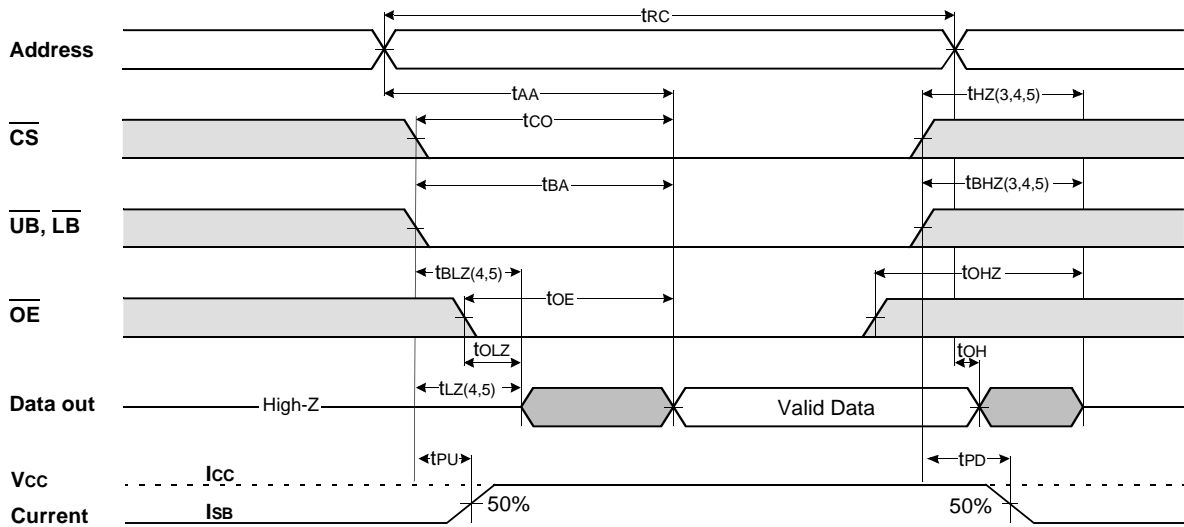
* The above parameters are also guaranteed at industrial temperature range.

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}=\overline{OE}=V_{IL}$, $\overline{WE}=V_{IH}$, \overline{UB} , $\overline{LB}=V_{IL}$)



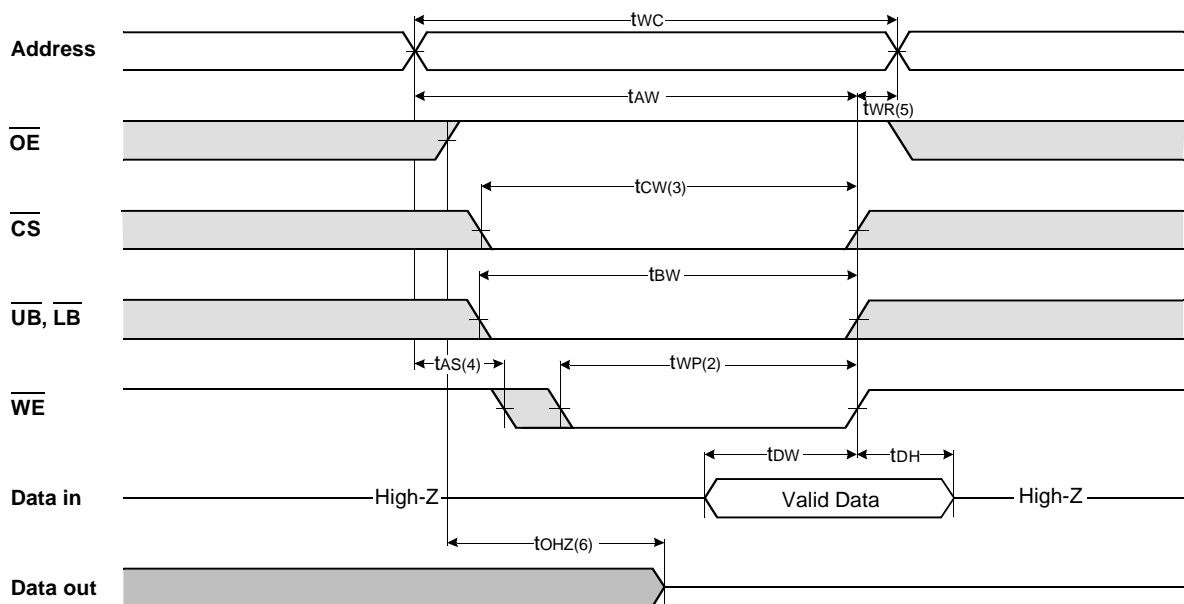
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



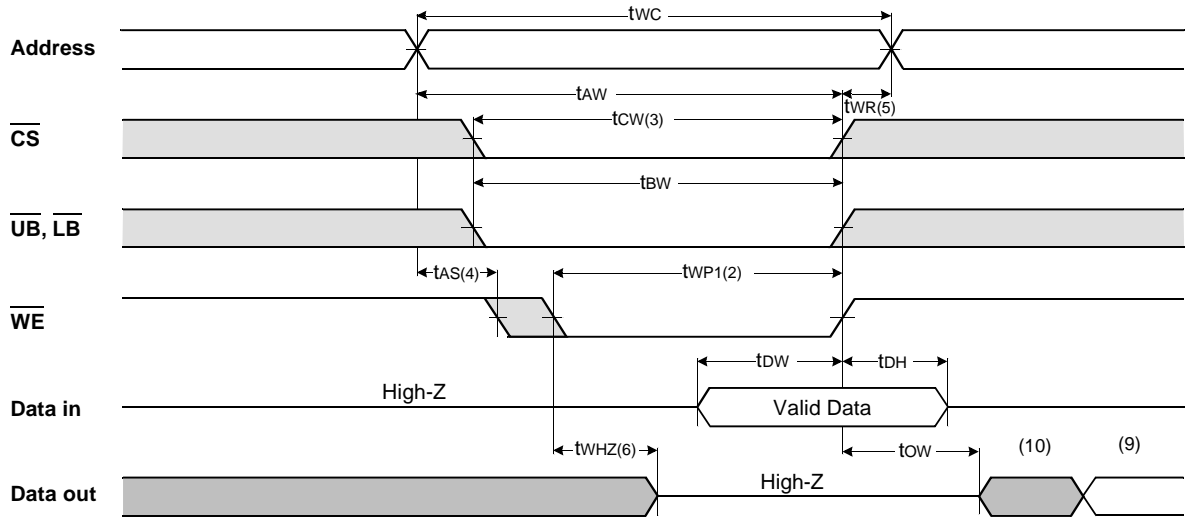
NOTES(READ CYCLE)

1. \overline{WE} is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device.
5. Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}=V_{IL}$.
7. Address valid prior to coincident with \overline{CS} transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

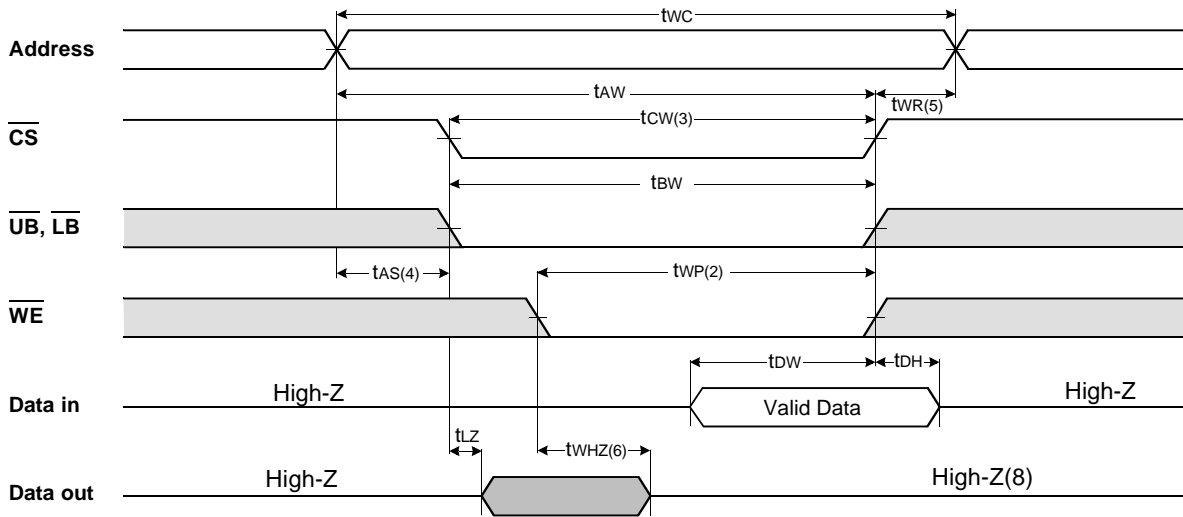
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}=\text{Clock}$)



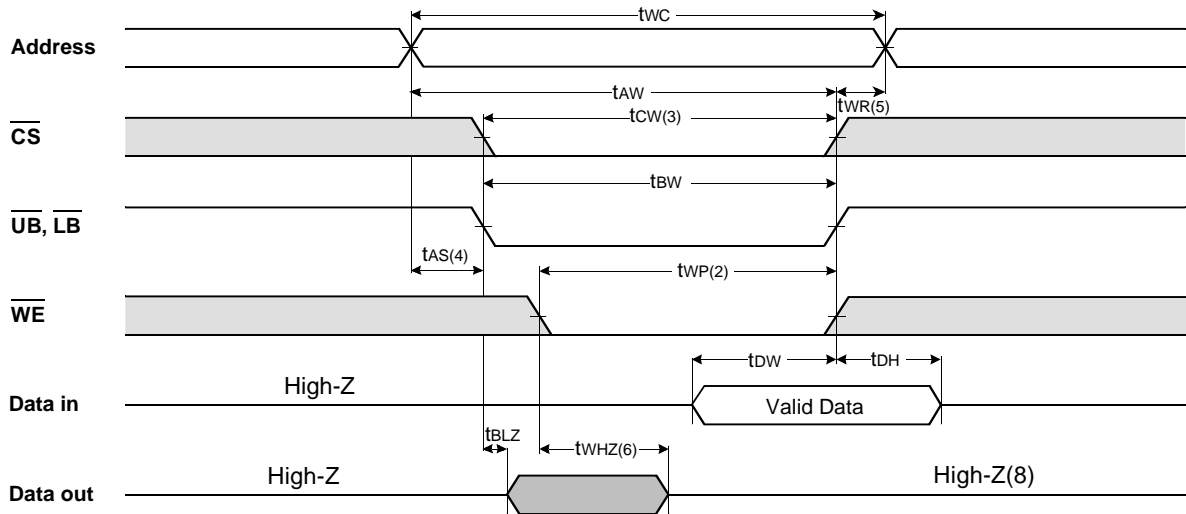
TIMING WAVEFORM OF WRITE CYCLE(2) (\overline{OE} =Low fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) (\overline{CS} =Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) (\overline{UB} , \overline{LB} Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low CS, WE, LB and UB. A write begins at the latest transition CS going low and WE going low; A write ends at the earliest transition CS going high or WE going high. tWP is measured from the beginning of write to the end of write.
3. tcw is measured from the later of CS going low to end of write.
4. tAS is measured from the address valid to the beginning of write.
5. tWR is measured from the end of write to the address change. tWR applied in case a write ends as CS or WE going high.
6. If OE, CS and WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If CS goes low simultaneously with WE going or after WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When CS is low: I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

FUNCTIONAL DESCRIPTION

\overline{CS}	\overline{WE}	\overline{OE}	\overline{LB}	\overline{UB}	Mode	I/O Pin		Supply Current
						I/O1~I/O8	I/O9~I/O16	
H	X	X*	X	X	Not Select	High-Z	High-Z	ISB, ISB1
L	H	H	X	X	Output Disable	High-Z	High-Z	Icc
L	X	X	H	H	Read	DOUT	High-Z	Icc
L	H	L	L	H		High-Z	DOUT	
L	H	L	L	L		DOUT	DOUT	
L	L	X	L	H	Write	DIN	High-Z	Icc
L	L	X	H	L		High-Z	DIN	
L	L	X	L	L		DIN	DIN	

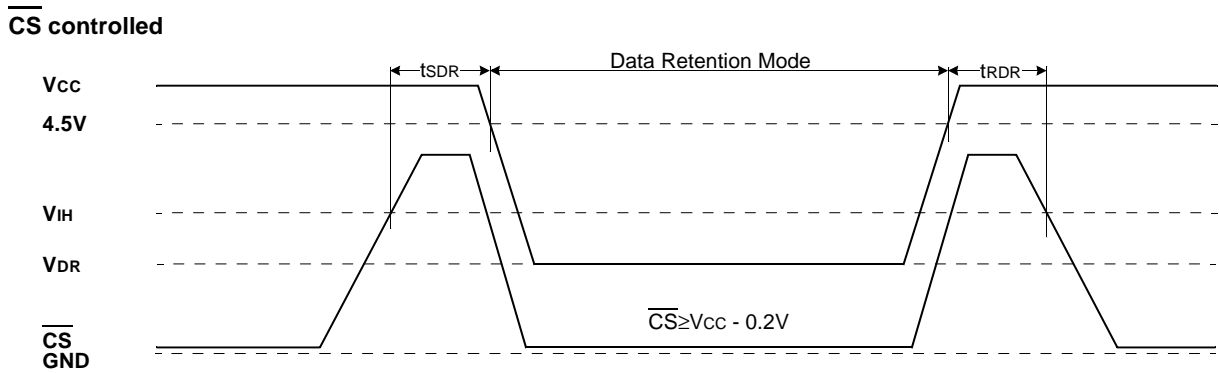
* X means Don't Care.

DATA RETENTION CHARACTERISTICS*(TA=0 to 70°C)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Vcc for Data Retention	VDR	$\overline{CS} \geq V_{CC} - 0.2V$	2.0	-	5.5	V
Data Retention Current	IDR	$V_{CC} = 3.0V, \overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.4	mA
		$V_{CC} = 2.0V, \overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	-	-	0.3	
Data Retention Set-Up Time	tSDR	See Data Retention Wave form(below)	0	-	-	ns
Recovery Time	tRDR	See Data Retention Wave form(below)	5	-	-	ms

* The above parameters are also guaranteed at industrial temperature range.
Data Retention Characteristic is for L-ver only.

DATA RETENTION WAVE FORM



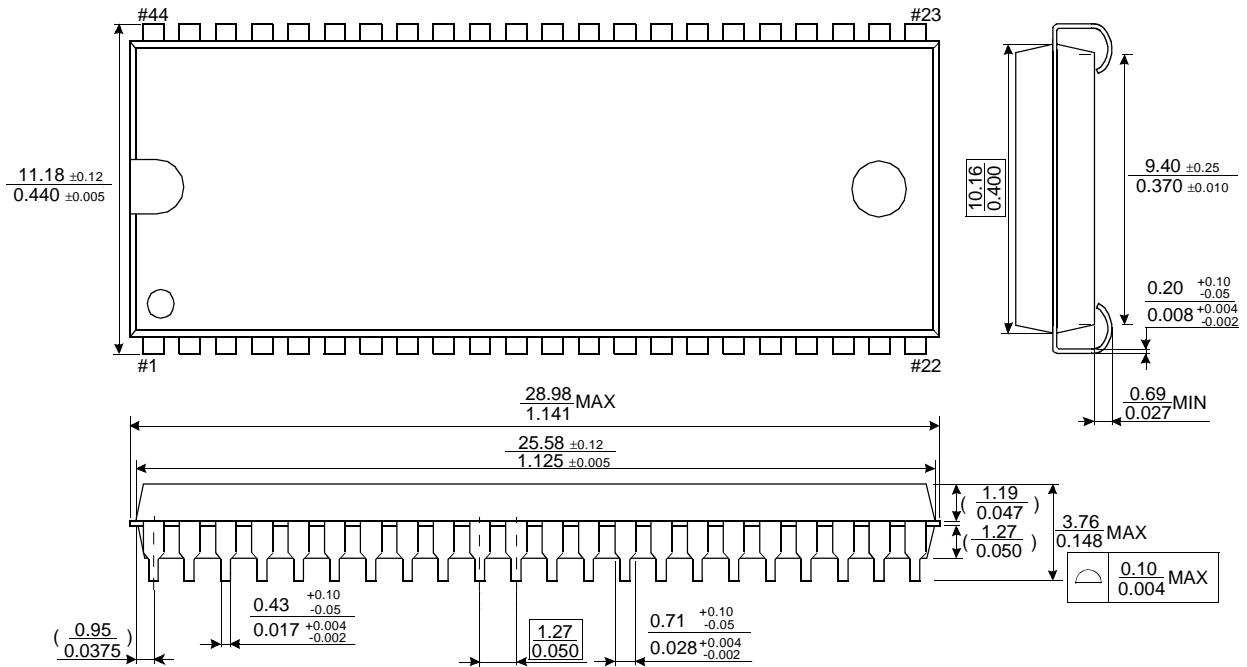
K6R1016C1C-C/C-L, K6R1016C1C-I/C-P

CMOS SRAM

PACKAGE DIMENSIONS

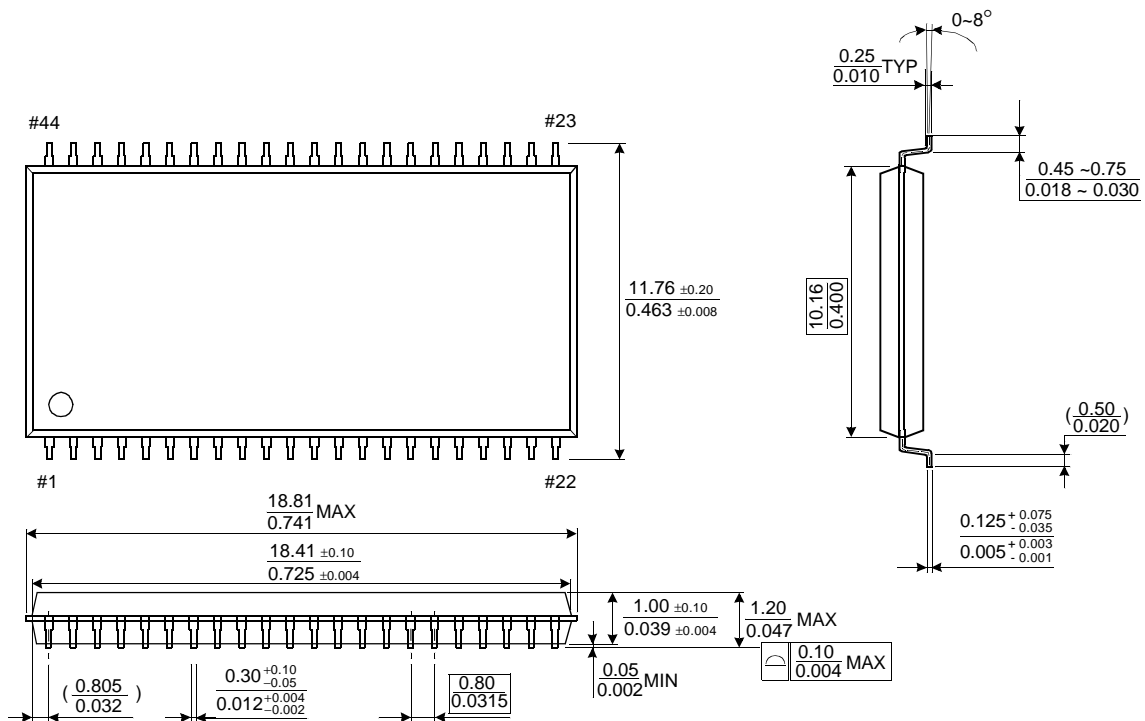
Units: millimeters/Inches

44-SOJ-400



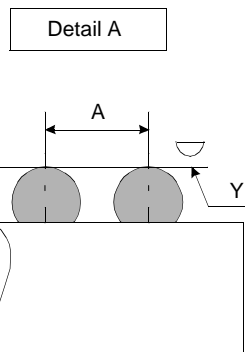
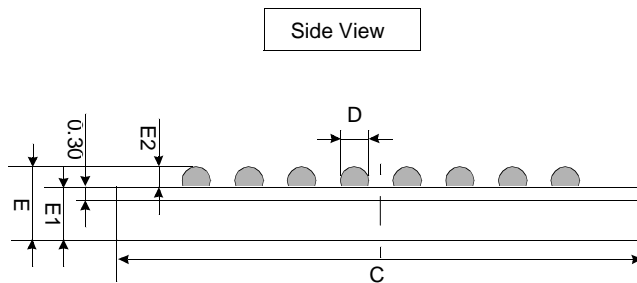
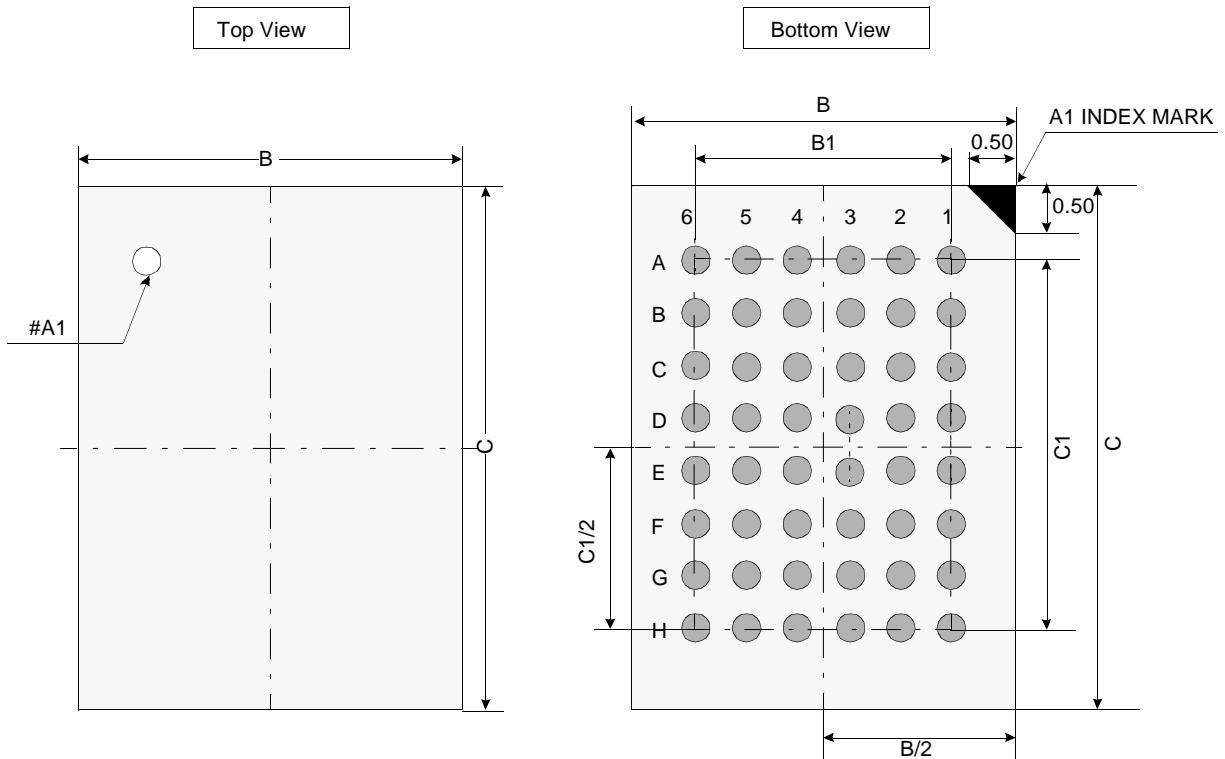
44-TSOP2-400BF

Units: millimeters/Inches



PACKAGE OUTLINE

(Units : millimeter)



	Min	Typ	Max
A	-	0.75	-
B	5.90	6.00	6.10
B1	-	3.75	-
C	6.90	7.00	7.10
C1	-	5.25	-
D	0.30	0.35	0.40
E	-	1.05	1.20
E1	-	0.80	-
E2	0.20	0.25	0.30
Y	-	-	0.08

- Notes.**
1. Bump counts: 48(8row x 6column)
 2. Bump pitch : (x,y)=(0.75 x 0.75)(typ.)
 3. All tolerance are +/-0.050 unless otherwise specified.
 4. Typ : Typical
 5. Y is coplanarity: 0.08(Max)