Document Title

128Kx24 Bit High-Speed CMOS Static RAM(3.3V Operating)
Operated at Commercial and Industrial Temperature Ranges.

Revision History

Rev.No.	History	Draft Data	Remark
Rev. 0.0	Design-In Specification	Dec. 05. 2000	Design-In
Rev. 0.1	Pin Configurations Modified (page 2) Add Timing Diagram page 6 ~ 8)	Mar. 07. 2001	Preliminary
Rev. 0.2	Modified Read Cycle Timing(2)	April. 04.2001	Preliminary
Rev. 0.3	1) Version change from M to D 2) Cin from 20 to 15 pF 3) Icc from 300 to 170mA for 9ns products from 270 to 150mA for 10ns products from 240 to 130mA for 12ns products 4) Isb (TTL) from 120 to 40 mA for all products (CMOS) from 30 to 15 mA for all products 5) Part number change from -9 to -09 for 9ns products	June. 23.2001	Preliminary
Rev. 0.4	Change write parameter(tDW) from 6ns to 5ns at -10	Oct. 31. 2001	Preliminary
Rev. 1.0	Final Specification Release	Dec. 19. 2001	Final

128K x 24 Bit High-Speed CMOS Static RAM(3.3V Operating)

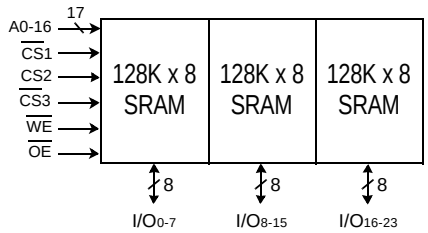
FEATURES

- Fast Access Time 9,10,12ns
- Power Dissipation
  Standby (TTL) : 40mA(Max.)
  (CMOS) : 15mA(Max.)
  Operating K6R3024V1D-09 : 170mA(Max.)
  K6R3024V1D-10 : 150mA(Max.)
  K6R3024V1D-12 : 130mA(Max.)
  Single 3.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Center Power/Ground Pin Configuration
- 119(7x17)Pin Ball Grid Array Package(14mmx22mm)
- Operating in Commercial and Industrial Temperature range.

GENERAL DESCRIPTION

The K6R3024V1D is a 3,145,728-bit high-speed Static Random Access Memory organized as 131,072 words by 24 bits. The K6R3024V1D uses 24 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The K6R3024V1D is a three megabit static RAM constructed on an multilayer laminate sub-strate using three 3.3V, 128K x 8 static RAMS encapsulated in a Ball Grid Array(BGA).

FUNCTIONAL BLOCK DIAGRAM



PIN FUNCTION

Pin Name	Pin Function
A_0 - A_{16}	Addresses Inputs
$\overline{WE}$	Write Enable
$\overline{CS_1}$,CS_2,$\overline{CS_3}$	Chip Select
$\overline{OE}$	Output Enable
I/O_0 ~ I/O_{23}	Data Inputs/Outputs
V_{CC}	Power(+3.3v)
V_{SS}	Ground
NC	No Connection

ORDERING INFORMATION

K6R3024V1D-HC09/HC10/HC12	Commercial Temp.
K6R3024V1D-HI09/HI10/HI12	Industrial Temp.

PIN CONFIGURATIONS(TOP VIEW)

K6R3024V1D

	1	2	3	4	5	6	7
A	NC	A	A	A	A	A	NC
B	NC	A	A	$\overline{CS_1}$	A	A	NC
C	I/O	NC	CS_2	NC	$\overline{CS_3}$	NC	I/O
D	I/O	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O
E	I/O	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	I/O
F	I/O	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O
G	I/O	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	I/O
H	I/O	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O
J	V_{CC}	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	V_{CC}
K	I/O	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O
L	I/O	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	I/O
M	I/O	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O
N	I/O	V_{SS}	V_{CC}	V_{SS}	V_{CC}	V_{SS}	I/O
P	I/O	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	I/O
R	I/O	NC	NC	NC	NC	NC	I/O
T	NC	A	A	$\overline{WE}$	A	A	NC
U	NC	A	A	$\overline{OE}$	A	A	NC

ABSOLUTE MAXIMUM RATINGS*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{IN}, V_{OUT}	-0.5 to 4.6	V
Voltage on V_{CC} Supply Relative to V_{SS}		V_{CC}	-0.5 to 4.6	V
Power Dissipation		P_d	2	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C

***** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_3}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
H	X	X	X	X	Standby	High-Z	Standby
X	L	X	X	X	Standby	High-Z	Standby
X	X	H	X	X	Standby	High-Z	Standby
L	H	L	L	H	Read	$DATA_{OUT}$	Active
L	H	L	X	L	Write	$DATA_{IN}$	Active
L	H	L	H	H	Outputs Disabled	High-Z	Active

RECOMMENDED DC OPERATING CONDITIONS*(T_A=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	-	V_{CC}+0.3***	V
Input Low Voltage	V_{IL}	-0.3**	-	0.8	V

* The above parameters are also guaranteed at industrial temperature range.
** V_{IL}(Min) = -2.0V a.c(Pulse Width ≤ 8ns) for I ≤ 20mA.
*** V_{IH}(Max) = V_{CC} + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA.

DC AND OPERATING CHARACTERISTICS*(T_A=0 to 70°C, Vcc=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-	6	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=V_{SS} to V_{CC}		-	2	μA
Operating Current	I_{CC}	Min. Cycle, 100% Duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IH} or V_{IL}, I_{OUT}=0mA	-09	-	170	mA
			-10	-	150	mA
			-12	-	130	mA
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$=V_{IH}	-09	-	40	mA
			-10	-	40	mA
			-12	-	40	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{IN}≤0.2V	-09	-	15	mA
			-10	-	15	mA
			-12	-	15	mA
Output Low Voltage Level	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage Level	V_{OH}	I_{OH}=-4mA		2.4	-	V

* The above parameters are also guaranteed at industrial temperature range.
* $\overline{CS}$ represents $\overline{CS_1}$, CS_2 and $\overline{CS_3}$ in this data sheet. CS_2 as of opposite polarity to $\overline{CS_1}$ and $\overline{CS_3}$.

CAPACITANCE*(T_A=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	8	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	15	pF

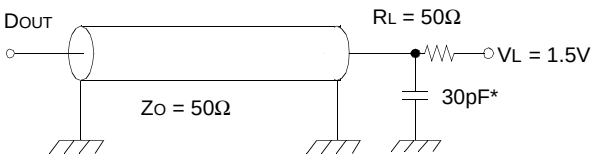
* Capacitance is sampled and not 100% tested

AC TEST CONDITIONS*(T_A=0 to 70°C, Vcc=3.3±0.3V, unless otherwise specified)

Parameter	Value
Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and output Timing Reference Levels	1.5V
Output Load	See Below

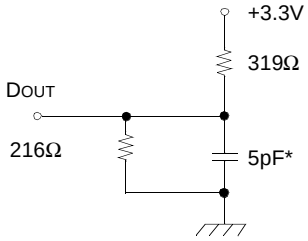
* The above parameters are also guaranteed at industrial temperature range.

Output Loads(A)



* Capacitive Load consists of all components of the test environment.

Output Loads(B)
for t_{HZ}, t_{LZ}, t_{WHZ}, t_{OW}, t_{OLZ} & t_{OHZ}



* Including Scope and Jig Capacitance

READ CYCLE*

Parameter	Symbol	K6R3024V1D-09		K6R3024V1D-10		K6R3024V1D-12		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	9	-	10	-	12	-	ns
Address Access Time	t_{AA}	-	9	-	10	-	12	ns
Chip Select to Output	t_{CO}	-	9	-	10	-	12	ns
Output Enable to Valid Output	t_{OE}	-	4	-	5	-	6	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	4	0	5	0	6	ns
Output Disable to High-Z Output	t_{OHZ}	0	5	0	6	0	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns
Chip Select to Power-Up Time	t_{PU}	0	-	0	-	0	-	ns
Chip Deselect to Power DownTime	t_{PD}	-	9	-	10	-	12	ns

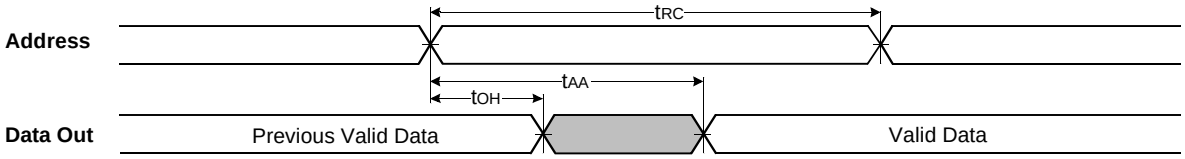
WRITE CYCLE*

Parameter	Symbol	K6R3024V1D-09		K6R3024V1D-10		K6R3024V1D-12		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	9	-	10	-	12	-	ns
Chip Select to End of Write	t_{CW}	7	-	7	-	8	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	7	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	7	-	7	-	8	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	9	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	5	0	5	0	5	ns
Data to Write Time Overlap	t_{DW}	5	-	5	-	7	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns
End Write to Output Low-Z	t_{OW}	3	-	3	-	3	-	ns

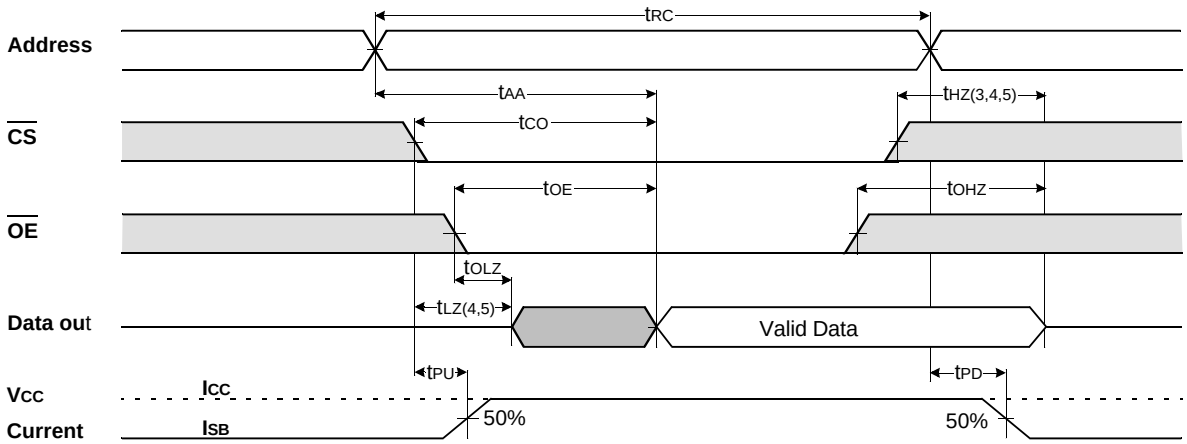
* This parameter is guaranteed by design but not tested.
These specifications are for the individual K6R3024V1D Static RAMs.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



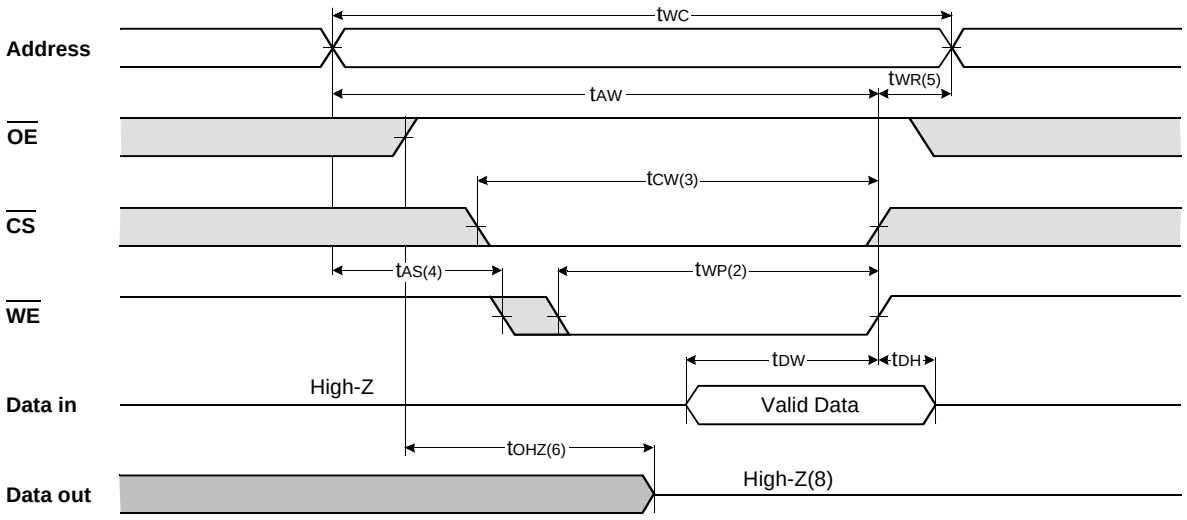
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



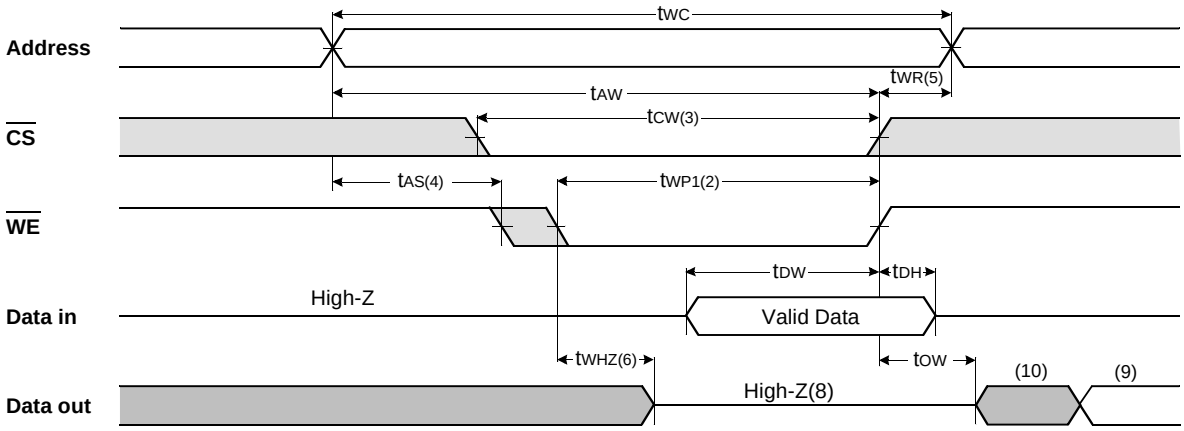
NOTES(READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$=V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
9. $\overline{CS}$ represents $\overline{CS_1}$, CS_2 and $\overline{CS_3}$ in this data sheet. CS_2 as of opposite polarity to $\overline{CS_1}$ and $\overline{CS_3}$.

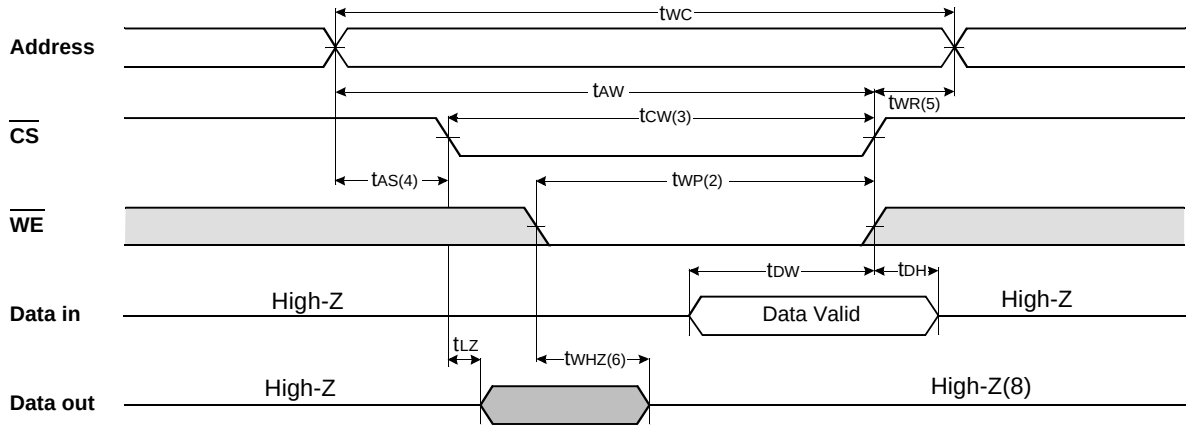
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{OE}$= Clock)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{OE}$=Low Fixed)



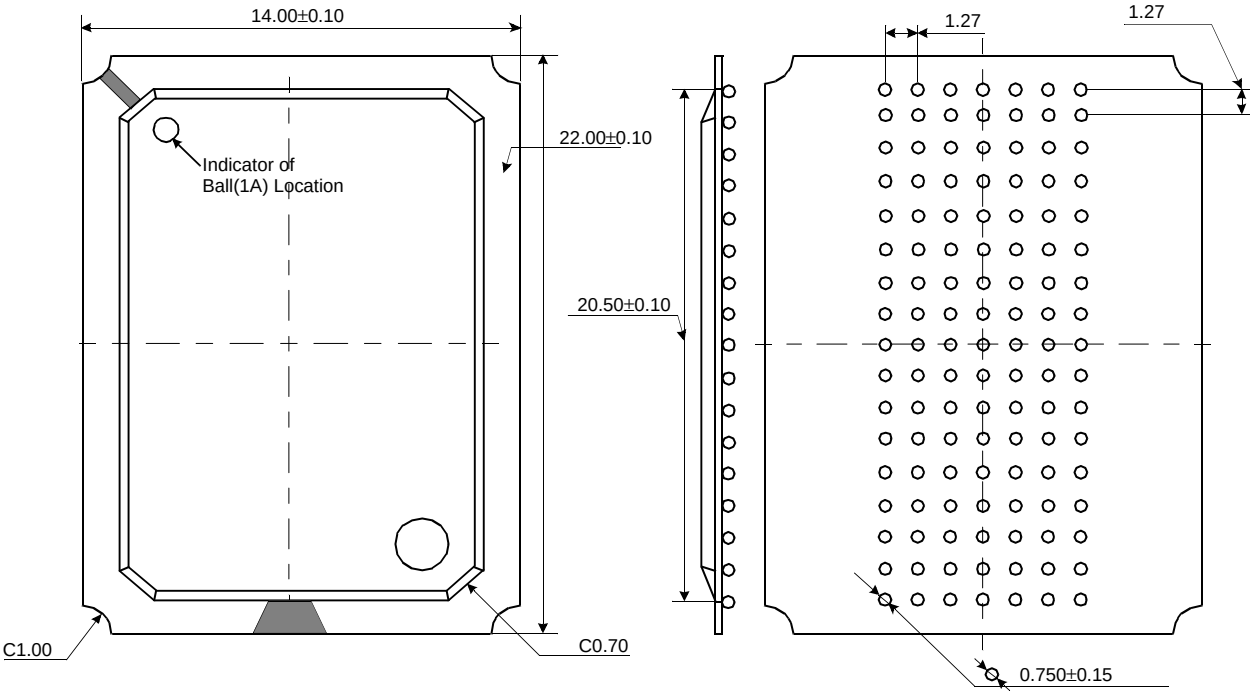
TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{CS}$ = Controlled)

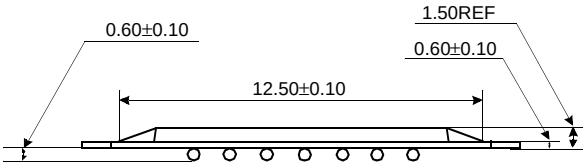


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$ and $\overline{WE}$. A write begins at the latest transition $\overline{CS}$ going low and $\overline{WE}$ going low ; A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after $\overline{WE}$ going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.
11. $\overline{CS}$ represents $\overline{CS_1}$, CS_2 and $\overline{CS_3}$ in this data sheet. CS_2 as of opposite polarity to $\overline{CS_1}$ and $\overline{CS_3}$.

119 BGA PACKAGE DIMENSIONS





NOTE :

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.