

KMM372F213CK/CS EDO Mode

2M x 72 DRAM DIMM with ECC using 2Mx8, 2K Refresh, 3.3V

GENERAL DESCRIPTION

The Samsung KMM372F213C is a 2Mx72bits Dynamic RAM high density memory module. The Samsung KMM372F213C consists of nine CMOS 2Mx8bits DRAMs in SOJ/TSOP-II 300mil package, and two 16bits driver IC in 48pin TSSOP package mounted on a 168-pin glass-epoxy substrate. A 0.1 or 0.22uF decoupling capacitor is mounted on the printed circuit board for each DRAM. The KMM372F213C is a Dual In-line Memory Module and is intended for mounting into 168-pin edge connector sockets.

PERFORMANCE RANGE

Speed	trAC	tcAC	trc	tHPC
-5	50ns	18ns	84ns	20ns
-6	60ns	20ns	104ns	25ns

FEATURES

- Part Identification
 - KMM372F213CK (2048 cycles/32ms Ref., SOJ)
 - KMM372F213CS (2048 cycles/32ms Ref., TSOP)
- Fast Page Mode with Extended Data Out Mode Operation
- \overline{CAS} -before- \overline{RAS} Refresh capability
- \overline{RAS} -only and Hidden refresh capability
- LVTTTL compatible inputs and outputs
- Single 3.3V±0.3V power supply
- JEDEC standard pinout & Buffered PDpin
- Buffered input except \overline{RAS} and DQ
- PCB : Height(1000mil), Single sided component

PIN CONFIGURATIONS

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back	Pin	Back
1	V _{ss}	29	RSVD	57	DQ22	85	V _{ss}	113	RSVD	141	DQ58		
2	DQ0	30	$\overline{RAS0}$	58	DQ23	86	DQ36	114	* $\overline{RAS1}$	142	DQ59		
3	DQ1	31	$\overline{OE0}$	59	V _{cc}	87	DQ37	115	RFU	143	V _{cc}		
4	DQ2	32	V _{ss}	60	DQ24	88	DQ38	116	V _{ss}	144	DQ60		
5	DQ3	33	A0	61	RFU	89	DQ39	117	A1	145	RFU		
6	V _{cc}	34	A2	62	RFU	90	V _{cc}	118	A3	146	RFU		
7	DQ4	35	A4	63	RFU	91	DQ40	119	A5	147	RFU		
8	DQ5	36	A6	64	RFU	92	DQ41	120	A7	148	RFU		
9	DQ6	37	A8	65	DQ25	93	DQ42	121	A9	149	DQ61		
10	DQ7	38	A10	66	DQ26	94	DQ43	122	*A11	150	DQ62		
11	DQ8	39	*A12	67	DQ27	95	DQ44	123	*A13	151	DQ63		
12	V _{ss}	40	V _{cc}	68	V _{ss}	96	V _{ss}	124	V _{cc}	152	V _{ss}		
13	DQ9	41	RFU	69	DQ28	97	DQ45	125	RFU	153	DQ64		
14	DQ10	42	RFU	70	DQ29	98	DQ46	126	B0	154	DQ65		
15	DQ11	43	V _{ss}	71	DQ30	99	DQ47	127	V _{ss}	155	DQ66		
16	DQ12	44	$\overline{OE2}$	72	DQ31	100	DQ48	128	RFU	156	DQ67		
17	DQ13	45	$\overline{RAS2}$	73	V _{cc}	101	DQ49	129	* $\overline{RAS3}$	157	V _{cc}		
18	V _{cc}	46	$\overline{CAS4}$	74	DQ32	102	V _{cc}	130	* $\overline{CAS5}$	158	DQ68		
19	DQ14	47	RSVD	75	DQ33	103	DQ50	131	RSVD	159	DQ69		
20	DQ15	48	$\overline{W2}$	76	DQ34	104	DQ51	132	PDE	160	DQ70		
21	DQ16	49	V _{cc}	77	DQ35	105	DQ52	133	V _{cc}	161	DQ71		
22	DQ17	50	RSVD	78	V _{ss}	106	DQ53	134	RSVD	162	V _{ss}		
23	V _{ss}	51	RSVD	79	PD1	107	V _{ss}	135	RSVD	163	PD2		
24	RSVD	52	DQ18	80	PD3	108	RSVD	136	DQ54	164	PD4		
25	RSVD	53	DQ19	81	PD5	109	RSVD	137	DQ55	165	PD6		
26	V _{cc}	54	V _{ss}	82	PD7	110	V _{cc}	138	V _{ss}	166	PD8		
27	$\overline{W0}$	55	DQ20	83	ID0	111	RFU	139	DQ56	167	ID1		
28	$\overline{CAS0}$	56	DQ21	84	V _{cc}	112	* $\overline{CAS1}$	140	DQ57	168	V _{cc}		

PIN NAMES

Pin Names	Function
A0, B0, A1 - A10	Address Input
DQ0 - DQ71	Data In/Out
$\overline{W0}$, $\overline{W2}$	Read/Write Enable
\overline{OE} , $\overline{OE2}$	Output Enable
$\overline{RAS0}$, $\overline{RAS2}$	Row Address Strobe
$\overline{CAS0}$, $\overline{CAS4}$	Column Address Strobe
V _{cc}	Power(+3.3V)
V _{ss}	Ground
NC	No Connection
PDE	Presence Detect Enable
PD1 - 8	Presence Detect
ID0 - 1	ID bit
RSVD	Reserved Use
RFU	Reserved for Future Use

Pins marked "*" are not used in this module.

PD & ID Table

Pin	50NS	60NS
PD1	1	1
PD2	0	0
PD3	0	0
PD4	1	1
PD5	1	1
PD6	0	1
PD7	0	1
PD8	0	0
ID0	0	0
ID1	0	0

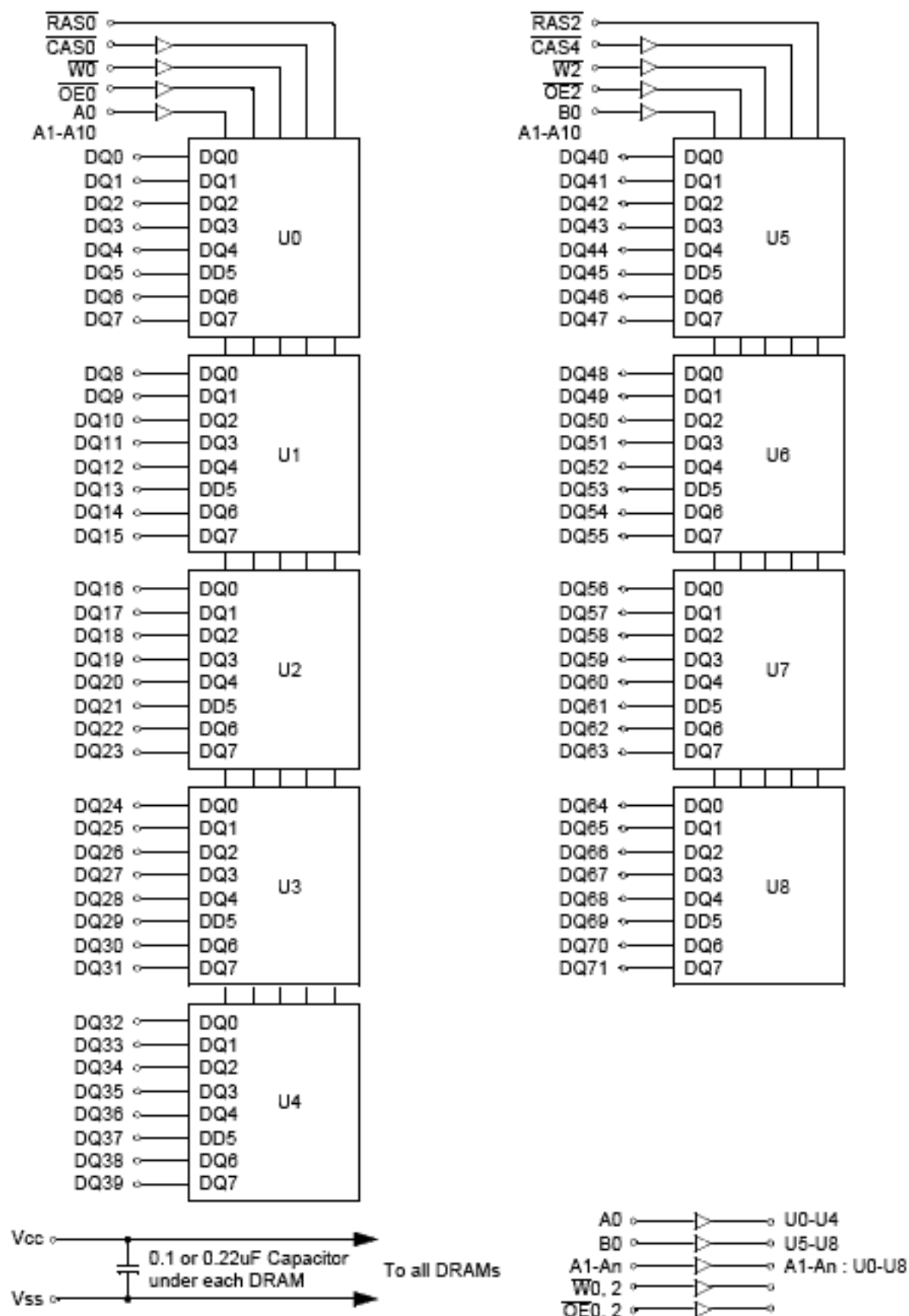
PD Note : PD & ID Terminals must each be pulled up through a resistor to V_{cc} at the next higher level assembly. PDs will be either open (NC) or driven to V_{ss} via on-board buffer circuits.

ID Note : IDs will be either open (NC) or connected directly to V_{ss} without a buffer.

PD : 0 for Vol of Drive IC & 1 for N.C

ID : 0 for V_{ss} & 1 for N.C

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Rating	Unit
Voltage on any pin relative V _{SS}	V _{IN} , V _{OUT}	-0.5 to +4.6	V
Voltage on V _{CC} supply relative to V _{SS}	V _{CC}	-0.5 to +4.6	V
Storage Temperature	T _{stg}	-55 to +125	°C
Power Dissipation	P _D	9	W
Short Circuit Output Current	I _{OS}	50	mA

* Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for intended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage referenced to V_{SS}, T_A = 0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V _{CC}	3.0	3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.0	-	V _{CC} +0.3 ^{*1}	V
Input Low Voltage	V _{IL}	-0.3 ^{*2}	-	0.8	V

*1 : V_{CC}+1.3V/15ns, Pulse width is measured at V_{CC}.

*2 : -1.3V/15ns, Pulse width is measured at V_{SS}.

DC AND OPERATING CHARACTERISTICS (Recommended operating conditions unless otherwise noted)

Symbol	Speed	KMM372F213CK/CS		Unit
		Min	Max	
I _{CC1}	-5	-	990	mA
	-6	-	900	mA
I _{CC2}	Don't care	-	100	mA
I _{CC3}	-5	-	990	mA
	-6	-	900	mA
I _{CC4}	-5	-	810	mA
	-6	-	720	mA
I _{CC5}	Don't care	-	30	mA
I _{CC6}	-5	-	990	mA
	-6	-	900	mA
I _{I(L)}	Don't care	-25	25	uA
I _{O(L)}		-5	5	uA
V _{OH}	Don't care	2.4	-	V
V _{OL}		-	0.4	V

I_{CC1}* : Operating Current * (\overline{RAS} , \overline{CAS} , Address cycling @trc=min)

I_{CC2} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{IH}$)

I_{CC3}* : \overline{RAS} Only Refresh Current * ($\overline{CAS}=V_{IH}$, \overline{RAS} cycling @trc=min)

I_{CC4}* : EDO Mode Current * ($\overline{RAS}=V_{IL}$, \overline{CAS} cycling : tHPC=min)

I_{CC5} : Standby Current ($\overline{RAS}=\overline{CAS}=\overline{W}=V_{CC}-0.2V$)

I_{CC6}* : \overline{CAS} -Before- \overline{RAS} Refresh Current * (\overline{RAS} and \overline{CAS} cycling @trc=min)

I_{I(L)} : Input Leakage Current (Any input $0 \leq V_{IN} \leq V_{CC}+0.3V$, all other pins not under test=0 V)

I_{O(L)} : Output Leakage Current(Data Out is disabled, $0V \leq V_{OUT} \leq V_{CC}$)

V_{OH} : Output High Voltage Level (I_{OH} = -2mA)

V_{OL} : Output Low Voltage Level (I_{OL} = 2mA)

* **NOTE** : I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependent on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as an average current. In I_{CC1} and I_{CC3}, address can be changed maximum once while $\overline{RAS}=V_{IL}$. In I_{CC4}, address can be changed maximum once within one hyper page mode cycle, tHPC.

CAPACITANCE (TA = 25°C, VCC=3.3V, f = 1MHz)

Item	Symbol	Min	Max	Unit
Input capacitance[A0-A10, B0]	CIN1	-	20	pF
Input capacitance[$\overline{W0}$, $\overline{W2}$, $\overline{OE0}$, $\overline{OE2}$]	CIN2	-	20	pF
Input capacitance[$\overline{RAS0}$, $\overline{RAS2}$]	CIN3	-	45	pF
Input capacitance[$\overline{CAS0}$, $\overline{CAS4}$]	CIN4	-	20	pF
Input/Output capacitance[DQ0 - 71]	CDQ1	-	20	pF

AC CHARACTERISTICS (0°C≤TA≤70°C, VCC=3.3V±0.3V. See notes 1,2.)

Test condition : VIH/VIL=2.0/0.8V, VOH/VOL=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Random read or write cycle time	tRC	84		104		ns	
Read-modify-write cycle time	tRWC	131		155		ns	
Access time from \overline{RAS}	tRAC		50		60	ns	3,4,10
Access time from \overline{CAS}	tCAC		18		20	ns	3,4,5,14
Access time from column address	tAA		30		35	ns	3,10,14
\overline{CAS} to output in Low-Z	tCLZ	8		8		ns	3,14
\overline{OE} to output in Low-Z	tOLZ	8		8		ns	3,14
Output buffer turn-off delay from \overline{CAS}	tCEZ	8	18	8	20	ns	6,11,12,14
Transition time(rise and fall)	tT	2	50	2	50	ns	2
\overline{RAS} precharge time	tRP	30		40		ns	
\overline{RAS} pulse width	tRAS	50	10K	60	10K	ns	
\overline{RAS} hold time	tRSH	18		20		ns	14
\overline{CAS} hold time	tCSH	36		43		ns	14
\overline{CAS} pulse width	tCAS	8	10K	10	10K	ns	13
\overline{RAS} to \overline{CAS} delay time	tRCD	18	32	18	40	ns	4,14
\overline{RAS} to column address delay time	tRAD	13	20	13	25	ns	10,14
\overline{CAS} to \overline{RAS} precharge time	tCRP	10		10		ns	14
Row address set-up time	tASR	5		5		ns	14
Row address hold time	tRAH	8		8		ns	14
Column address set-up time	tASC	0		0		ns	
Column address hold time	tCAH	8		10		ns	
Column address to \overline{RAS} lead time	tRAL	30		35		ns	14
Read command set-up time	tRCS	0		0		ns	
Read command hold time referenced to \overline{CAS}	tRCH	0		0		ns	8
Read command hold time referenced to \overline{RAS}	tRRH	-2		-2		ns	8,14
Write command hold time	tWCH	10		10		ns	
Write command pulse width	tWP	10		10		ns	
Write command to \overline{RAS} lead time	tRWL	18		20		ns	14
Write command to \overline{CAS} lead time	tCWL	8		10		ns	
Data set-up time	tDS	-2		-2		ns	9,14
Data hold time	tDH	13		15		ns	9,14
Refresh period(2K Ref.)	tREF		32		32	ms	
Write command set-up time	tWCS	0		0		ns	7
\overline{CAS} to \overline{W} delay time	tCWD	36		40		ns	7
\overline{RAS} to \overline{W} delay time	tRWD	71		83		ns	7,14

AC CHARACTERISTICS (0°C≤T_A≤70°C, V_{CC}=3.3V±0.3V. See notes 1,2.)

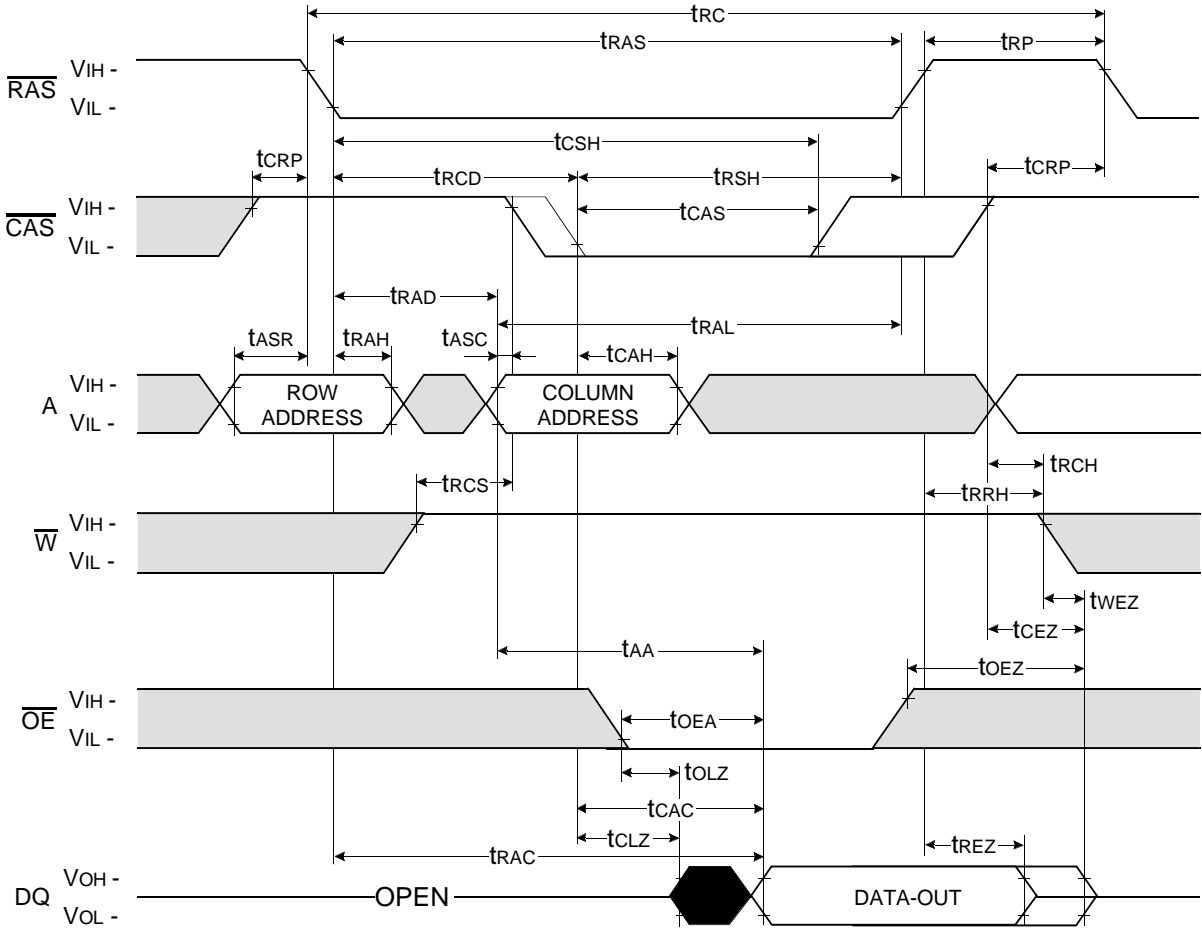
Test condition : V_{ih}/V_{il}=2.0/0.8V, V_{oh}/V_{ol}=2.0/0.8V, Output loading CL=100pF

Parameter	Symbol	-5		-6		Unit	Note
		Min	Max	Min	Max		
Column address to \overline{W} delay time	tAWD	48		55		ns	7
\overline{CAS} precharge time to \overline{W} delay time	tCPWD	53		60		ns	
\overline{CAS} set-up time(\overline{CAS} -before- \overline{RAS} refresh)	tCSR	5		5		ns	14
\overline{CAS} hold time(\overline{CAS} -before- \overline{RAS} refresh)	tCHR	8		8		ns	14
\overline{RAS} to \overline{CAS} precharge time	tRPC	3		3		ns	14
Access time from \overline{CAS} precharge	tCPA		33		40	ns	3,14
Hyper page cycle time	tHPC	20		25		ns	12
Hyper page read-modify-write cycle time	tHPRWC	68		77		ns	12
\overline{CAS} precharge time(Hyper page cycle)	tCP	8		10		ns	
\overline{RAS} pulse width (Hyper page cycle)	tRASP	50	200K	60	200K	ns	
\overline{RAS} hold time from \overline{CAS} precharge	tRHCP	35		40		ns	14
\overline{OE} access time	tOEA		18		20	ns	14
\overline{OE} to data delay	tOED	18		20		ns	14
Output buffer turn off delay time from \overline{OE}	tOEZ	5	18	5	20	ns	6,11,14
\overline{OE} command hold time	tOEH	13		15		ns	
\overline{W} to \overline{RAS} precharge time(C-B-R refresh)	tWRP	15		15		ns	14
\overline{W} to \overline{RAS} hold time(C-B-R refresh)	tWRH	8		8		ns	14
Output data hold time	tDOH	10		10		ns	14
Output buffer turn off delay time from \overline{RAS}	tREZ	3	13	3	15	ns	6.11.12
Output buffer turn off delay time from \overline{W}	tWEZ	3	18	3	20	ns	6.11.14
\overline{W} to data delay	tWED	20		20		ns	14
\overline{OE} to \overline{CAS} hold time	tOCH	5		5		ns	
\overline{CAS} hold time to \overline{OE}	tCHO	5		5		ns	
\overline{OE} precharge time	tOEP	5		5		ns	
\overline{W} pulse width(Hyper page cycle)	tWPE	5		5		ns	
Present Detect Read Cycle							
\overline{PDE} to Valid PD bit	tPD		10		10	ns	
\overline{PDE} to PD bit Inactive	tPDOFF	2	7	2	7	ns	

NOTES

1. An initial pause of 200us is required after power-up followed by any 8 \overline{RAS} -only or \overline{CAS} -before- \overline{RAS} refresh cycles before proper device operation is achieved.
2. Input voltage levels are V_{ih}/V_{il} . $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\min)$ and $V_{IL}(\max)$ and are assumed to be 5ns for all inputs.
3. Measured with a load equivalent to 1 TTL loads and 100pF. $V_{oh}=2.0V$ and $V_{ol}=0.8V$.
4. Operation within the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RCD}(\max)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
5. Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
7. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are non restrictive operating parameter. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\min)$ the cycle is an early write cycle and the data out pin will remain high impedance for the duration of the cycle.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the \overline{CAS} leading edge in early write cycles and to the \overline{W} leading edge in read-write cycles.
10. Operation within the $t_{RAD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met. $t_{RAD}(\max)$ is specified as reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max)$ limit, then access time is controlled by t_{AA} .
11. $t_{CEZ}(\max)$, $t_{REZ}(\max)$, $t_{WEZ}(\max)$ and $t_{OEZ}(\max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If \overline{RAS} goes to high before \overline{CAS} high going, the open circuit condition of the output is achieved by \overline{CAS} high going. If \overline{CAS} goes to high before \overline{RAS} high going, the open circuit condition of the output is achieved by \overline{RAS} high going.
13. $t_{ASC} \geq t_{CP \min}$
14. The timing skew from the DRAM to the DIMM resulted from the addition of buffers.

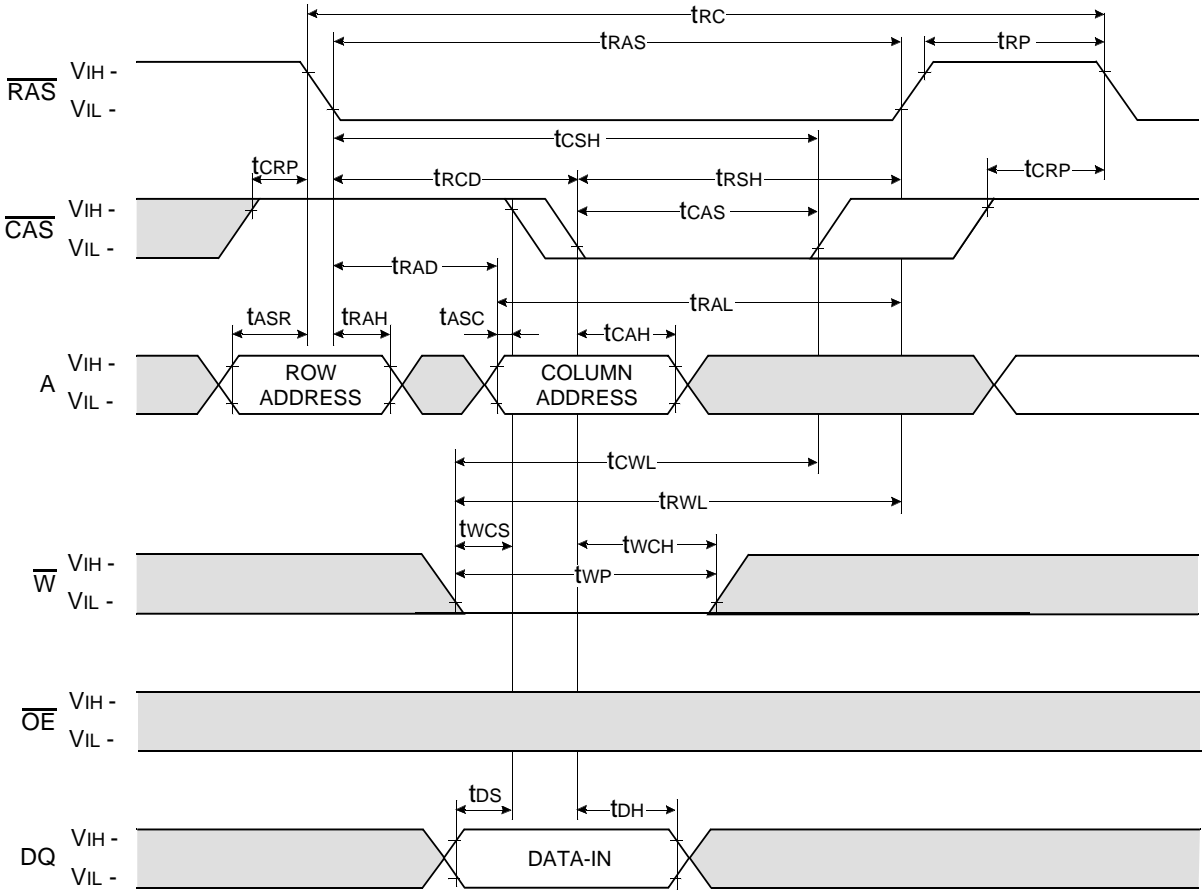
READ CYCLE



Don't care
Undefined

WRITE CYCLE (EARLY WRITE)

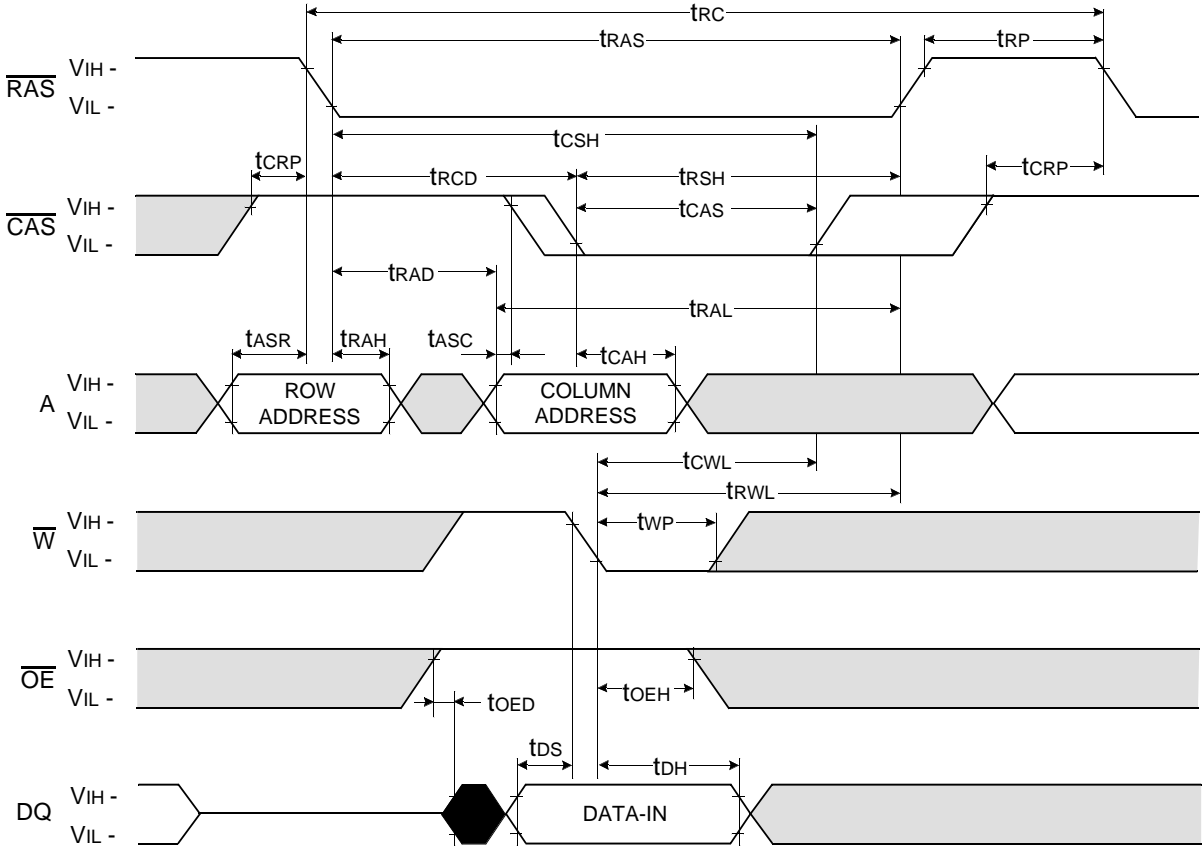
NOTE : DOUT = OPEN



Don't care
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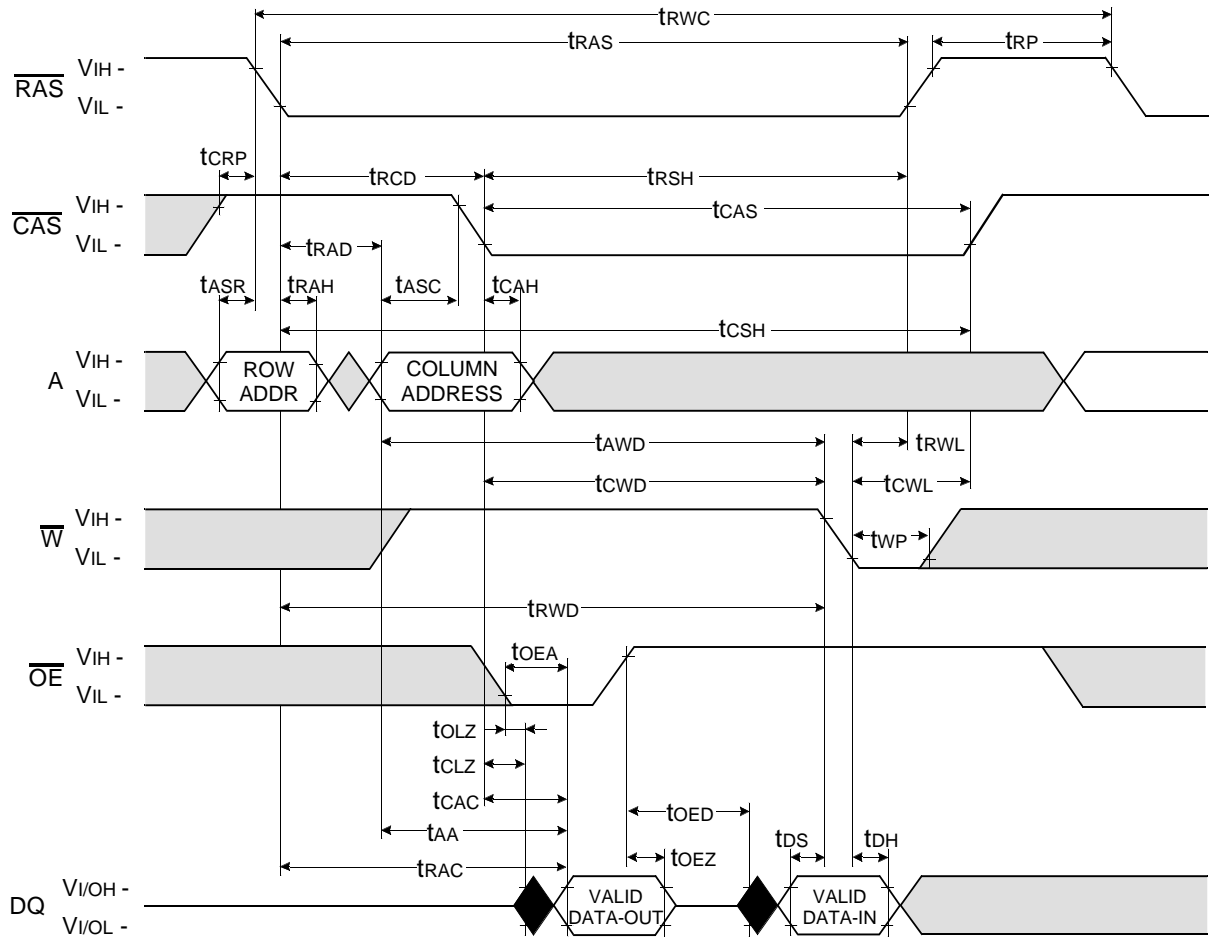
WRITE CYCLE (\overline{OE} CONTROLLED WRITE)

NOTE : DOUT = OPEN



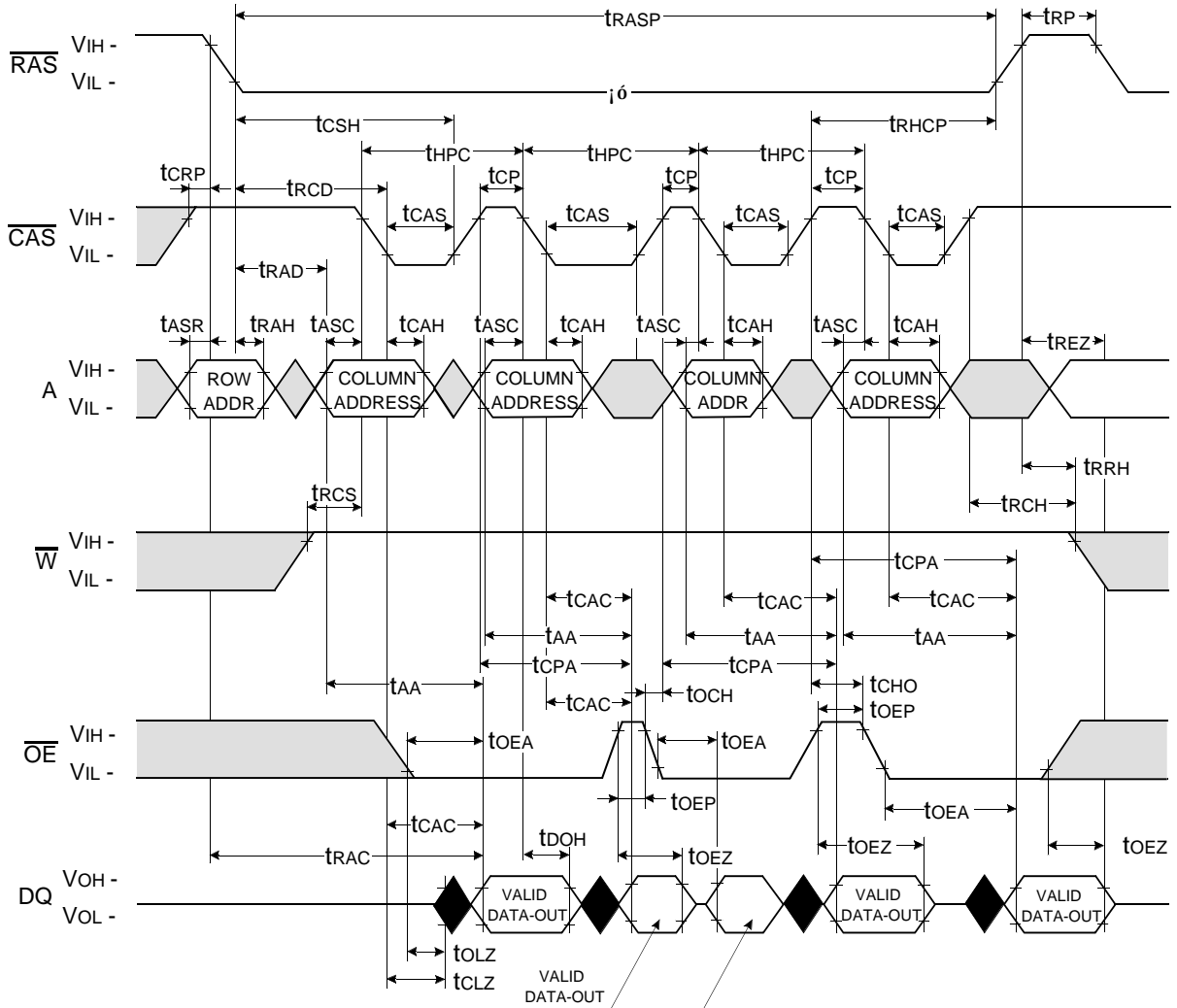
□ Don't care
■ Undefined

READ - MODIFY - WRITE CYCLE



Don't care
 Undefined

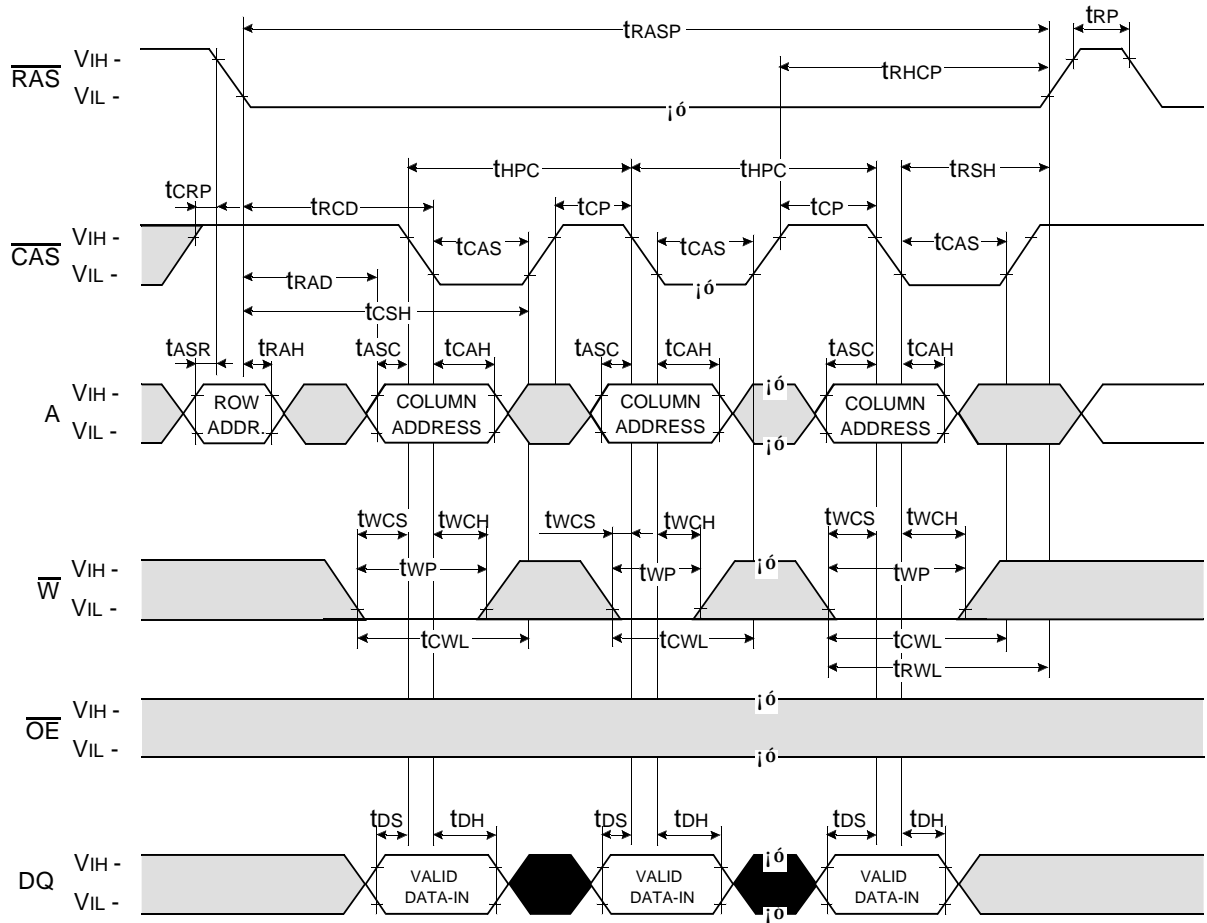
HYPER PAGE READ CYCLE





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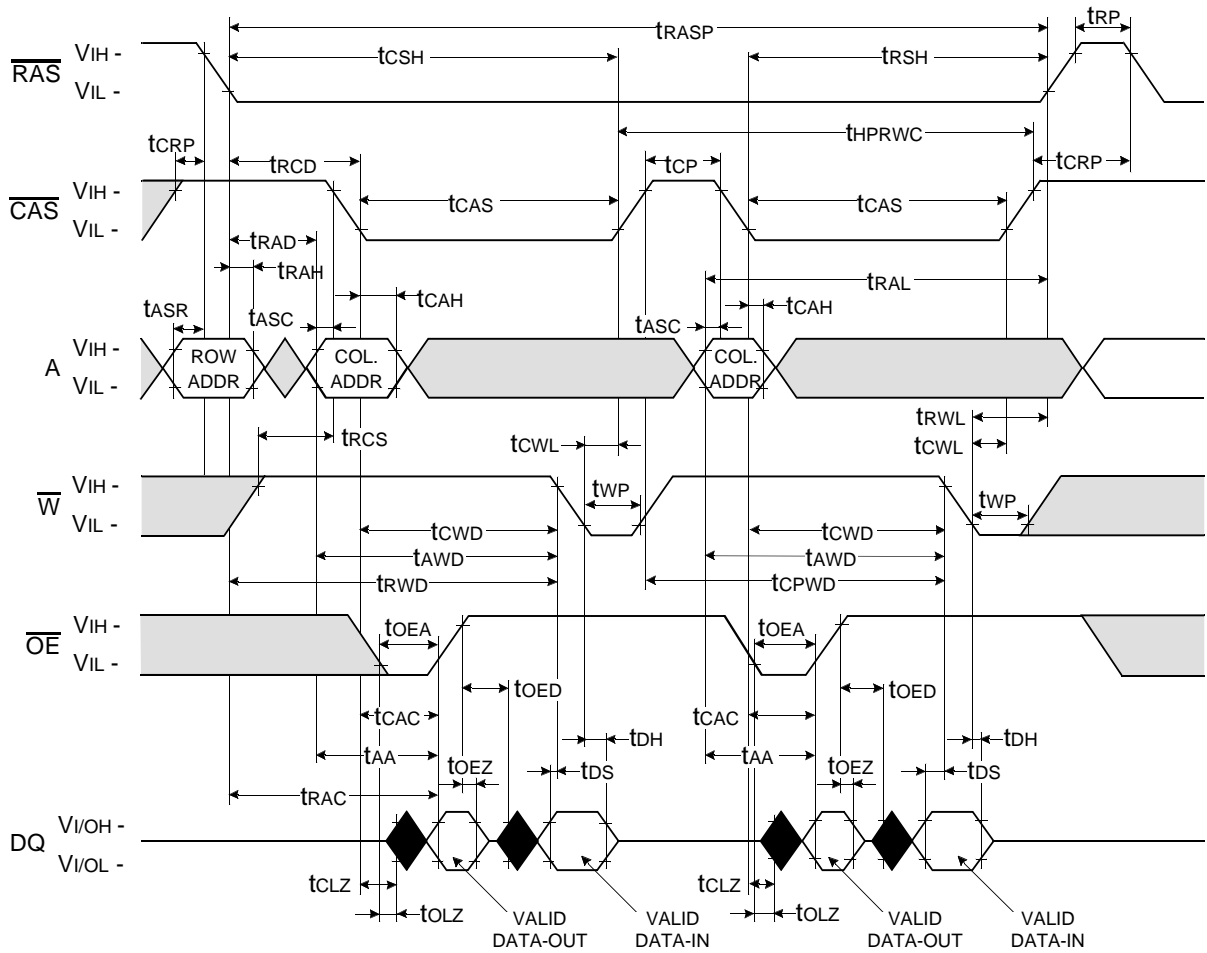
HYPER PAGE WRITE CYCLE (EARLY WRITE)

NOTE : DOUT = OPEN



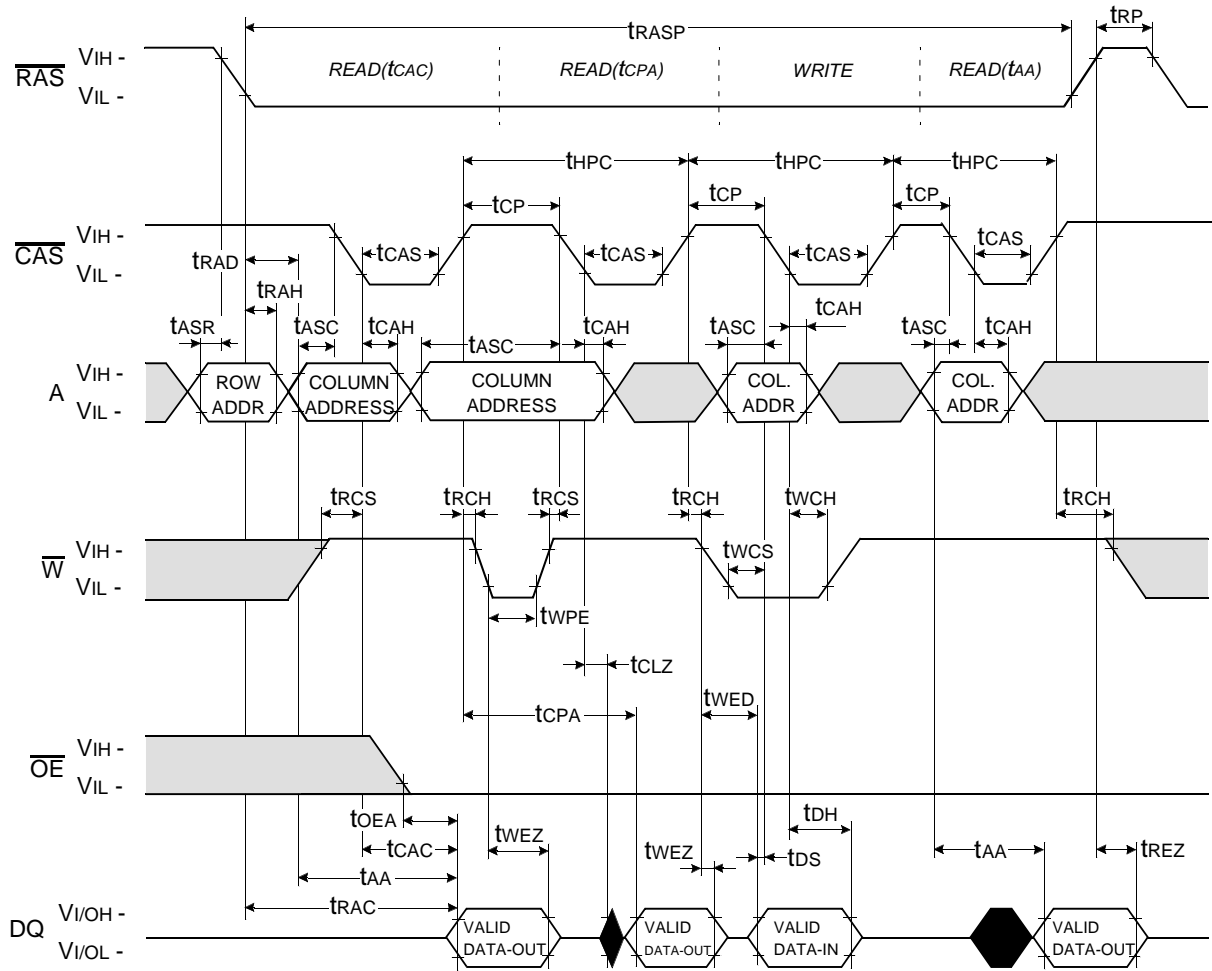
 Don't care
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HYPER PAGE READ-MODIFY-WRITE CYCLE



Don't care
 Undefined

HYPER PAGE READ AND WRITE MIXED CYCLE

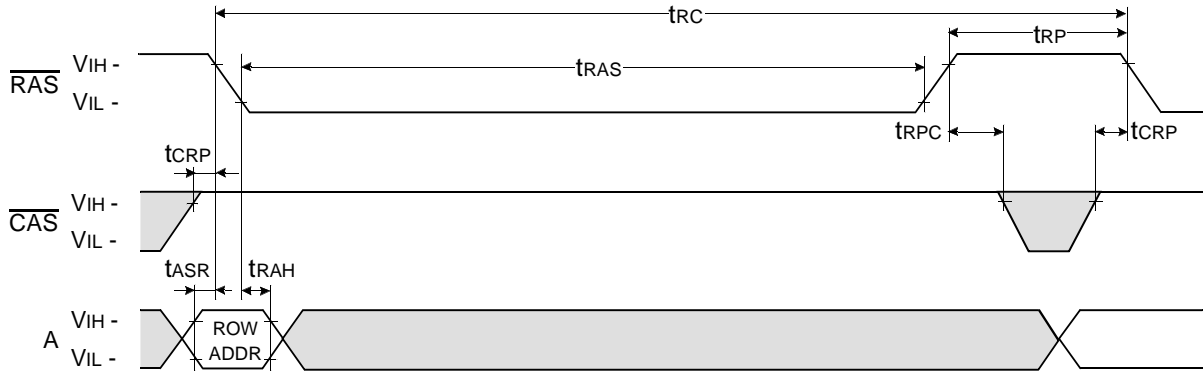


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$\overline{\text{RAS}}$ - ONLY REFRESH CYCLE*

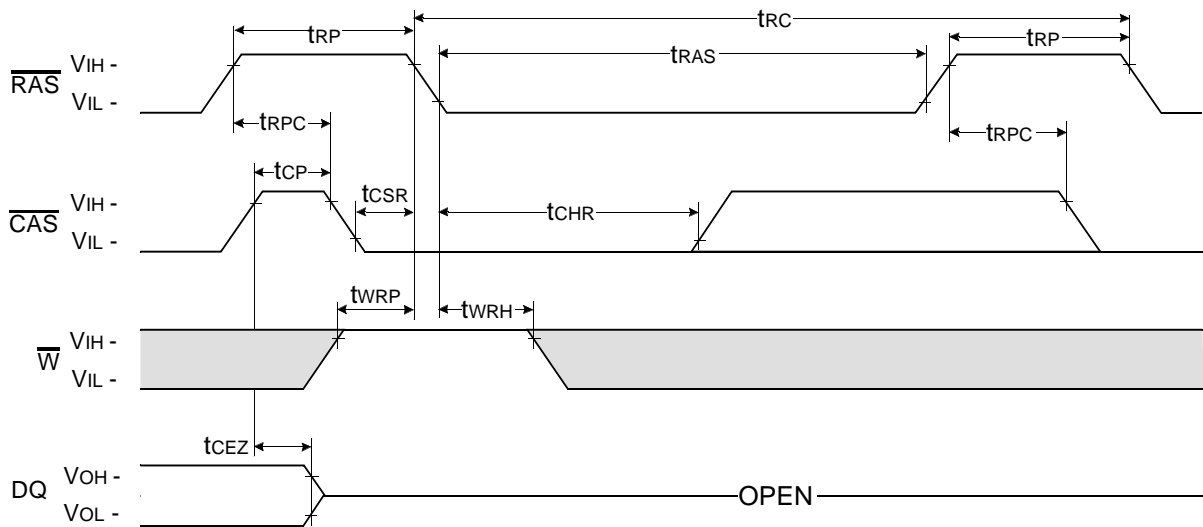
NOTE : $\overline{\text{W}}$, $\overline{\text{OE}}$, DIN = Don't care

DOUT = OPEN



$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ REFRESH CYCLE

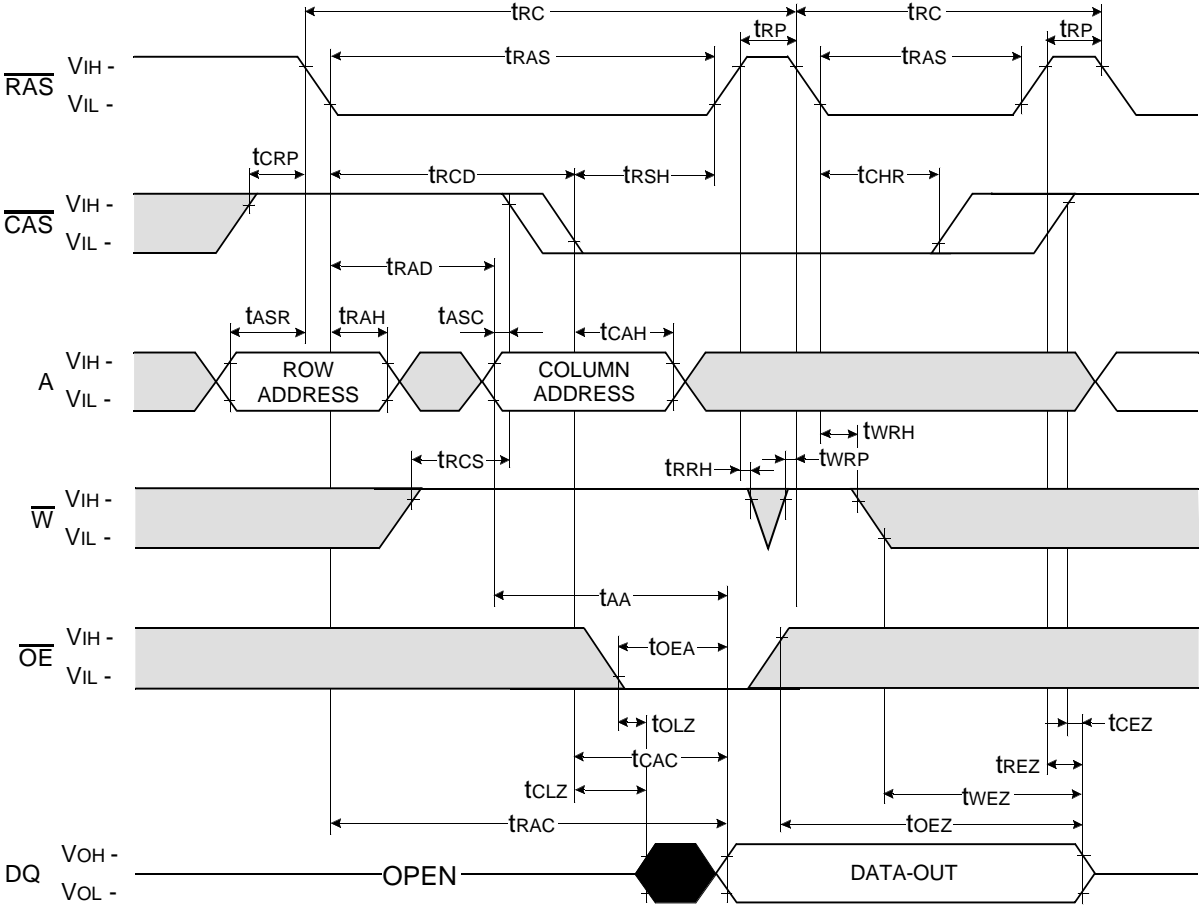
NOTE : $\overline{\text{OE}}$, A = Don't care



Don't care
 Undefined

* In $\overline{\text{RAS}}$ -only refresh cycle of 64Mb A-die & B-die, when $\overline{\text{CAS}}$ signal transits from Low to High, the valid data may be cut off.

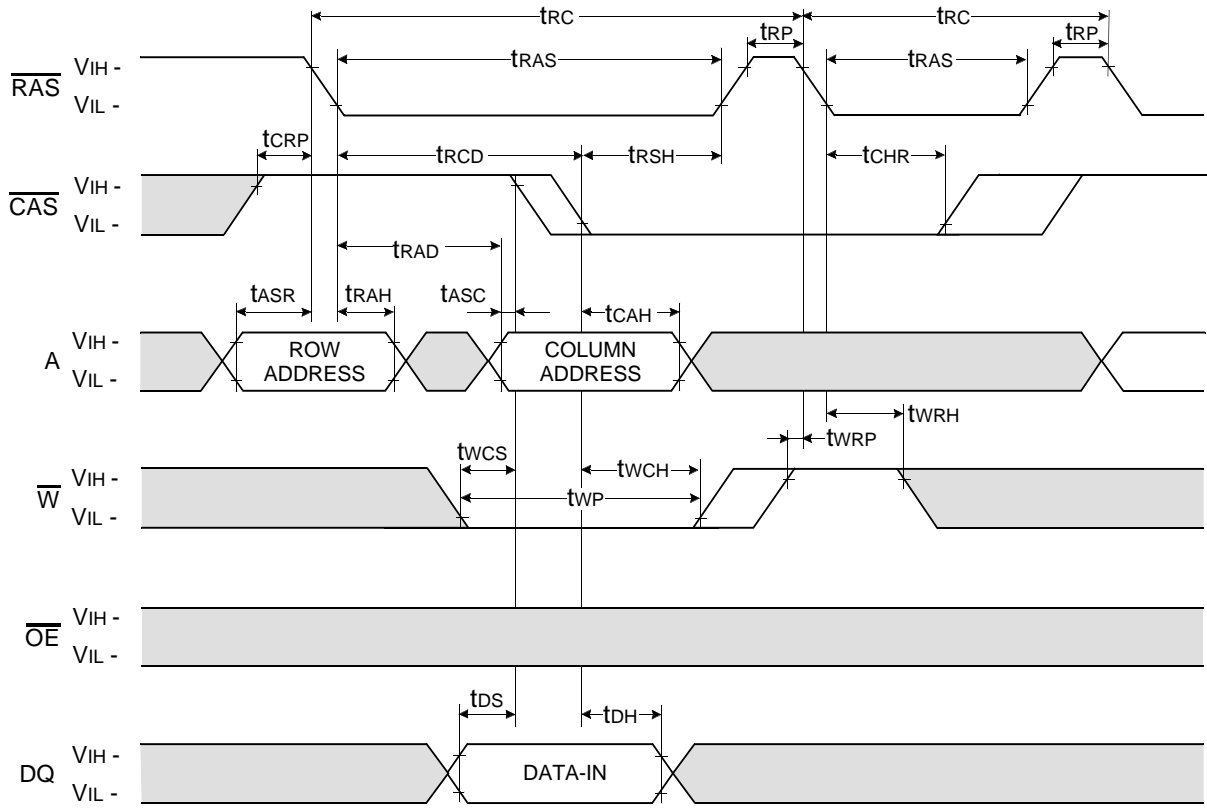
HIDDEN REFRESH CYCLE (READ)



Don't care
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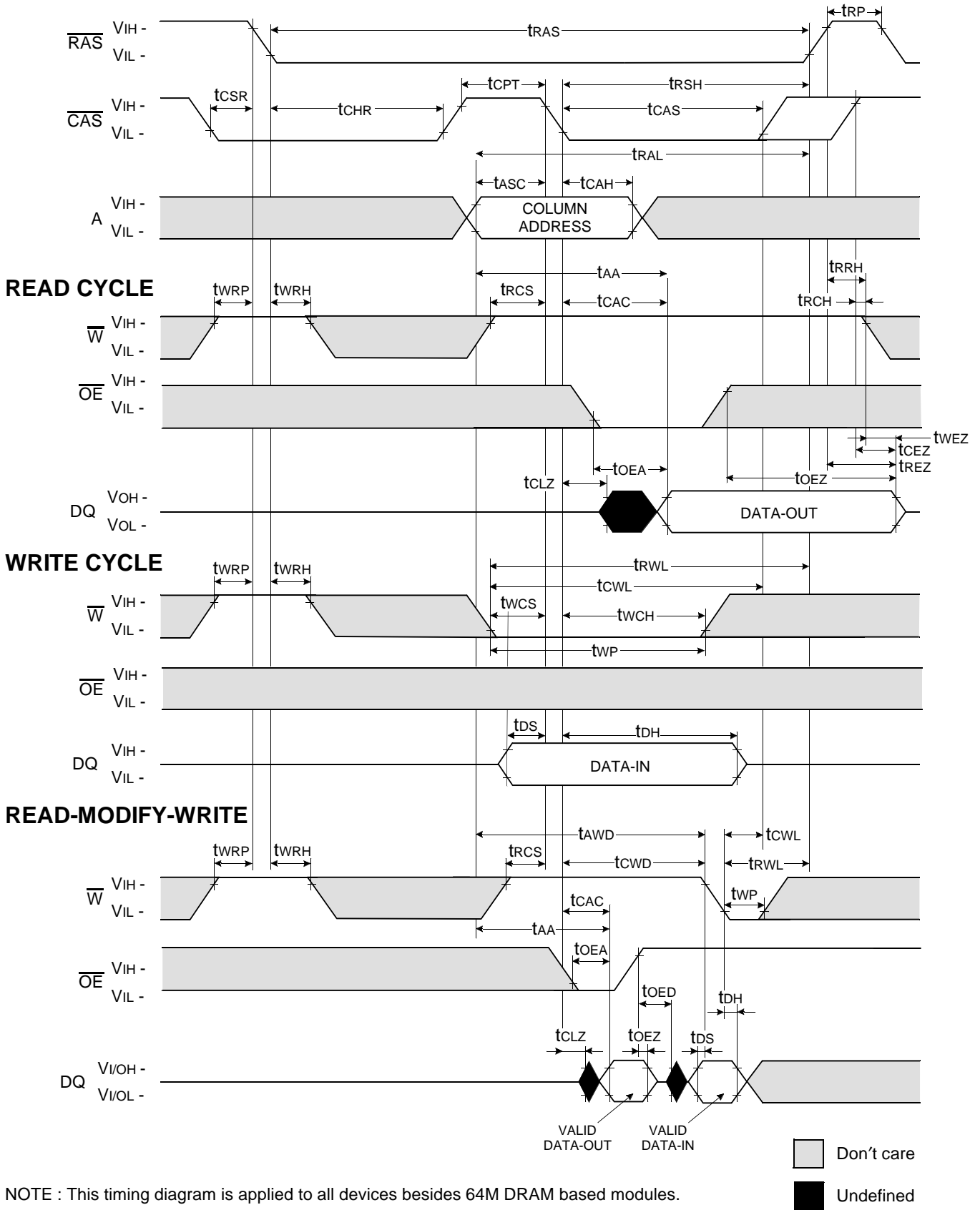
HIDDEN REFRESH CYCLE (WRITE)

NOTE : DOUT = OPEN



□ Don't care
■ Undefined

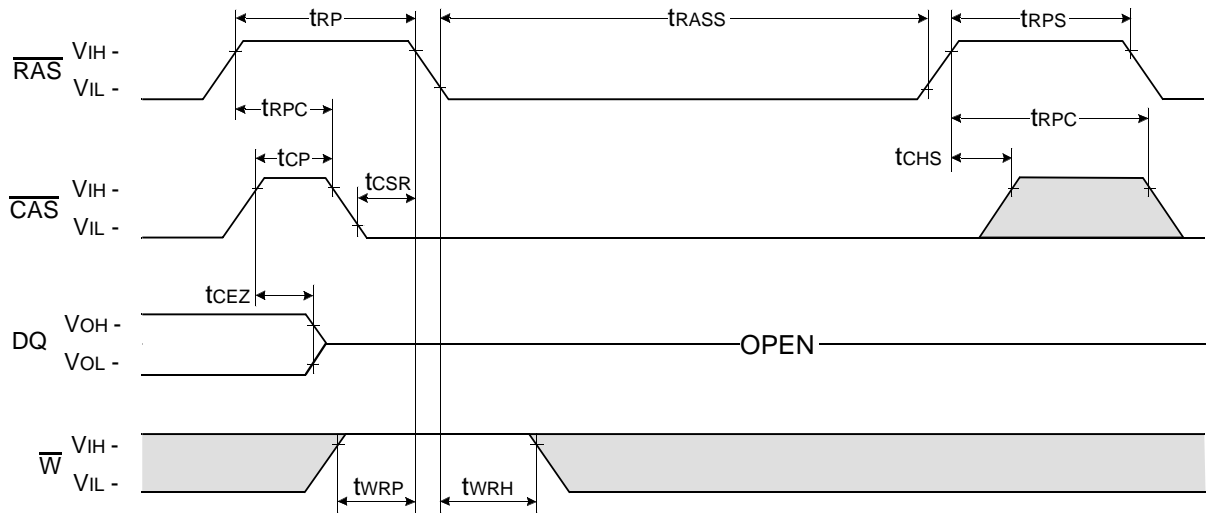
CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



NOTE : This timing diagram is applied to all devices besides 64M DRAM based modules.

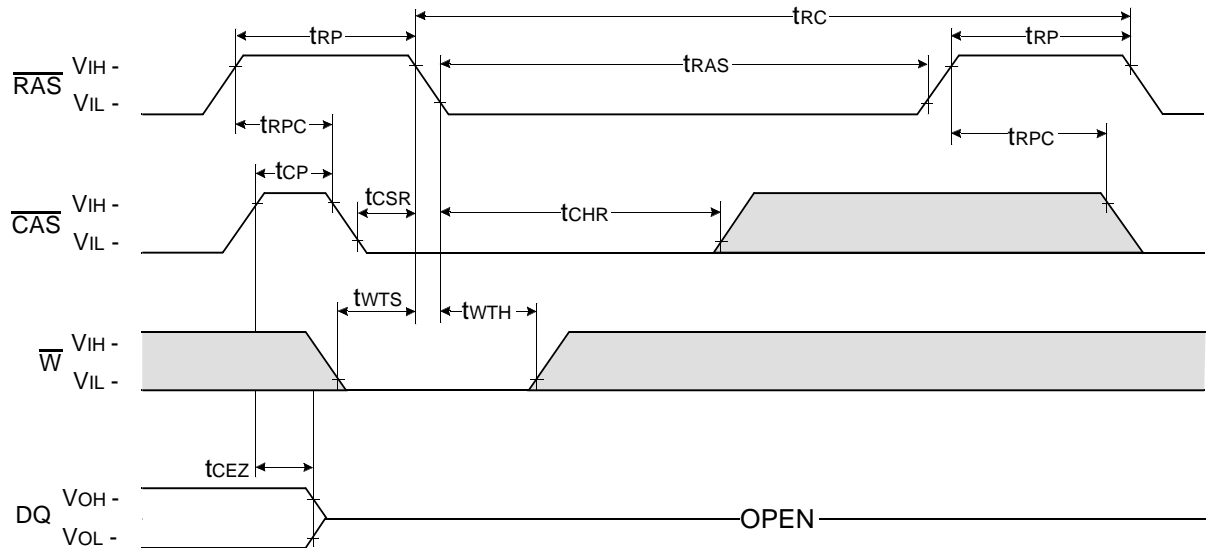
$\overline{\text{CAS}}$ - BEFORE - $\overline{\text{RAS}}$ SELF REFRESH CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



TEST MODE IN CYCLE

NOTE : $\overline{\text{OE}}$, A = Don't care



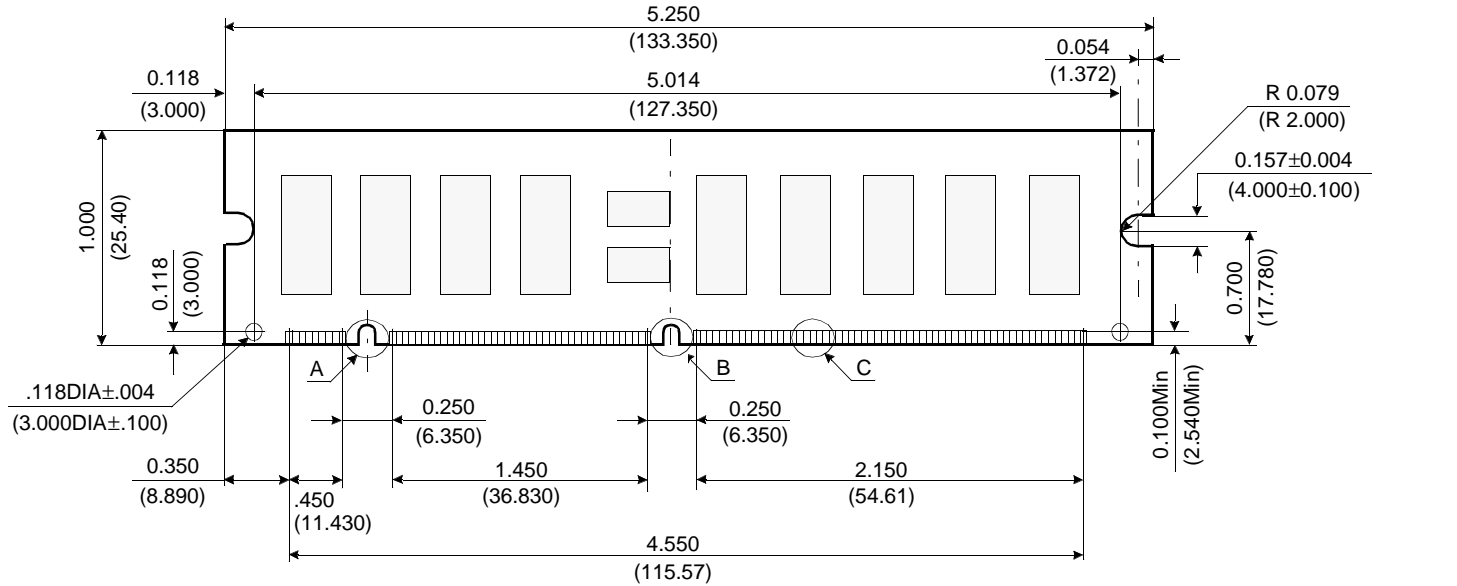
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DRAM MODULE

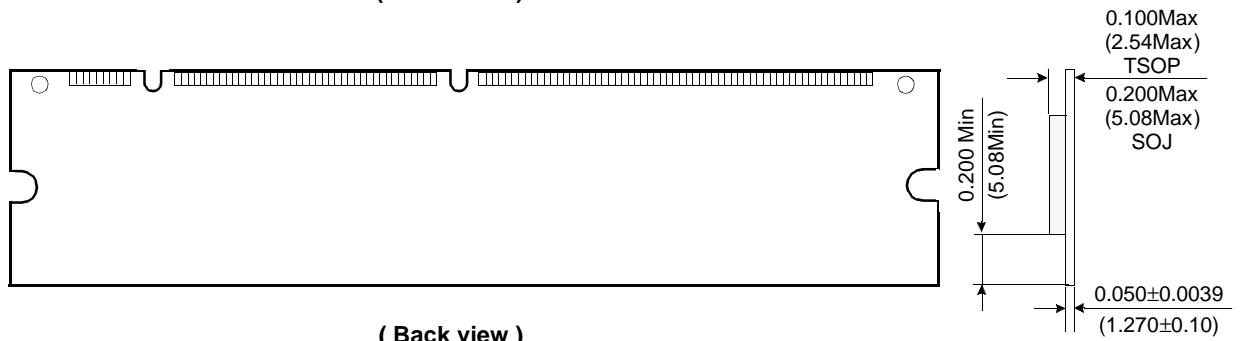
KMM372F213CK/CS

PACKAGE DIMENSIONS

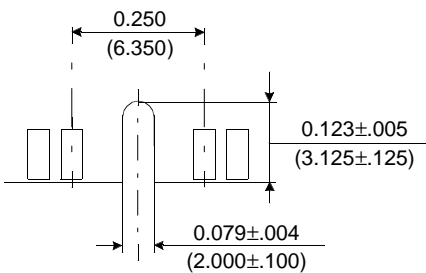
Units : Inches (millimeters)



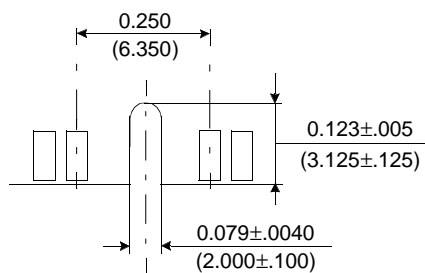
(Front view)



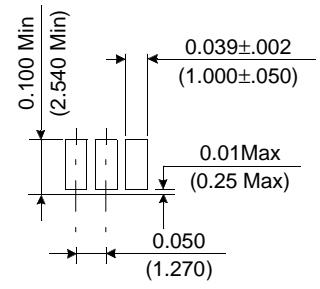
(Back view)



Detail A



Detail B



Detail C

Tolerances : ±.005(.13) unless otherwise specified

The used device is 2Mx8 DRAM with EDO mode, SOJ or TSOP II. (Forward)
 DRAM Part No. : KMM372F213CK/CS - KM48V2104CK and KM48V2104CS.