

KS0715

33 COM / 100 SEG DRIVER & CONTROLLER FOR STN LCD

January.2000

Ver. 4.0

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| KS0715 Specification Revision History | | |
|---------------------------------------|--|----------|
| Version | Content | Date |
| 1.0 | CAP3P → C3+, CAP2P → C2+, CAP1P → C1+ CAP3M → C3-, CAP2M → C2-, CAP1M → C1- Oscillator frequency FOSC (kHz) = → 19 (Min.): 22.5 (Typ.): 26 (Max.) FCL (kHz) = → 2.37 (Min.): 2.81 (Typ.): 3.25 (Max.) | |
| 2.0 | Temperature coefficient TEMPS = L: -0.0%/°C → -0.05%/°C Absolute maximum ratings VLCD: +0.3 to +15.0 → -0.3 to +17.0 Dynamic current consumption IDD1: 40μA (Max.) IDD2: 75μA (Typ.), 100μA (Max.) | |
| 3.0 | Oscillator frequency (internal) 19: 22.5: 26 → 17: 22.5: 27 Oscillator frequency (external) 2.13: 2.81: 3.25 → 2.13: 2.81: 3.37 | |
| 3.1 | | Apr.1999 |
| 4.0 | Change VDD Range : 2.4V to 5.5V → 2.4V to 3.6V | Jan.2000 |

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INTRODUCTION

The KS0715 is a driver & controller LSI for graphic dot-matrix liquid crystal display systems. It contains 33 common and 100 segment driver circuits. This chip is connected directly to a microprocessor, accepts serial or 8-bit parallel display data and stores in an on-chip display data RAM of 65 x 132 bits. It provides a highly-flexible display section due to 1-to-1 correspondence between on-chip display data RAM bits and LCD panel pixels. And it performs display data RAM read/write operation with no external operating clock to minimize power consumption. In addition, because it contains power supply circuits necessary to drive liquid crystal, it is possible to make a display system with the fewest components.

FEATURES

Driver Output Circuits

- 33 common outputs / 100 segment outputs

On-chip Display Data RAM

- Capacity: 65 x 132 = 8,580 bits
- Bit data "1": a dot of display is illuminated.
- Bit data "0": a dot of display is not illuminated.

Multi-chip Operation (Master, Slave) Available

Applicable Duty Ratios

| Duty ratio | Applicable LCD bias | Maximum display area |
|------------|---------------------|----------------------|
| 1/33 | 1/5 or 1/6 | 33 × 100 |

Microprocessor Interface

- 8-bit parallel bi-directional interface with 6800-series or 8080-series
- Serial interface (only write operation) available

Various Instruction Setting

On-chip Low Power Analog Circuit

- On-chip oscillator circuit
- Voltage converter (x2, x3 and x4)
- Voltage regulator (temperature coefficient: -0.05%/°C, -0.2%/°C)
- On-chip electronic contrast control function (32 steps)
- Voltage follower (LCD bias: 1/5 or 1/6)

Operating Voltage Range

- Supply voltage (V_{DD}): 2.4 to 3.6 V
- LCD driving voltage (V_{LCD} = V_O - V_{SS}): 4.0 to 15.0 V

Low Power Consumption

- 100 μA Typ. (V_{DD} = 3V, x4 boosting, V_O = 8V, internal power supply ON and display OFF)
- 10 μA Max. (during power save [standby] mode)

Wide Operating Temperature Range

- T_a = -40°C to +85°C

Package Type

- Gold bumped chip or TCP

Series Specifications

| Product code | TEMPS pin | Temp. coefficient | Package | Chip thickness |
|------------------|----------------------|-------------------|---------|----------------|
| KS0715UM-L0CC | 0 (VSS connected) | -0.05%/°C | COG | 670 μm |
| KS0715UM-L4CC | | | | 470 μm |
| KS0715UM-H0CC | 1 (VDD connected) | -0.2%/°C | | 670 μm |
| KS0715UM-H4CC | | | | 470 μm |
| KS0715TB-XX-L0TF | 0 (VSS connected) | -0.05%/°C | TCP | 670 μm |
| KS0715TB-XX-L4TF | | | | 470 μm |
| KS0715TB-XX-H0TF | 1 (VDD connected) | -0.2%/°C | | 670 μm |
| KS0715TB-XX-H4TF | | | | 470 μm |

* XX: TCP ordering number

BLOCK DIAGRAM

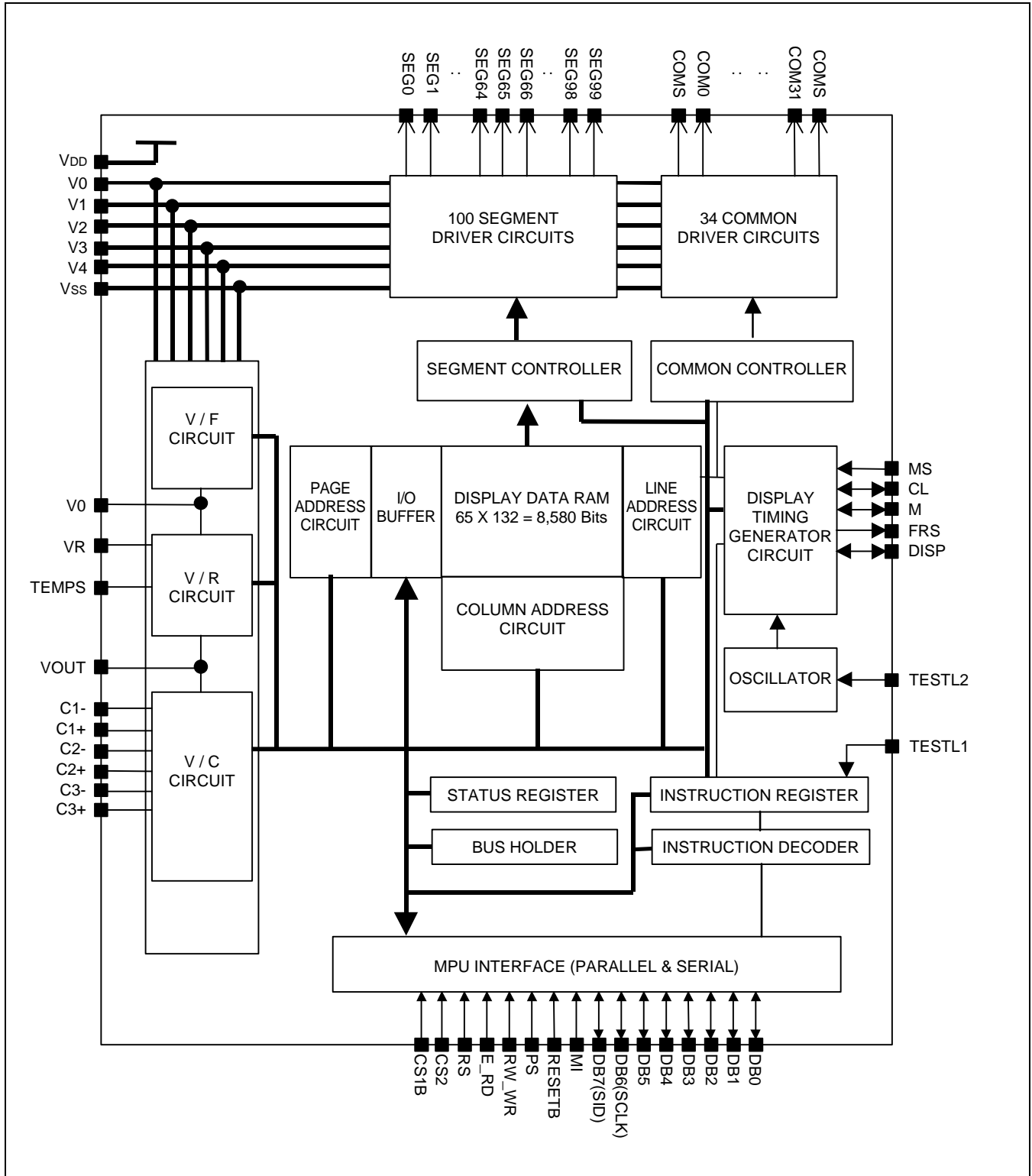


Figure 1. Block Diagram

PAD CONFIGURATION

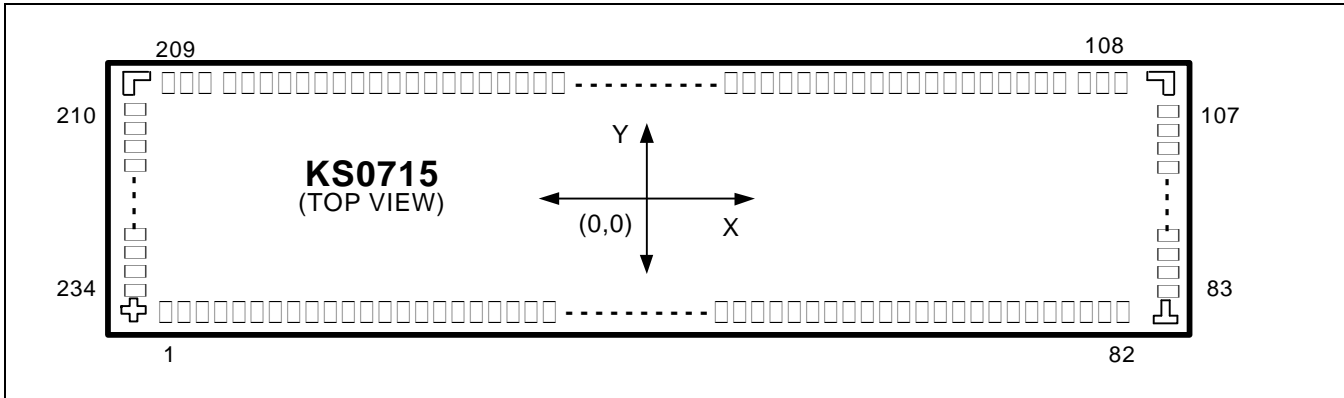
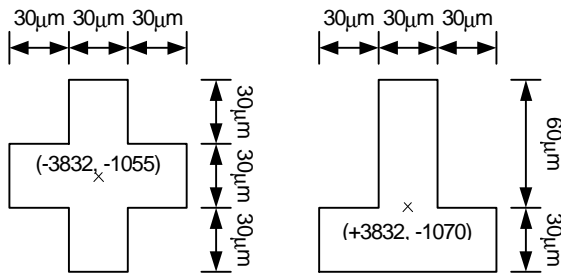


Figure 2. KS0715 Chip Configuration

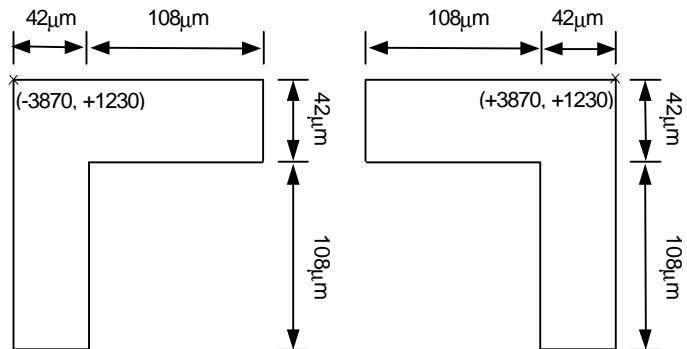
Table 1. KS0715 Pad Dimensions

| Item | Pad No. | Size | | Unit |
|-------------------|------------|-----------|------|------|
| | | X | Y | |
| Chip size | - | 7980 | 2700 | μm |
| Pad pitch | 1 to 82 | 90 | | |
| | 83 to 234 | 70 | | |
| Bumped pad size | 1 to 82 | 56 | 114 | |
| | 83 to 107 | 108 | 50 | |
| | 108 to 209 | 50 | 108 | |
| | 210 to 234 | 108 | 50 | |
| Bumped pad height | All pad | 17 (Typ.) | | |

COG Align Key Coordinate



ILB Align Key Coordinate



PAD CENTER COORDINATES

Table 2. Pad Center Coordinates

| [Unit: μm] | | | | | | | | | | | |
|------------------------|--------|-------|-------|-----|--------|------|-------|-----|-------|------|------|
| No. | Name | X | Y | No. | Name | X | Y | No. | Name | X | Y |
| 1 | DUMMY | -3645 | -1226 | 51 | C1+ | 855 | -1226 | 101 | COM1 | 3830 | 420 |
| 2 | TESTL1 | -3555 | -1226 | 52 | C1+ | 945 | -1226 | 102 | COM0 | 3830 | 490 |
| 3 | VDD | -3465 | -1226 | 53 | C1- | 1035 | -1226 | 103 | COMS | 3830 | 560 |
| 4 | FRS | -3375 | -1226 | 54 | C1- | 1125 | -1226 | 104 | DUMMY | 3830 | 630 |
| 5 | M | -3285 | -1226 | 55 | C2+ | 1215 | -1226 | 105 | DUMMY | 3830 | 700 |
| 6 | CL | -3195 | -1226 | 56 | C2+ | 1305 | -1226 | 106 | DUMMY | 3830 | 770 |
| 7 | DISP | -3105 | -1226 | 57 | C2- | 1395 | -1226 | 107 | DUMMY | 3830 | 840 |
| 8 | VDD | -3015 | -1226 | 58 | C2- | 1485 | -1226 | 108 | DUMMY | 3535 | 1190 |
| 9 | MS | -2925 | -1226 | 59 | VSS | 1575 | -1226 | 109 | SEG0 | 3465 | 1190 |
| 10 | VSS | -2835 | -1226 | 60 | VSS | 1665 | -1226 | 110 | SEG1 | 3395 | 1190 |
| 11 | RESETB | -2745 | -1226 | 61 | VR | 1755 | -1226 | 111 | SEG2 | 3325 | 1190 |
| 12 | VDD | -2655 | -1226 | 62 | VR | 1845 | -1226 | 112 | SEG3 | 3255 | 1190 |
| 13 | PS | -2565 | -1226 | 63 | V0 | 1935 | -1226 | 113 | SEG4 | 3185 | 1190 |
| 14 | VSS | -2475 | -1226 | 64 | V0 | 2025 | -1226 | 114 | SEG5 | 3115 | 1190 |
| 15 | CS1B | -2385 | -1226 | 65 | V0 | 2115 | -1226 | 115 | SEG6 | 3045 | 1190 |
| 16 | CS2 | -2295 | -1226 | 66 | V0 | 2205 | -1226 | 116 | SEG7 | 2975 | 1190 |
| 17 | VDD | -2205 | -1226 | 67 | V0 | 2295 | -1226 | 117 | SEG8 | 2905 | 1190 |
| 18 | MI | -2115 | -1226 | 68 | V0 | 2385 | -1226 | 118 | SEG9 | 2835 | 1190 |
| 19 | VSS | -2025 | -1226 | 69 | V1 | 2475 | -1226 | 119 | SEG10 | 2765 | 1190 |
| 20 | VDD | -1935 | -1226 | 70 | V1 | 2565 | -1226 | 120 | SEG11 | 2695 | 1190 |
| 21 | RS | -1845 | -1226 | 71 | V2 | 2655 | -1226 | 121 | SEG12 | 2625 | 1190 |
| 22 | VSS | -1755 | -1226 | 72 | V2 | 2745 | -1226 | 122 | SEG13 | 2555 | 1190 |
| 23 | RW_WR | -1665 | -1226 | 73 | V3 | 2835 | -1226 | 123 | SEG14 | 2485 | 1190 |
| 24 | E_RD | -1575 | -1226 | 74 | V3 | 2925 | -1226 | 124 | SEG15 | 2415 | 1190 |
| 25 | VDD | -1485 | -1226 | 75 | V4 | 3015 | -1226 | 125 | SEG16 | 2345 | 1190 |
| 26 | VDD | -1395 | -1226 | 76 | V4 | 3105 | -1226 | 126 | SEG17 | 2275 | 1190 |
| 27 | VDD | -1305 | -1226 | 77 | VSS | 3195 | -1226 | 127 | SEG18 | 2205 | 1190 |
| 28 | VDD | -1215 | -1226 | 78 | VSS | 3285 | -1226 | 128 | SEG19 | 2135 | 1190 |
| 29 | VDD | -1125 | -1226 | 79 | TEMPS | 3375 | -1226 | 129 | SEG20 | 2065 | 1190 |
| 30 | VDD | -1035 | -1226 | 80 | VDD | 3465 | -1226 | 130 | SEG21 | 1995 | 1190 |
| 31 | DB0 | -945 | -1226 | 81 | TESTL2 | 3555 | -1226 | 131 | SEG22 | 1925 | 1190 |
| 32 | DB1 | -855 | -1226 | 82 | DUMMY | 3645 | -1226 | 132 | SEG23 | 1855 | 1190 |
| 33 | DB2 | -765 | -1226 | 83 | DUMMY | 3830 | -840 | 133 | SEG24 | 1785 | 1190 |
| 34 | DB3 | -675 | -1226 | 84 | DUMMY | 3830 | -770 | 134 | SEG25 | 1715 | 1190 |
| 35 | DB4 | -585 | -1226 | 85 | DUMMY | 3830 | -700 | 135 | SEG26 | 1645 | 1190 |
| 36 | DB5 | -495 | -1226 | 86 | DUMMY | 3830 | -630 | 136 | SEG27 | 1575 | 1190 |
| 37 | DB6 | -405 | -1226 | 87 | COM15 | 3830 | -560 | 137 | SEG28 | 1505 | 1190 |
| 38 | DB7 | -315 | -1226 | 88 | COM14 | 3830 | -490 | 138 | SEG29 | 1435 | 1190 |
| 39 | VSS | -225 | -1226 | 89 | COM13 | 3830 | -420 | 139 | SEG30 | 1365 | 1190 |
| 40 | VSS | -135 | -1226 | 90 | COM12 | 3830 | -350 | 140 | SEG31 | 1295 | 1190 |
| 41 | VSS | -45 | -1226 | 91 | COM11 | 3830 | -280 | 141 | SEG32 | 1225 | 1190 |
| 42 | VSS | 45 | -1226 | 92 | COM10 | 3830 | -210 | 142 | SEG33 | 1155 | 1190 |
| 43 | VSS | 135 | -1226 | 93 | COM9 | 3830 | -140 | 143 | SEG34 | 1085 | 1190 |
| 44 | VSS | 225 | -1226 | 94 | COM8 | 3830 | -70 | 144 | SEG35 | 1015 | 1190 |
| 45 | VOUT | 315 | -1226 | 95 | COM7 | 3830 | 0 | 145 | SEG36 | 945 | 1190 |
| 46 | VOUT | 405 | -1226 | 96 | COM6 | 3830 | 70 | 146 | SEG37 | 875 | 1190 |
| 47 | C3+ | 495 | -1226 | 97 | COM5 | 3830 | 140 | 147 | SEG38 | 805 | 1190 |
| 48 | C3+ | 585 | -1226 | 98 | COM4 | 3830 | 210 | 148 | SEG39 | 735 | 1190 |
| 49 | C3- | 675 | -1226 | 99 | COM3 | 3830 | 280 | 149 | SEG40 | 665 | 1190 |
| 50 | C3- | 765 | -1226 | 100 | COM2 | 3830 | 350 | 150 | SEG41 | 595 | 1190 |

Table 2. Pad Center Coordinates (Continued)

[Unit: μm]

| No. | Name | X | Y | No. | Name | X | Y | No. | Name | X | Y |
|-----|-------|-------|------|-----|-------|-------|------|-----|------|---|---|
| 151 | SEG42 | 525 | 1190 | 201 | SEG92 | -2975 | 1190 | | | | |
| 152 | SEG43 | 455 | 1190 | 202 | SEG93 | -3045 | 1190 | | | | |
| 153 | SEG44 | 385 | 1190 | 203 | SEG94 | -3115 | 1190 | | | | |
| 154 | SEG45 | 315 | 1190 | 204 | SEG95 | -3185 | 1190 | | | | |
| 155 | SEG46 | 245 | 1190 | 205 | SEG96 | -3255 | 1190 | | | | |
| 156 | SEG47 | 175 | 1190 | 206 | SEG97 | -3325 | 1190 | | | | |
| 157 | SEG48 | 105 | 1190 | 207 | SEG98 | -3395 | 1190 | | | | |
| 158 | SEG49 | 35 | 1190 | 208 | SEG99 | -3465 | 1190 | | | | |
| 159 | SEG50 | -35 | 1190 | 209 | DUMMY | -3535 | 1190 | | | | |
| 160 | SEG51 | -105 | 1190 | 210 | DUMMY | -3830 | 840 | | | | |
| 161 | SEG52 | -175 | 1190 | 211 | DUMMY | -3830 | 770 | | | | |
| 162 | SEG53 | -245 | 1190 | 212 | DUMMY | -3830 | 700 | | | | |
| 163 | SEG54 | -315 | 1190 | 213 | DUMMY | -3830 | 630 | | | | |
| 164 | SEG55 | -385 | 1190 | 214 | COM16 | -3830 | 560 | | | | |
| 165 | SEG56 | -455 | 1190 | 215 | COM17 | -3830 | 490 | | | | |
| 166 | SEG57 | -525 | 1190 | 216 | COM18 | -3830 | 420 | | | | |
| 167 | SEG58 | -595 | 1190 | 217 | COM19 | -3830 | 350 | | | | |
| 168 | SEG59 | -665 | 1190 | 218 | COM20 | -3830 | 280 | | | | |
| 169 | SEG60 | -735 | 1190 | 219 | COM21 | -3830 | 210 | | | | |
| 170 | SEG61 | -805 | 1190 | 220 | COM22 | -3830 | 140 | | | | |
| 171 | SEG62 | -875 | 1190 | 221 | COM23 | -3830 | 70 | | | | |
| 172 | SEG63 | -945 | 1190 | 222 | COM24 | -3830 | 0 | | | | |
| 173 | SEG64 | -1015 | 1190 | 223 | COM25 | -3830 | -70 | | | | |
| 174 | SEG65 | -1085 | 1190 | 224 | COM26 | -3830 | -140 | | | | |
| 175 | SEG66 | -1155 | 1190 | 225 | COM27 | -3830 | -210 | | | | |
| 176 | SEG67 | -1225 | 1190 | 226 | COM28 | -3830 | -280 | | | | |
| 177 | SEG68 | -1295 | 1190 | 227 | COM29 | -3830 | -350 | | | | |
| 178 | SEG69 | -1365 | 1190 | 228 | COM30 | -3830 | -420 | | | | |
| 179 | SEG70 | -1435 | 1190 | 229 | COM31 | -3830 | -490 | | | | |
| 180 | SEG71 | -1505 | 1190 | 230 | COMS | -3830 | -560 | | | | |
| 181 | SEG72 | -1575 | 1190 | 231 | DUMMY | -3830 | -630 | | | | |
| 182 | SEG73 | -1645 | 1190 | 232 | DUMMY | -3830 | -700 | | | | |
| 183 | SEG74 | -1715 | 1190 | 233 | DUMMY | -3830 | -770 | | | | |
| 184 | SEG75 | -1785 | 1190 | 234 | DUMMY | -3830 | -840 | | | | |
| 185 | SEG76 | -1855 | 1190 | | | | | | | | |
| 186 | SEG77 | -1925 | 1190 | | | | | | | | |
| 187 | SEG78 | -1995 | 1190 | | | | | | | | |
| 188 | SEG79 | -2065 | 1190 | | | | | | | | |
| 189 | SEG80 | -2135 | 1190 | | | | | | | | |
| 190 | SEG81 | -2205 | 1190 | | | | | | | | |
| 191 | SEG82 | -2275 | 1190 | | | | | | | | |
| 192 | SEG83 | -2345 | 1190 | | | | | | | | |
| 193 | SEG84 | -2415 | 1190 | | | | | | | | |
| 194 | SEG85 | -2485 | 1190 | | | | | | | | |
| 195 | SEG86 | -2555 | 1190 | | | | | | | | |
| 196 | SEG87 | -2625 | 1190 | | | | | | | | |
| 197 | SEG88 | -2695 | 1190 | | | | | | | | |
| 198 | SEG89 | -2765 | 1190 | | | | | | | | |
| 199 | SEG90 | -2835 | 1190 | | | | | | | | |
| 200 | SEG91 | -2905 | 1190 | | | | | | | | |

PIN DESCRIPTION

POWER SUPPLY

Table 3. Power Supply Pin Description

| Name | I/O | Description | | | | | | | | | | | | | | | |
|----------------------------|-------------------|---|-------------------|-------------------|----|----|----|----------|-------------------|-------------------|-------------------|-------------------|----------|-------------------|-------------------|-------------------|-------------------|
| VDD | Supply | Power supply | | | | | | | | | | | | | | | |
| VSS | Supply | Ground | | | | | | | | | | | | | | | |
| V0 V1 V2 V3 V4 | I/O | <p>LCD driver supply voltages The voltage determined by LCD pixel is impedance-converted by an operational amplifier for application. Voltages should have the following relationship; $V0 \geq V1 \geq V2 \geq V3 \geq V4 \geq VSS$ When the internal power circuit is active, these voltages are generated as following table according to the state of LCD Bias.</p> <table border="1"> <thead> <tr> <th>LCD bias</th> <th>V1</th> <th>V2</th> <th>V3</th> <th>V4</th> </tr> </thead> <tbody> <tr> <td>1/6 bias</td> <td>$(5/6) \times V0$</td> <td>$(4/6) \times V0$</td> <td>$(2/6) \times V0$</td> <td>$(1/6) \times V0$</td> </tr> <tr> <td>1/5 bias</td> <td>$(4/5) \times V0$</td> <td>$(3/5) \times V0$</td> <td>$(2/5) \times V0$</td> <td>$(1/5) \times V0$</td> </tr> </tbody> </table> | LCD bias | V1 | V2 | V3 | V4 | 1/6 bias | $(5/6) \times V0$ | $(4/6) \times V0$ | $(2/6) \times V0$ | $(1/6) \times V0$ | 1/5 bias | $(4/5) \times V0$ | $(3/5) \times V0$ | $(2/5) \times V0$ | $(1/5) \times V0$ |
| LCD bias | V1 | V2 | V3 | V4 | | | | | | | | | | | | | |
| 1/6 bias | $(5/6) \times V0$ | $(4/6) \times V0$ | $(2/6) \times V0$ | $(1/6) \times V0$ | | | | | | | | | | | | | |
| 1/5 bias | $(4/5) \times V0$ | $(3/5) \times V0$ | $(2/5) \times V0$ | $(1/5) \times V0$ | | | | | | | | | | | | | |

LCD DRIVER SUPPLY

Table 4. LCD Driver Supply Pin Description

| Name | I/O | Description |
|------|-----|---|
| C1- | O | Capacitor 1 negative connection pin for voltage converter |
| C1+ | O | Capacitor 1 positive connection pin for voltage converter |
| C2- | O | Capacitor 2 negative connection pin for voltage converter |
| C2+ | O | Capacitor 2 positive connection pin for voltage converter |
| C3- | O | Capacitor 3 negative connection pin for voltage converter |
| C3+ | O | Capacitor 3 positive connection pin for voltage converter |
| VOUT | I/O | Voltage converter input / output pin |
| VR | I | V0 voltage adjustment pin |

SYSTEM CONTROL

Table 5. System Control Pin Description

| Name | I/O | Description | | | | | | |
|-------|-----|---|-------------|----------------------|--------|--------|--------|--------|
| MS | I | Master / Slave operation select pin – MS = "H": master operation – MS = "L": slave operation The following table depends on the MS status. | | | | | | |
| | | MS | OSC circuit | Power supply circuit | CL | M | FRS | DISP |
| | | H | Enabled | Input | Output | Output | Output | Output |
| | | L | Disabled | Disabled | Input | Input | Output | Input |
| CL | I/O | Display clock input / output pin When the KS0715 is used in master/slave mode (multi-chip), the CL pins must be connected each other for sync. | | | | | | |
| M | I/O | LCD AC signal input / output pin When the KS0715 is used in master/slave mode (multi-chip), the M pins must be connected each other. – MS = "H": output – MS = "L": input | | | | | | |
| FRS | O | Static driver segment output pin This pin is used together with the M pin. | | | | | | |
| DISP | I/O | LCD display blanking control input/output. When KS0715 is used in master/slave mode (multi-chip), the DISP pins must be connected each other. – MS = "H": output – MS = "L": input | | | | | | |
| TEMPS | I | Selects temperature coefficient of the reference voltage – TEMPS = "L": -0.05%/°C – TEMPS = "H": -0.2%/°C | | | | | | |

MICROPROCESSOR INTERFACE

Table 6. Microprocessor Interface Pin Description

| Name | I/O | Description | | | | | | |
|---|-----|--|----------------|-------------|--|------------|---------------|--------------|
| RESETB | I | Reset input pin When RESETB is "L", initialization is executed. | | | | | | |
| PS | I | Parallel / serial data input select input | | | | | | |
| | | PS | Interface mode | Chip select | Data / instruction | Data | Read / write | Serial clock |
| | | H | Parallel | CS1B, CS2 | RS | DB0 to DB7 | E_RD RW_WR | - |
| | | L | Serial | CS1B, CS2 | RS | SID (DB7) | Write only | SCLK (DB6) |
| *NOTE: When PS is "L", DB0 to DB5 are high impedance and E_RD and RW_WR should be fixed to either "H" or "L". | | | | | | | | |
| MI | I | Microprocessor interface select input pin – MI = "H": 6800-series MPU interface – MI = "L": 8080-series MPU interface | | | | | | |
| CS1B CS2 | I | Chip select input pins Data / instruction I/O is enabled only when CS1B is "L" and CS2 is "H". When chip select is non-active, DB0 to DB7 may be high impedance. | | | | | | |
| RS | I | Register select input pin – RS = "H": DB0 to DB7 are display data. – RS = "L": DB0 to DB7 are control data. | | | | | | |
| RW_WR | I | Read / Write execution control pin | | | | | | |
| | | MI | MPU type | RW_WR | Description | | | |
| | | H | 6800-series | RW | Read/Write control input pin – RW = "H": read – RW = "L": write | | | |
| | | L | 8080-series | /WR | Write enable clock input pin The data on DB0 to DB7 are latched at the rising edge of the /WR signal. | | | |
| | | | | | | | | |

Table 6. Microprocessor Interface Pin Description (Continued)

| Name | I/O | Description | | | |
|------------|-----|--|-------------|------|---|
| E_RD | I | Read / Write execution control pin | | | |
| | | MI | MPU Type | E_RD | Description |
| | | H | 6800-series | E | Read / Write control input pin – RW = "H": When E is "H", DB0 to DB7 are in an output status. – RW = "L": The data on DB0 to DB7 are latched at the falling edge of the E signal. |
| | | L | 8080-series | /RD | Read enable clock input pin When /RD is "L", DB0 to DB7 are in an output status. |
| DB0 to DB7 | I/O | 8-bit bi-directional data bus that is connected to the standard 8-bit microprocessor data bus. When the serial interface selected (PS = "L"); – DB0 to DB5: high impedance – DB6: serial input clock (SCLK) – DB7: serial input data (SID) When chip select is not active, DB0 to DB7 may be high impedance. | | | |

LCD DRIVER OUTPUTS

Table 8. LCD Driver Outputs Pin Description

| Name | I/O | Description | | | |
|---------------------|-----|--|---|-------------------------------|-----------------|
| SEG0 to SEG99 | O | LCD segment driver outputs The display data and the M signal control the output voltage of segment driver. | | | |
| | | Display data | M | Segment driver output voltage | |
| | | | | Normal display | Reverse display |
| | | H | H | V0 | V2 |
| | | H | L | Vss | V3 |
| | | L | H | V2 | V0 |
| | | L | L | V3 | Vss |
| | | Power save mode | | Vss | Vss |
| COM0 to COM31 | O | LCD common driver outputs The internal scanning data and M signal control the output voltage of common driver. | | | |
| | | Scan data | M | Common driver output voltage | |
| | | H | H | Vss | |
| | | H | L | V0 | |
| | | L | H | V1 | |
| | | L | L | V4 | |
| | | Power save mode | | Vss | |
| COMS | O | Common output for the icons The output signals of two pins are same. When not used, these pins should be left open. In multi-chip (master/slave) mode, all COMS pins on both master and slave units are the same signal. | | | |

TEST PINS

Table 8. Test Pin Description

| Name | I/O | Description |
|------------------|-----|---|
| TESTL1 TESTL2 | I | IC test pins with pull-up These pins must be open. |

NOTE: **DUMMY** – These pins should be opened (floated).

FUNCTIONAL DESCRIPTION

MICROPROCESSOR INTERFACE

Chip Select Input

There are CS1B and CS2 pins for Chip Selection. The KS0715 can interface with an MPU only when CS1B is "L" and CS2 is "H". When these pins are set to any other combination, RS, E_RD, and RW_WR inputs are disabled and DB0 to DB7 are to be high impedance. And, in case of serial interface, the internal shift register and the counter are reset.

Parallel / Serial Interface

KS0715 has three types of interface with an MPU, which are one serial and two parallel interface. This parallel or serial interface is determined by PS pin as shown in table 9.

Table 9. Parallel / Serial Interface Mode

| PS | Type | CS1B | CS2 | MI | Interface mode |
|----|----------|------|-----|----|----------------------|
| H | Parallel | CS1B | CS2 | H | 6800-series MPU mode |
| | | | | L | 8080-series MPU mode |
| L | Serial | CS1B | CS2 | *x | Serial-mode |

*x: Don't care

Parallel Interface (PS = "H")

The 8-bit bi-directional data bus is used in parallel interface and the type of MPU is selected by MI as shown in table 10. The type of data transfer is determined by signals at RS, E_RD and RW_WR as shown in table 11.

Table 10. Microprocessor Selection for Parallel Interface

| MI | CS1B | CS2 | RS | E_RD | RW_WR | DB0 to DB7 | MPU bus |
|----|------|-----|----|------|-------|------------|-------------|
| H | CS1B | CS2 | RS | E | RW | DB0 to DB7 | 6800-series |
| L | CS1B | CS2 | RS | /RD | /WR | DB0 to DB7 | 8080-series |

Table 11. Parallel Data Transfer

| Common | 6800-series | | 8080-series | | Description |
|--------|-------------|------------|-------------|-------------|---|
| | E_RD (E) | RW_WR (RW) | E_RD (/RD) | RW_WR (/WR) | |
| RS | | | | | |
| H | H | H | L | H | Display data read out |
| H | H | L | H | L | Display data write |
| L | H | H | L | H | Register status read |
| L | H | L | H | L | Writes to internal register (instruction) |

Serial interface (PS = "L")

When the KS0715 is active, serial data (DB7) and serial clock (DB6) inputs are enabled. And not active, the internal 8-bit shift register and the 3-bit counter are reset. Serial data can be read on the rising edge of serial clock going into DB6 and processed as 8-bit parallel data on the eighth serial clock. Serial data input is display data when RS is high and control data when RS is low. Since the clock signal (DB6) is easy to be affected by the external noise caused by the line length, the operation check on the actual machine is recommended.

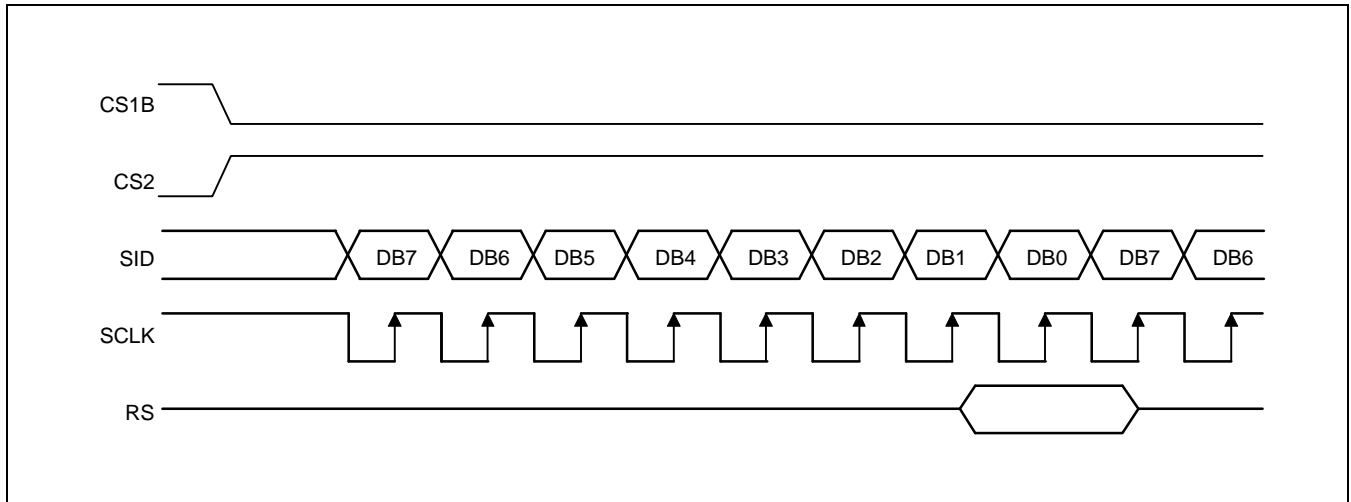


Figure 3. Serial Interface Timing

Busy Flag

The Busy Flag indicates whether the KS0715 is operating or not. When DB7 is "H" in read status operation, this device is in busy status and will accept only read status instruction. If the cycle time is correct, the microprocessor needs not to check this flag before each instruction, which improves the MPU performance.

Data Transfer

The KS0715 uses bus holder and internal data bus for Data Transfer with the MPU. When writing data from the MPU to on-chip RAM, data is automatically transferred from the bus holder to the RAM as shown in figure 4. And when reading data from on-chip RAM to the MPU, the data for the initial read cycle is stored in the bus holder (dummy read) and the MPU reads this stored data from bus holder for the next data read cycle as shown in figure 5. This means that a dummy read cycle must be inserted between each pair of address sets when a sequence of address sets is executed. Therefore, the data of the specified address cannot be output with the read display data instruction right after the address sets, but can be output at the second read of data.

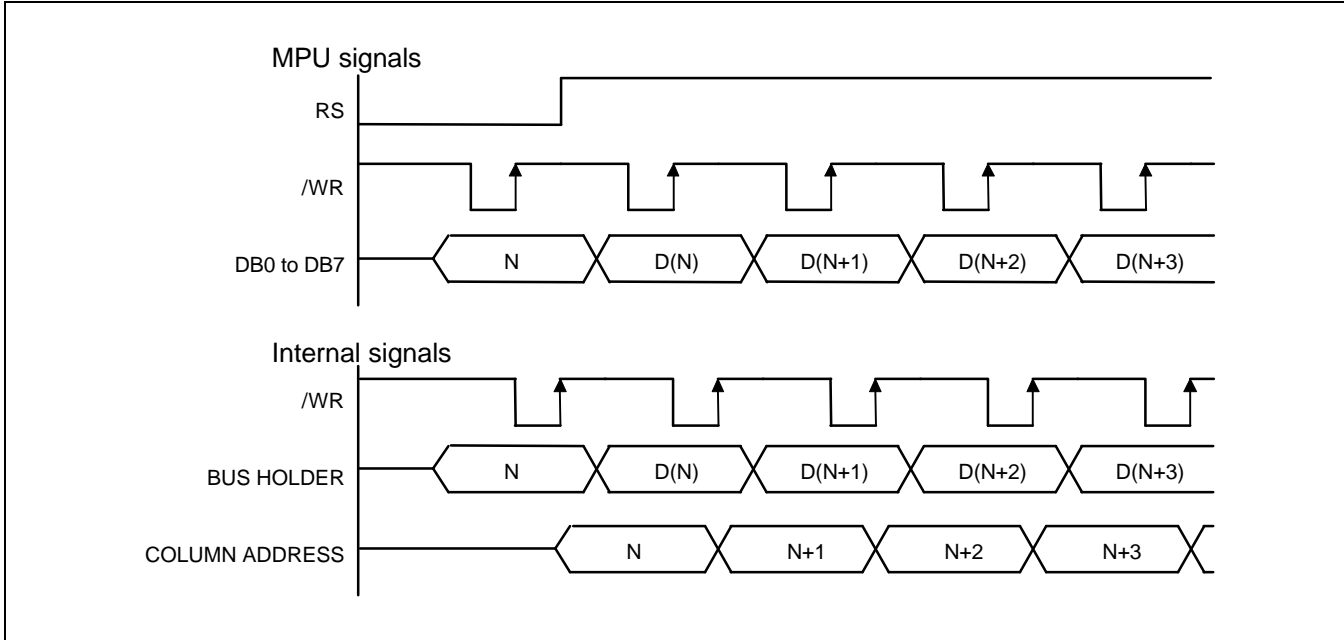


Figure 4. Write Timing

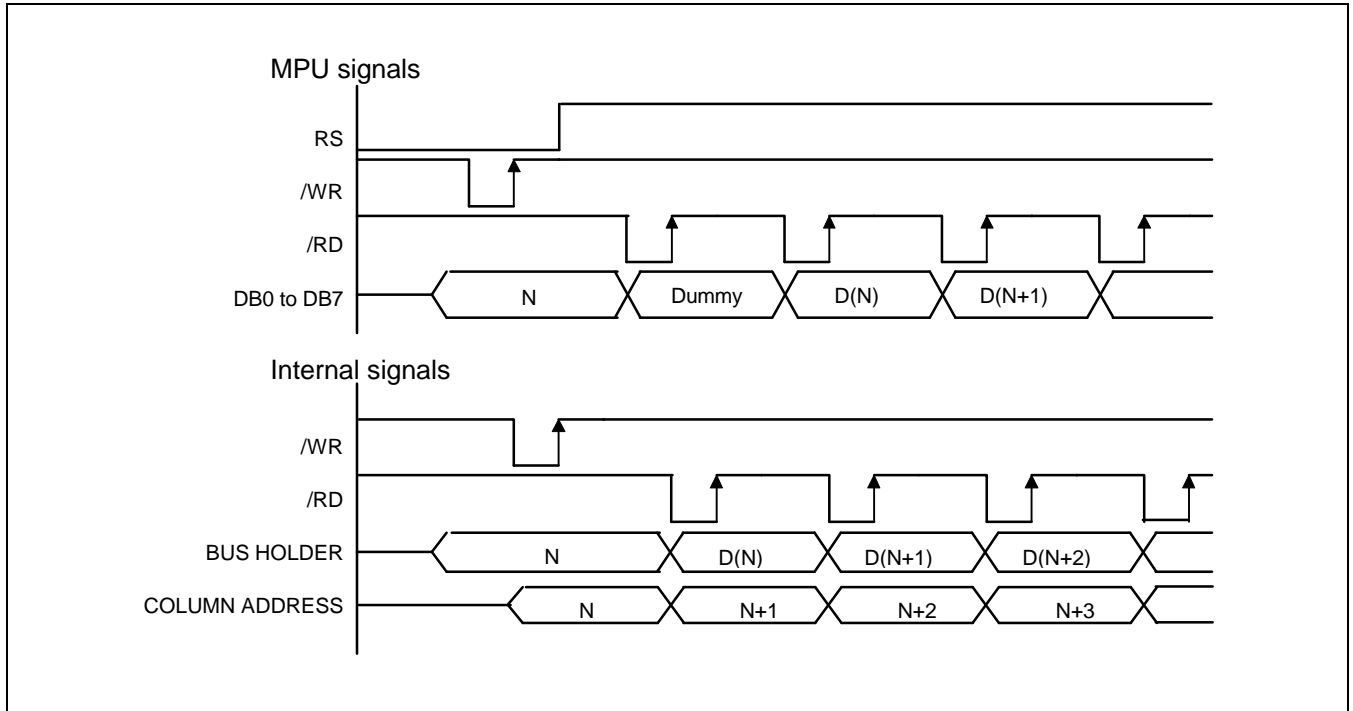


Figure 5. Read Timing

Column Address Circuit

Column Address circuit has an 8-bit preset counter that provides column address to the Display Data RAM as shown in figure 8. When set Column Address MSB / LSB instruction is issued, 8-bit [Y7:Y0] is updated. And, since this address is increased by 1 each a read or write Data instruction, microprocessor can access the display data continuously. However, the counter is not increased and locked if a non-existing address above 84H. It is unlocked if a column address is set again by set Column Address MSB / LSB instruction. And the column address counter is independent of page address register.

ADC select instruction makes it possible to invert the relationship between the column address and the segment outputs. It is necessary to rewrite the display data on built-in RAM after issuing ADC select instruction. Refer to the following figure 7.

| | | | | | | | | | |
|----------------------------------|---------------|-------|-------|-------|--------|--------|--------|--------|---------------|
| SEG output | - | SEG 0 | SEG 1 | SEG 2 | | SEG 97 | SEG 98 | SEG 99 | - |
| Column address [Y7:Y0] | 00H~0FH | 10H | 01H | 02H | | 71H | 72H | 73H | 74H~83H |
| Display data | × | 1 | 0 | 0 | | 0 | 1 | 1 | 0 |
| LCD panel display (ADC = 0) | Not outputted | | | | | | | | Not outputted |
| | | | | | | | | | |
| LCD panel display (ADC = 1) | Not outputted | | | | | | | | Not outputted |

Figure 7. The Relationship between the Column Address and the Segment Outputs

Segment Control Circuit

This circuit controls the display data by the display ON / OFF, reverse display ON / OFF and entire display ON / OFF instructions without changing the data in the display data RAM.

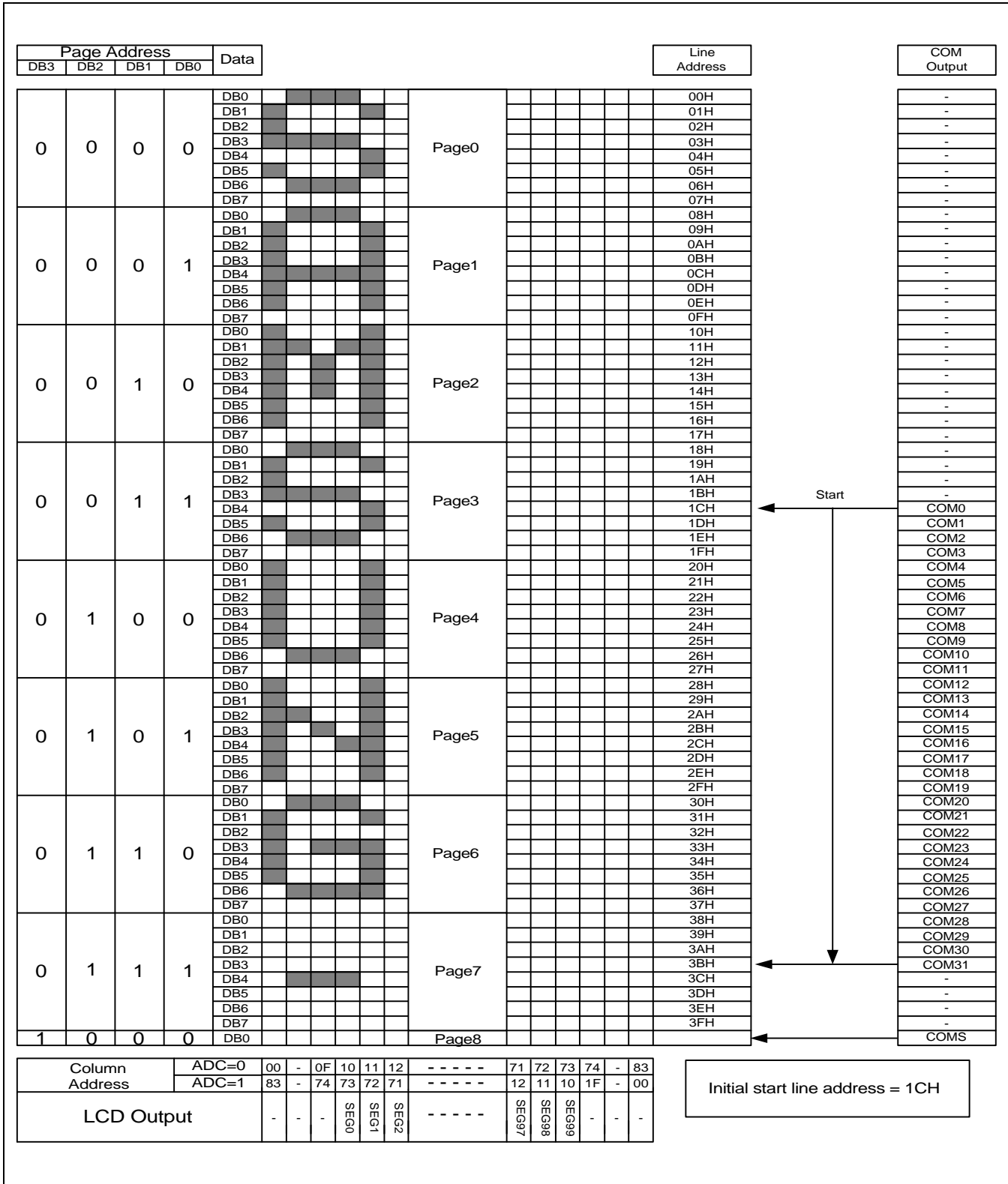


Figure 8. Display Data RAM Map

LCD DISPLAY CIRCUITS

Oscillator

This is completely on-chip Oscillator and its frequency is nearly independent of VDD. This oscillator signal is used in the voltage converter and display timing generation circuit.

* Test Condition: Temperature: 25°C & 85°C, TEMPS = "L", No Load

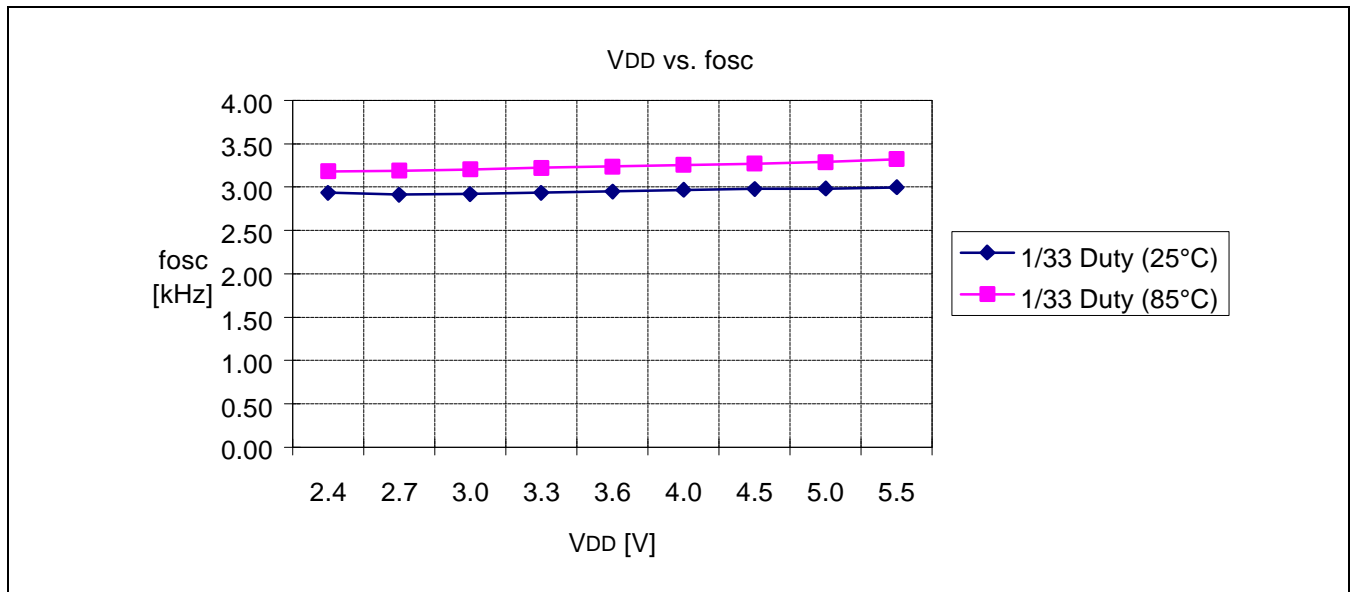


Figure 9. VDD vs. fosc

Display Timing Generator Circuit

This circuit generates some signals to be used for displaying LCD. The display clock, CL, generated by oscillation clock, generates the clock for the line counter and the signal for the display data latch. The line address of on-chip RAM is generated in synchronization with the display clock (CL) and the 100-bit display data is latched by the display data latch circuit in synchronization with the display clock. The display data, which is read to the LCD driver, is completely independent of the access to the display data RAM from the microprocessor. The display clock generates an LCD AC signal (M) which enables the LCD driver to make a AC drive waveform, and also generates an internal common timing signal and start signal to the common driver. Driving 2-frame AC driver waveform and internal timing signal are shown in figure 10.

In a multiple-chip configuration, the slave chip requires the M, CL and DISP signals from the master. Table 12 shows the M, CL, and DISP status.

Table 12. Master and Slave Timing Signal Status

| Operation mode | Oscillator | M | CL | DISP |
|----------------|---------------------------|--------|--------|--------|
| Master | ON (internal clock used) | Output | Output | Output |
| | OFF (external clock used) | Output | Input | Output |
| Slave | - | Input | Input | Input |

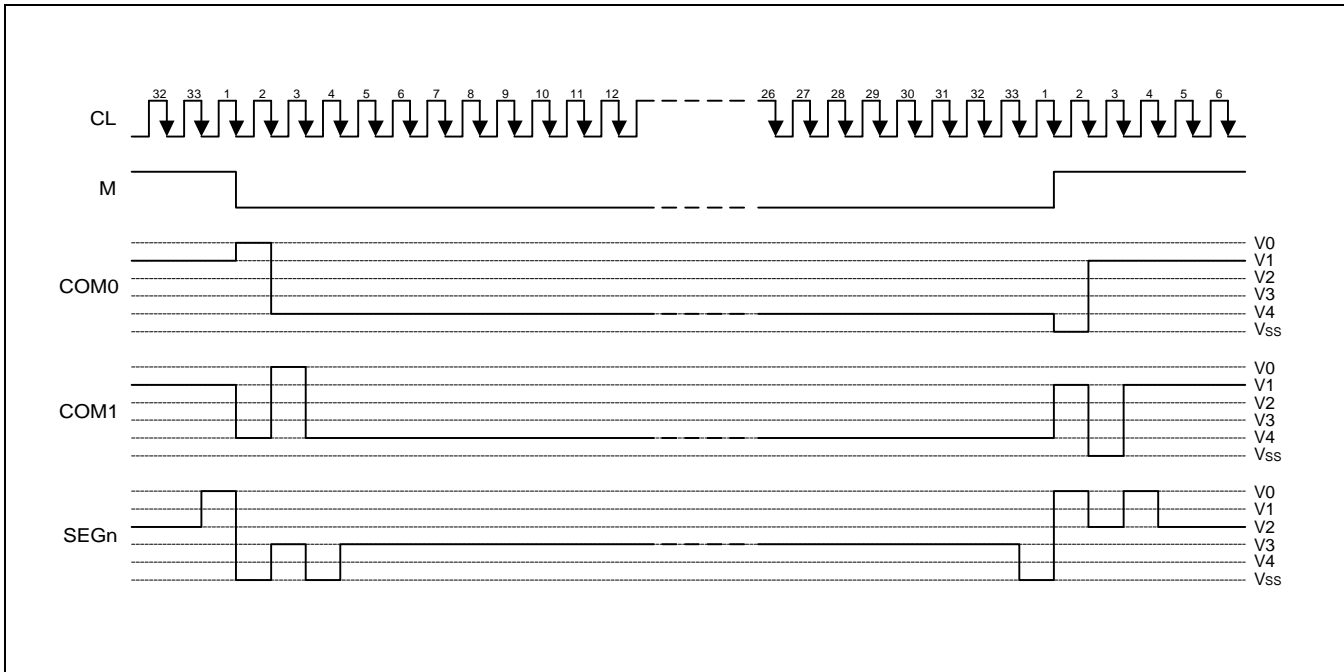


Figure 9. 2-frame AC Driving Waveform

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. SHL Select Instruction specifies the scanning direction of the common output pins.

Table 13. The Relationship between Duty Ratio and Common Output

| Duty | SHL | Common output pins | |
|------|-----|--------------------|------|
| | | COM0 to COM31 | COMS |
| 1/33 | 0 | COM0 to COM31 | COMS |
| | 1 | COM31 to COM0 | |

LCD DRIVER CIRCUIT

This driver circuit is configured by 34-channel (including 2 COMS channel) common driver and 100-channel segment driver. This LCD panel driver voltage depends on the combination of display data and M signal.

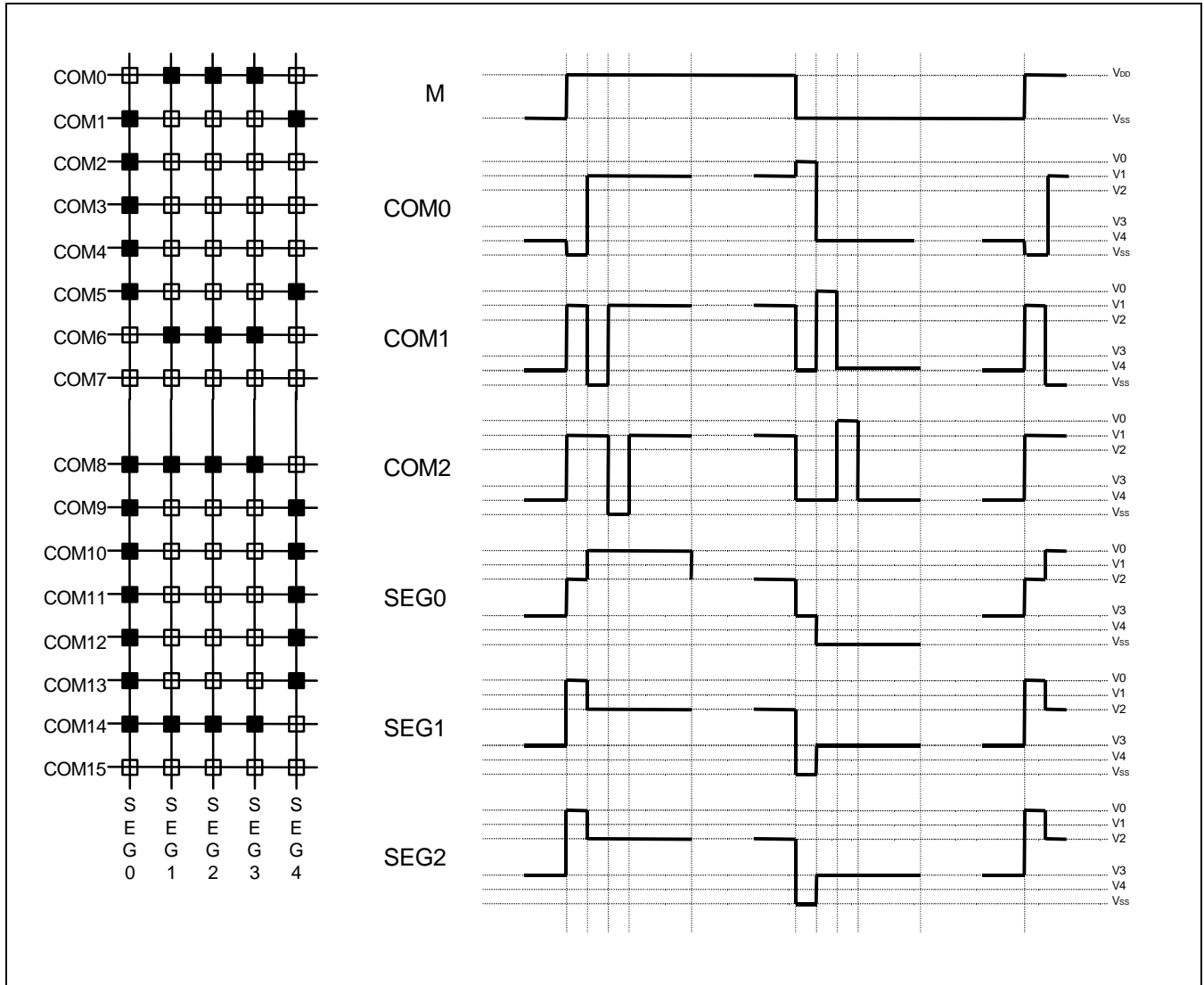


Figure 10. Segment and Common Timing

POWER SUPPLY CIRCUITS

The Power Supply circuits generate the voltage levels necessary to drive liquid crystal driver circuits with low-power consumption and the fewest components. There are voltage converter circuits, voltage regulator circuits, and voltage follower circuits. They are valid only in master operation and controlled by power control instruction. For details, refers to "Instruction Description". Table 14 shows the referenced combinations in using Power Supply circuits.

Table 14. Recommended Power Supply Combinations

| User setup | Power control (VC VR VF) | V/C circuits | V/R circuits | V/F circuits | VOUT | V0 | V1 to V4 |
|--|-----------------------------|-----------------|-----------------|-----------------|----------------|----------------|----------------|
| Only the internal power supply circuits are used | 1 1 1 | ON | ON | ON | Open | Open | Open |
| Only the voltage regulator circuits and voltage follower circuits are used | 0 1 1 | OFF | ON | ON | External input | Open | Open |
| Only the voltage follower circuits are used | 0 0 1 | OFF | OFF | ON | Open | External input | Open |
| Only the external power supply circuits are used | 0 0 0 | OFF | OFF | OFF | Open | External input | External input |

Voltage Converter Circuits

These circuits boost up the electric potential between VDD and VSS to 2, 3, or 4 times toward positive side and boosted voltage is outputted from VOUT pin.

[C1 = 1.0 to 4.7 nF]

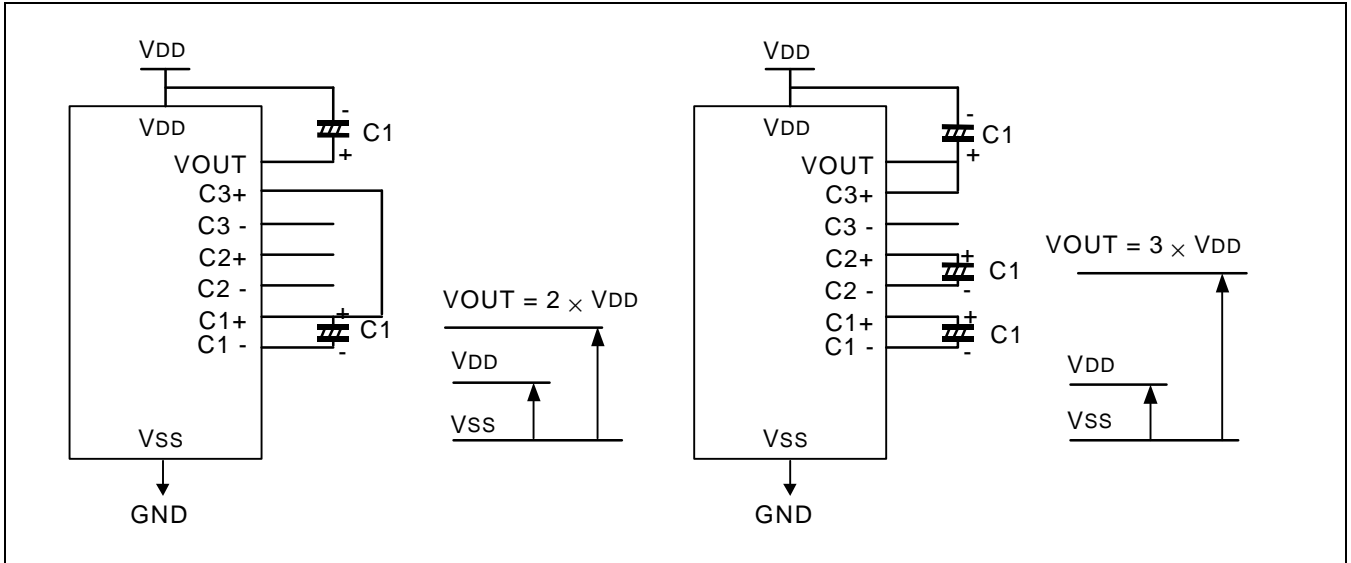


Figure 11. Two Times Boosting Circuit

Figure 12. Three Times Boosting Circuit

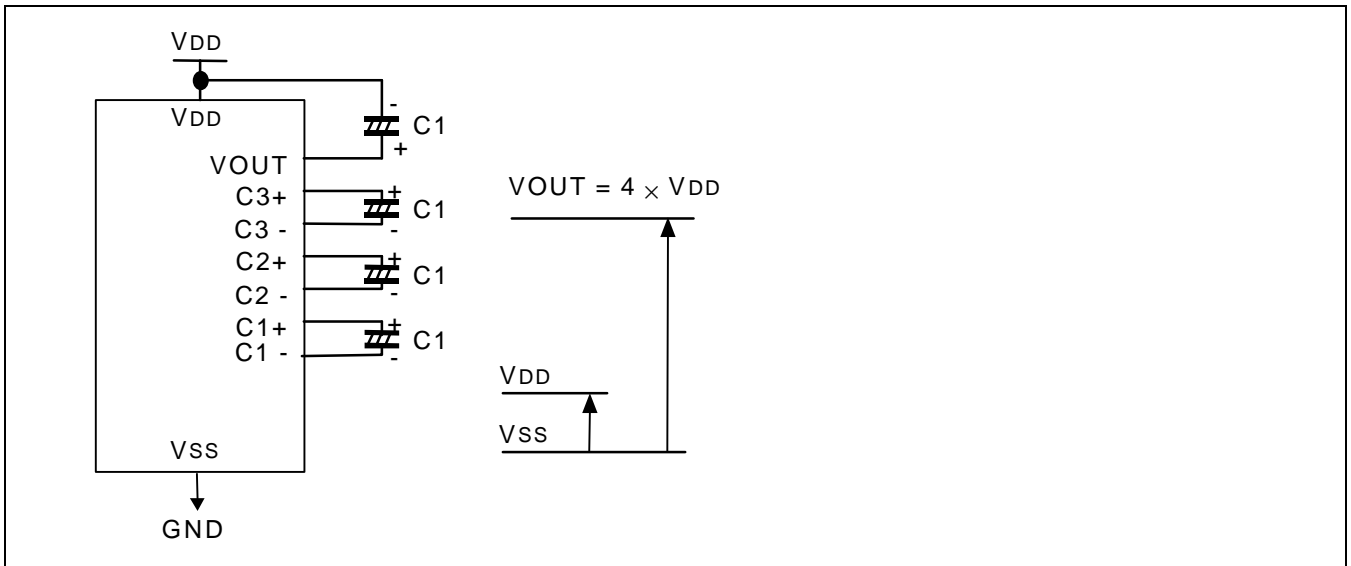


Figure 13. Four Times Boosting Circuit

Voltage Regulator Circuits

The function of the internal Voltage Regulator circuits is to determine liquid crystal operating voltage, V0, by adjusting resistors, Ra and Rb, within the range of |V0| < |VOUT|. Because VOUT is the operating voltage of operational-amplifier circuits shown in figure 14, it is necessary to be applied internally or externally.

For the Eq. 1, we determine V0 by Ra, Rb and VEV. The Ra and Rb are connected internally or externally by INTRS pin. And VEV called the voltage of electronic volume is determined by Eq. 2, where the parameter α is the value selected by instruction, "Set Reference Voltage Register", within the range 0 to 31. VREF voltage at Ta = 25°C is shown in table 15-1.

$$V0 = (1 + \frac{Rb}{Ra}) \times VEV \text{ [V] ----- (Eq. 1)}$$

$$VEV = (1 - \frac{(31 - \alpha)}{150}) \times VREF \text{ [V] ----- (Eq. 2)}$$

Table 15-1. VREF Voltage at Ta = 25°C

| TEMPS | Temp. coefficient | VREF [V] |
|-------|-------------------|----------|
| L | -0.05% / °C | 1.9 |
| H | -0.2% / °C | 2.1 |

Table 15-2. Reference Voltage Parameter (α)

| SV4 | SV3 | SV2 | SV1 | SV0 | Reference voltage parameter (α) |
|-----|-----|-----|-----|-----|---------------------------------|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : |
| : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 31 |

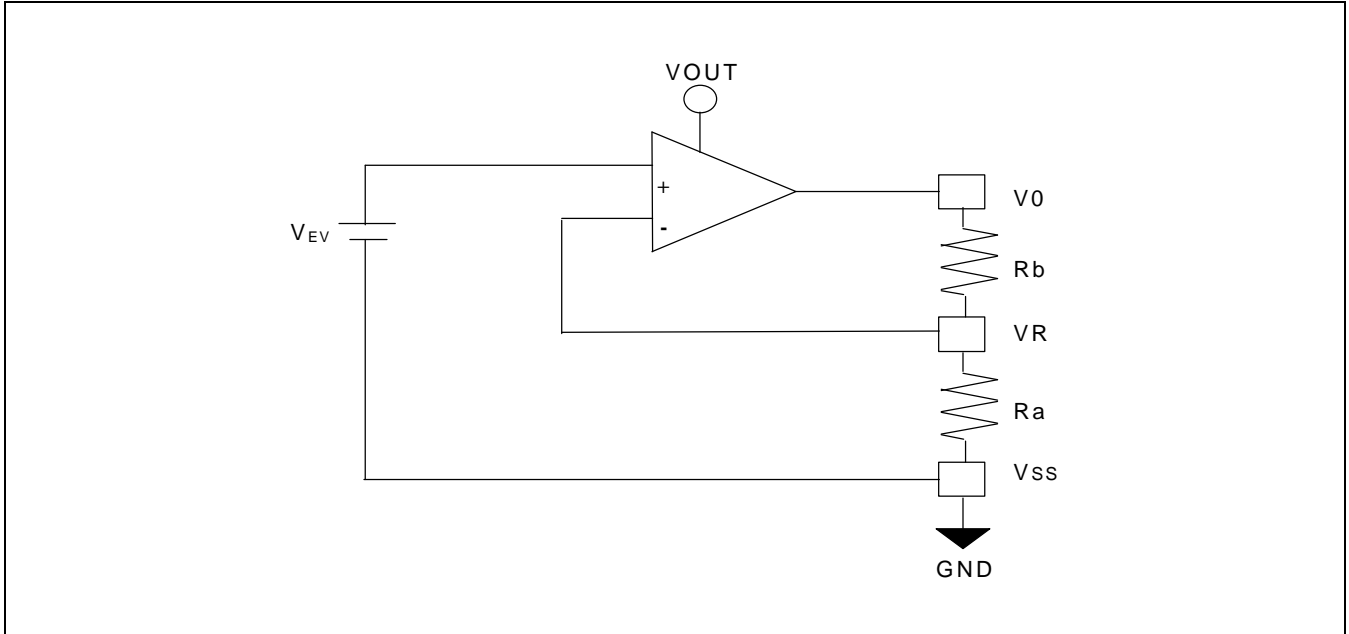


Figure 14. Internal Voltage Regulator Circuit

In Case of Using External Resistors, Ra and Rb

It is necessary to connect external regulator resistor Ra between VR and Vss, and Rb between V0 and VR.

Example: For the following requirements

1. LCD driver voltage, V0 = 8V
2. 5-bit reference voltage register = (1, 1, 1, 1, 1)
3. Maximum current flowing Ra, Rb = 1 uA

From Eq. 1

$$8 = \left(1 + \frac{R_b}{R_a} \right) \times V_{EV} \text{ [V]} \text{ ----- (Eq. 3)}$$

From Eq. 2

$$V_{EV} = \left(1 - \frac{(31 - 31)}{150} \right) \times 1.9 = 1.9 \text{ [V]} \text{ ----- (Eq. 4)}$$

From requirement 3.

$$\frac{8}{R_a + R_b} = 1 \text{ [uA]} \text{ ----- (Eq. 5)}$$

From equations Eq. 3, 4 and 5

Ra = 1.9 [MΩ]

Rb = 6.1 [MΩ]

The following table shows the range of V0 depending on the above requirements.

Table 16. V0 depending on Electronic Volume Level

| | Electronic volume level | | | | |
|----|-------------------------|-------|------|-------|----|
| | 0 | | 16 | | 31 |
| V0 | 6.33 | | 7.19 | | 8 |

Voltage Follower Circuits

VLCD voltage (V_0) is resistively divided into four voltage levels (V_1 , V_2 , V_3 and V_4) and those output impedance are converted by the Voltage Follower for increasing drive capability. Table 17 shows the relationship between V_1 to V_4 level and bias.

Table 17. The Relationship between V_1 to V_4 Level and Bias

| Duty ratio | LCD bias | V_1 | V_2 | V_3 | V_4 |
|------------|----------|--------------------|--------------------|--------------------|--------------------|
| 1/33 | 1/6 | $(5/6) \times V_0$ | $(4/6) \times V_0$ | $(2/6) \times V_0$ | $(1/6) \times V_0$ |
| | 1/5 | $(4/5) \times V_0$ | $(3/5) \times V_0$ | $(2/5) \times V_0$ | $(1/5) \times V_0$ |

REFERECE CIRCUIT EXAMPLES

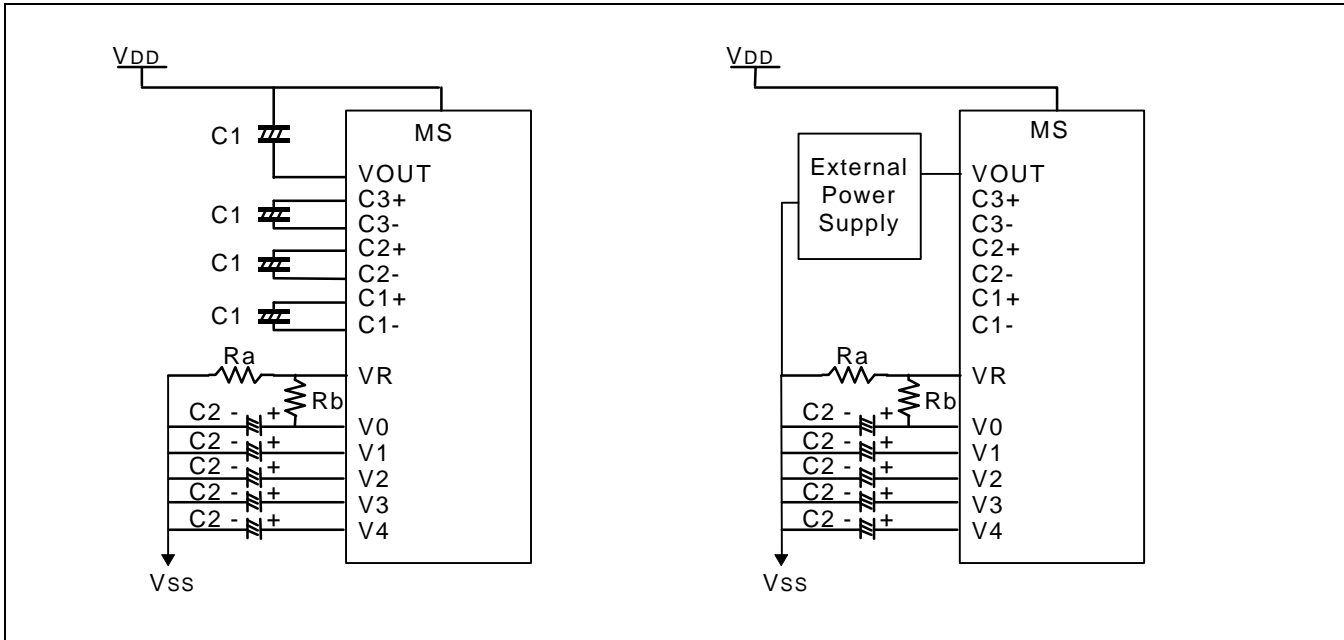


Figure 15. When Using all LCD Power Circuits (4-time V/C: ON, V/R: ON, V/F: ON)

Figure 16. When not Using V/C Circuit

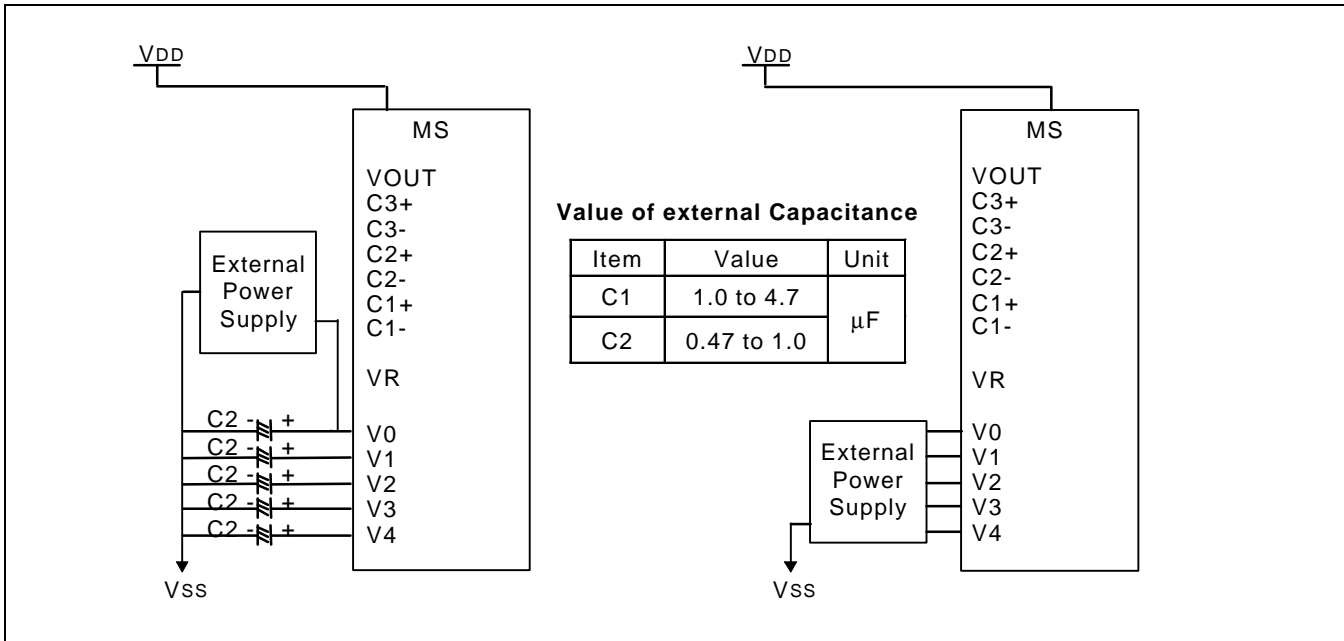


Figure 17. When Using some LCD Power Circuits (V/C: OFF, V/R: OFF, V/F: ON)

Figure 18. When not Using Internal LCD Power Supply Circuit

RESET CIRCUIT

Setting RESETB to "L" or Reset instruction can initialize internal function.
When RESETB becomes "L", following procedure is occurred.

- Display ON / OFF: OFF
- Entire display ON / OFF: OFF (normal)
- ADC select: OFF (normal)
- Reverse display ON / OFF: OFF (normal)
- Power control register (VC, VR, VF) = (0, 0, 0)
- LCD bias ratio: 1/6
- Read-modify-write: OFF
- SHL select: OFF (normal)
- Static indicator mode: OFF
- Display start line: 0 (first)
- Column address: 0
- Page address: 0
- Reference voltage set: off
- Reference voltage control register: (SV4, SV3, SV2, SV1, SV0) = (0, 0, 0, 0, 0)

When RESET instruction is issued, following procedure is occurred.

- Read-modify-write: OFF
- Static indicator mode: OFF
- SHL select: 0
- Display start line: 0 (first)
- Column address: 0
- Page address: 0
- Reference voltage set: OFF
- Reference voltage control register: (SV4, SV3, SV2, SV1, SV0) = (0, 0, 0, 0, 0)

While RESETB is "L" or reset instruction is executed, no instruction except read status could be accepted. Reset status appears at DB4. After DB4 becomes "L", any instruction can be accepted. RESETB must be connected to the reset pin of the MPU, and initialize the MPU and this LSI at the same time. The initialization by RESETB is essential before used.

INSTRUCTION DESCRIPTION

Table 18. Instruction Table

× : Don't care

| Instruction | RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Description |
|--------------------------------|----|----|------------|-----|-------|--------|-----|-----|-----|------|--|
| Read display data | 1 | 1 | Read data | | | | | | | | Read data from DDRAM |
| Write display data | 1 | 0 | Write data | | | | | | | | Write data into DDRAM |
| Read status | 0 | 1 | BUSY | ADC | ONOFF | RESETB | 0 | 0 | 0 | 0 | Read the internal status |
| Display ON / OFF | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | DON | Turn ON / OFF LCD panel When DON = 0: display OFF When DON = 1: display ON |
| Initial display line | 0 | 0 | 0 | 1 | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | Specify DDRAM line for COM0 |
| Set reference voltage mode | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Set reference voltage mode |
| Set reference voltage register | 0 | 0 | 1 | 0 | 0 | SV4 | SV3 | SV2 | SV1 | SV0 | Set reference voltage register |
| Set page address | 0 | 0 | 1 | 0 | 1 | 1 | P3 | P2 | P1 | P0 | Set page address |
| Set column address MSB | 0 | 0 | 0 | 0 | 0 | 1 | 0 | Y6 | Y5 | Y4 | Set column address MSB |
| Set column address LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | Y3 | Y2 | Y1 | Set column address LSB |
| ADC select | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ADC | Select SEG output direction When ADC = 0: normal direction (SEG0→SEG99) When ADC = 1: reverse direction (SEG99→SEG0) |
| Reverse display ON / OFF | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | REV | Select normal / reverse display When REV = 0: normal display When REV = 1: reverse display |
| Entire display ON / OFF | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | EON | Select normal/ entire display ON When EON = 0: normal display. When EON = 1: entire display ON |
| LCD bias select | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | BIAS | Select LCD bias |
| Set modify-read | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Set modify-read mode |
| Reset modify-read | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | release modify-read mode |
| Reset | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Initialize the internal functions |
| SHL select | 0 | 0 | 1 | 1 | 0 | 0 | SHL | × | × | × | Select COM output direction When SHL = 0: normal direction (COM0→COM31) When SHL = 1: reverse direction (COM31→COM0) |
| Power control | 0 | 0 | 0 | 0 | 1 | 0 | 1 | VC | VR | VF | Control power circuit operation |
| Set static indicator register | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | SI | Set static indicator register SI = 0 (OFF), SI = 1 (ON) |
| Power save | - | - | - | - | - | - | - | - | - | - | Compound instruction of display OFF and entire display ON |
| Test instruction | 0 | 0 | 1 | 1 | 1 | 1 | × | × | × | × | <i>Don't use this instruction.</i> |

Read Display Data

8-bit data from Display Data RAM specified by the column address and page address could be read by this instruction. As the column address is increased by 1 automatically after each this instruction, the microprocessor can continuously read data from the addressed page. A dummy read is required after loading an address into the column address register. Display data cannot be read through the serial interface.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----------|-----|-----|-----|-----|-----|-----|-----|
| 1 | 1 | Read data | | | | | | | |

Write Display Data

8-bit data of display data from the microprocessor can be written to the RAM location specified by the column address and page address. The column address is increased by 1 automatically so that the microprocessor can continuously write data to the addressed page.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------------|-----|-----|-----|-----|-----|-----|-----|
| 1 | 0 | Write data | | | | | | | |

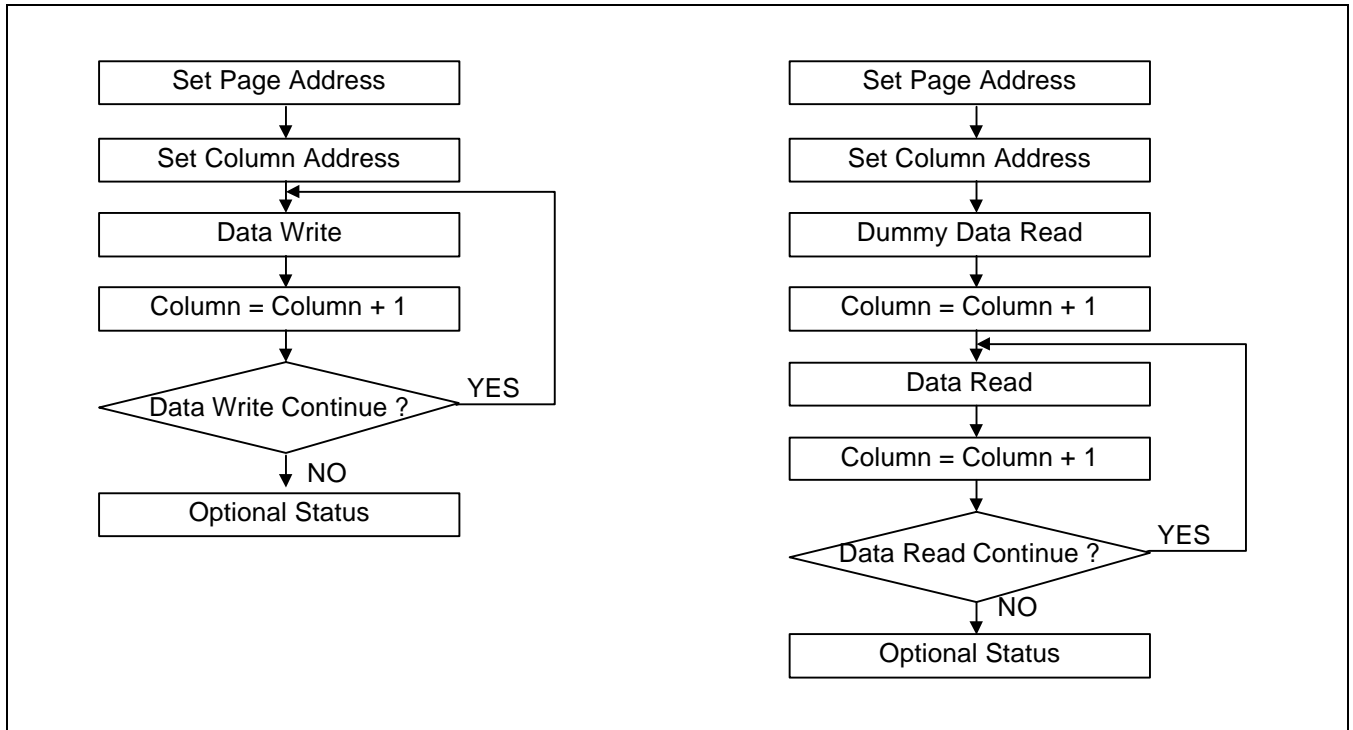


Figure 19. Sequence for Writing Display Data

Figure 20. Sequence for Reading Display Data

Read Status

Indicates the internal status of the KS0715

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|------|-----|--------|--------|-----|-----|-----|-----|
| 0 | 1 | BUSY | ADC | ON/OFF | RESETB | 0 | 0 | 0 | 0 |

| Flag | Description |
|----------|--|
| BUSY | The device is busy when internal operation or reset Any instruction is rejected until BUSY goes Low. 0: chip is active, 1: chip is being busy. |
| ADC | Indicates the relationship between RAM column address and segment driver. 0: reverse direction (SEG99 → SEG0), 1: normal direction (SEG0 → SEG99) |
| ON / OFF | Indicates display ON / OFF status 0: display ON, 1: display OFF |
| RESETB | Indicates the initialization is in progress by RESETB signal 0: chip is active, 1: chip is being reset |

Display ON / OFF

Turns the display ON or OFF

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | DON |

DON = 1: display ON

DON = 0: display OFF

Initial Display Line

Sets the line address of display RAM to determine the Initial Display Line. The RAM display data is displayed at the top row (COM0 when SHL = L, COM31 when SHL = H) of LCD panel.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 1 | ST5 | ST4 | ST3 | ST2 | ST1 | ST0 |

| ST5 | ST4 | ST3 | ST2 | ST1 | ST0 | Line address |
|-----|-----|-----|-----|-----|-----|--------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 1 | 1 | 1 | 1 | 1 | 1 | 63 |

Reference Voltage Select

Consists of 2-byte Instruction

The 1st instruction sets reference voltage mode, the 2nd one updates the contents of reference voltage register. After second instruction, reference voltage mode is released.

The 1st Instruction: Set Reference Voltage Select Mode

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

The 2nd Instruction: Set Reference Voltage Register

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 0 | SV4 | SV3 | SV2 | SV1 | SV0 |

| SV4 | SV3 | SV2 | SV1 | SV0 | Reference voltage parameter (α) |
|-----|-----|-----|-----|-----|--|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : |
| : | : | : | : | : | : |
| 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 31 |

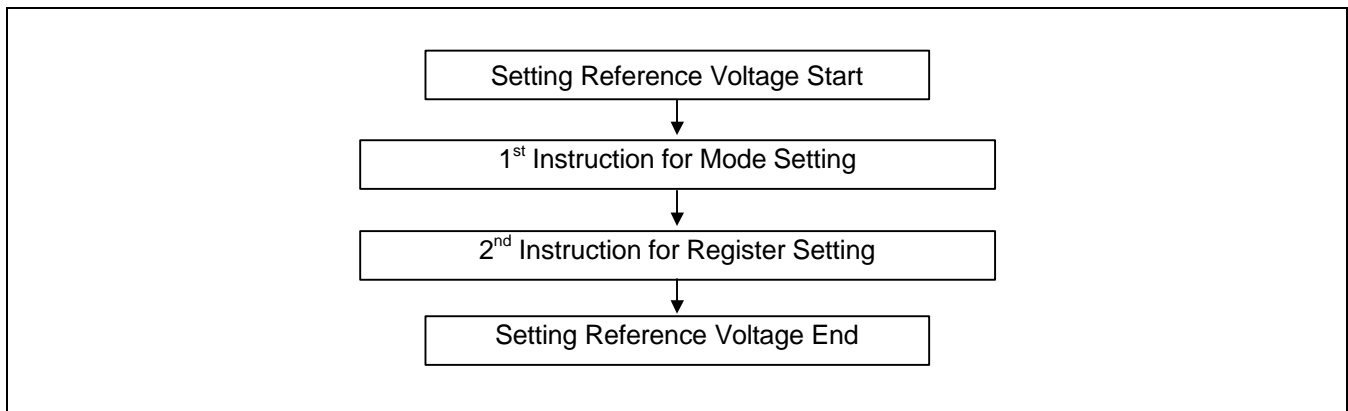


Figure 21. Sequence for Setting the Reference Voltage

Set Page Address

Sets the Page Address of display data RAM from the microprocessor into the Page Address register. Any RAM data bit can be accessed when its Page Address and column address are specified. Along with the column address, the Page Address defines the address of the display RAM to write or read display data. Changing the Page Address doesn't effect to the display status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 1 | P3 | P2 | P1 | P0 |

| P3 | P2 | P1 | P0 | Page |
|----|----|----|----|------|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |

Set Column Address

Sets the Column Address of display RAM from the microprocessor into the column address register. Along with the Column Address, the Column Address defines the address of the display RAM to write or read display data. When the microprocessor reads or writes display data to or from display RAM, Column Addresses are automatically increased.

Set Column Address MSB

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | Y6 | Y5 | Y4 |

Set Column Address LSB

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | Y3 | Y2 | Y1 | Y0 |

| Y6 | Y5 | Y4 | Y3 | Y2 | Y1 | Y0 | Column address |
|----|----|----|----|----|----|----|----------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| : | : | : | : | : | : | : | : |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 98 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 99 |

ADC Select

Changes the relationship between RAM column address and segment driver. The direction of segment driver output pins could be reversed by software. This makes IC layout flexible in LCD module assembly.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | ADC |

ADC = 0: normal direction (SEG0 → SEG99)

ADC = 1: reverse direction (SEG99 → SEG0)

Reverse Display ON / OFF

Reverses the display status on LCD panel without rewriting the contents of the display data RAM.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | REV |

| REV | RAM bit data = "1" | RAM bit data = "0" |
|-------------|------------------------------|------------------------------|
| 0 (normal) | LCD pixel is illuminated | LCD pixel is not illuminated |
| 1 (reverse) | LCD pixel is not illuminated | LCD pixel is illuminated |

Reverse Display ON / OFF

Forces the whole LCD points to be turned on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This instruction has priority over the reverse display ON / OFF instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | EON |

EON = 0: normal display

EON = 1: entire display ON

Select LCD Bias

Selects LCD bias ratio of the voltage required for driving the LCD.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|------|
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Bias |

| Duty ratio | LCD bias | |
|------------|----------|----------|
| | Bias = 0 | Bias = 1 |
| 1/33 | 1/6 | 1/5 |

Set Modify-read

This instruction stops the automatic increment of the column address by the read display data instruction, but the column address is still increased by the write display data instruction. And it reduces the load of microprocessor when the data of a specific area is repeatedly changed during cursor blinking or others. This mode is canceled by the reset Modify-read instruction.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |

Reset Modify-read

This instruction cancels the Modify-read mode, and makes the column address return to its initial value just before the set Modify-read instruction is started.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 |

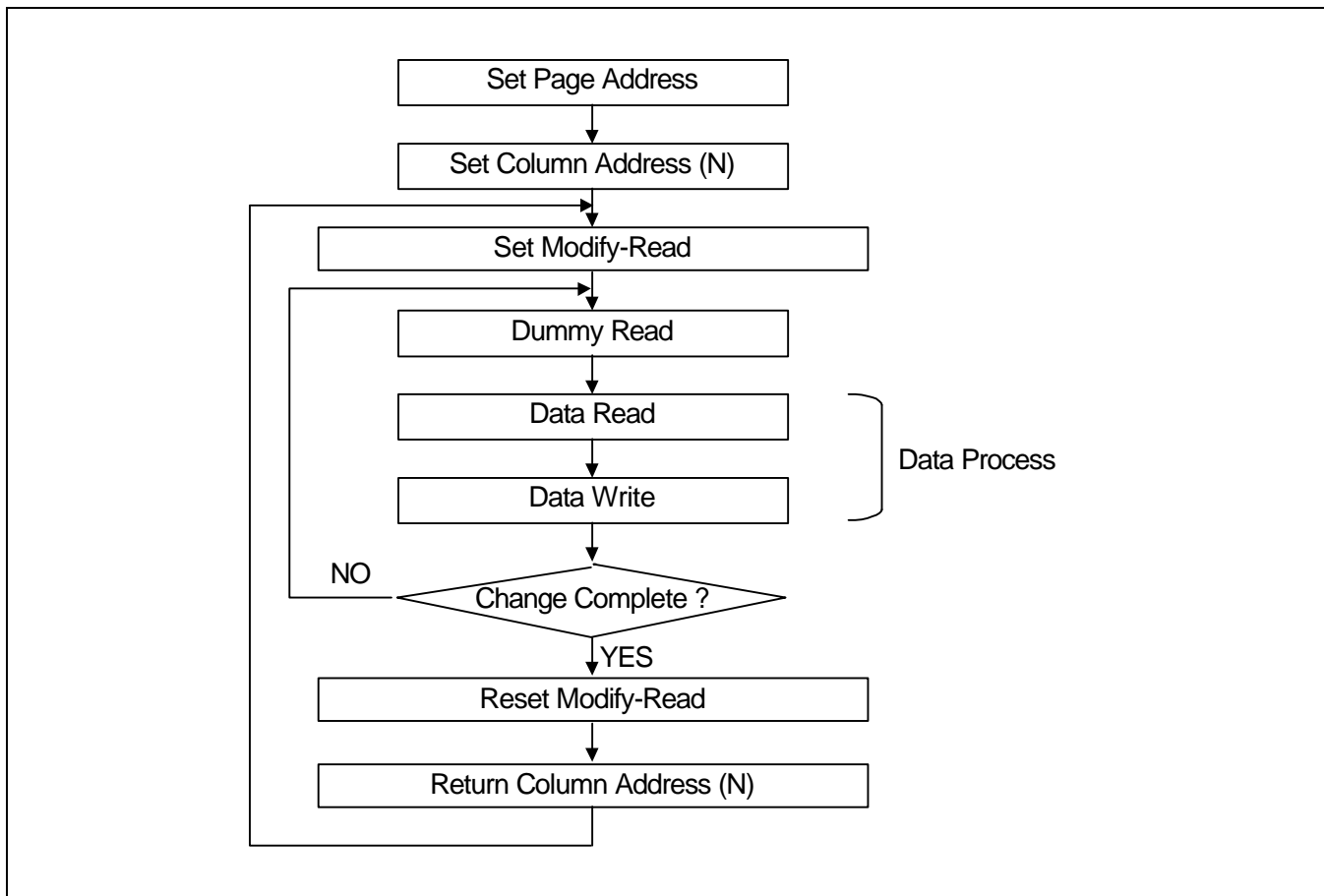


Figure 22. Sequence for Cursor Display

Reset

This instruction Resets initial display line, column address, page address, and common output status select to their initial status, but does not affect the contents of display data RAM. This instruction cannot initialize the LCD power supply, which is initialized by the RESETB pin.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |

SHL Select

COM output scanning direction is selected by this instruction which determines the LCD driver output status.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 1 | 0 | 0 | SHL | × | × | × |

× : Don't care

SHL = 0: normal direction (COM0 → COM31)

SHL = 1: reverse direction (COM31 → COM0)

Power Control

Selects one of eight power circuit functions by using 3-bit register. An external power supply and part of internal power supply functions can be used simultaneously.

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | VC | VR | VF |

| VC | VR | VF | Status of internal power supply circuits |
|----|----|----|---|
| 0 | | | Internal voltage converter circuit is OFF |
| 1 | | | Internal voltage converter circuit is ON |
| | 0 | | Internal voltage regulator circuit is OFF |
| | 1 | | Internal voltage regulator circuit is ON |
| | | 0 | Internal voltage follower circuit is OFF |
| | | 1 | Internal voltage follower circuit is ON |

Set Static Indicator State

This instruction sets the Static Indicator ON / OFF. When it is on, the static indicator operates and blinks at an interval of approximately 1second.

Set Static Indicator Register

| RS | RW | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
|----|----|-----|-----|-----|-----|-----|-----|-----|-----|
| 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | SI |

| SI | Status of static indicator output |
|----|-----------------------------------|
| 0 | OFF |
| 1 | ON (about 1 second blinking) |

Power Save (Compound Instruction)

If the entire display ON / OFF instruction is issued during the display OFF state, KS0715 enters the Power Save status to reduce the power consumption to the static power consumption value. According to the status of static indicator mode, Power Save is entered to one of two modes (sleep and standby mode). When static indicator mode is ON, standby mode is issued, when OFF, sleep mode is issued. Power Save mode is released by the display ON & entire display OFF instruction.

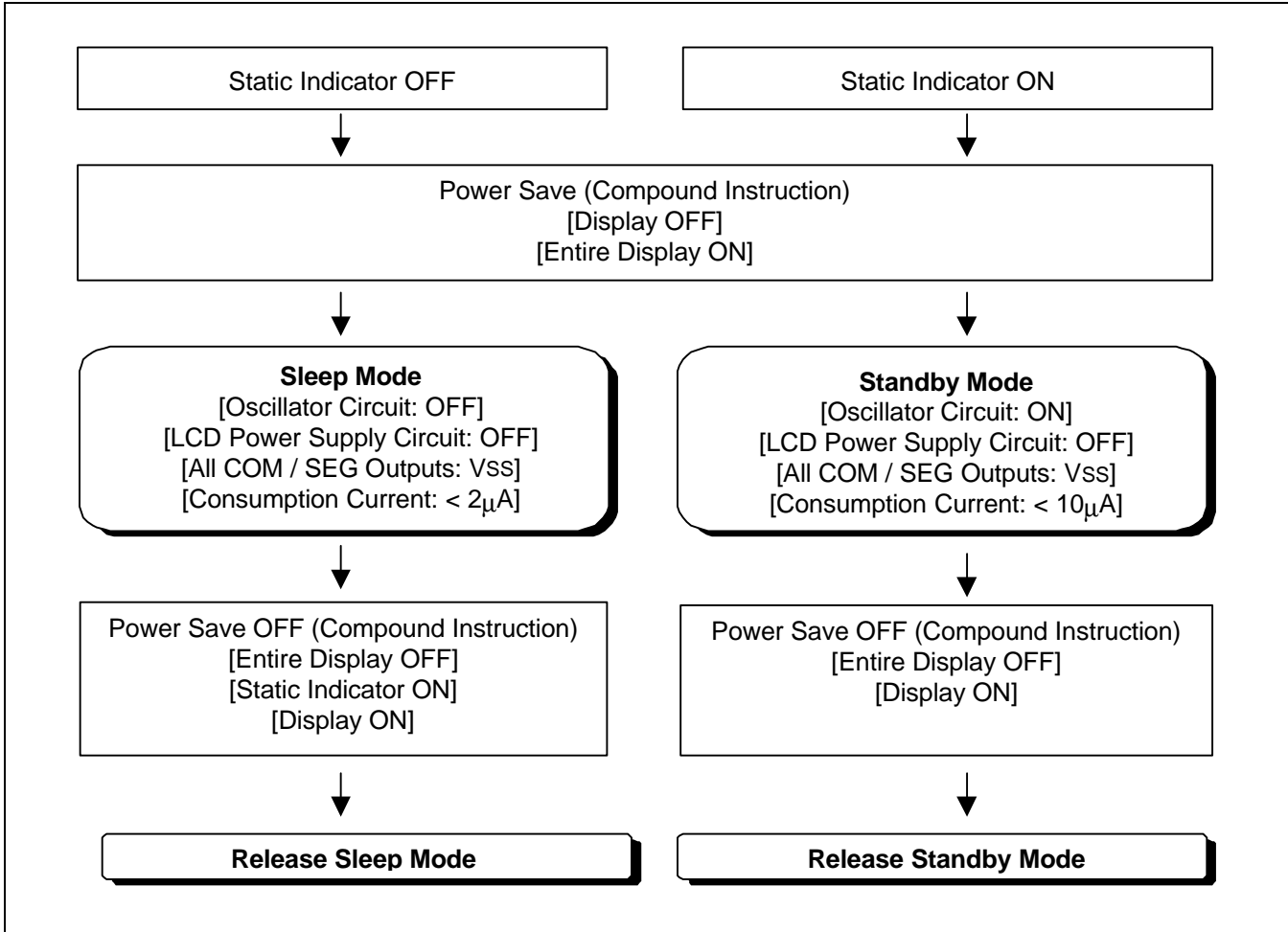


Figure 23. Power Save Routine

Referential Instruction Setup Flow (1)

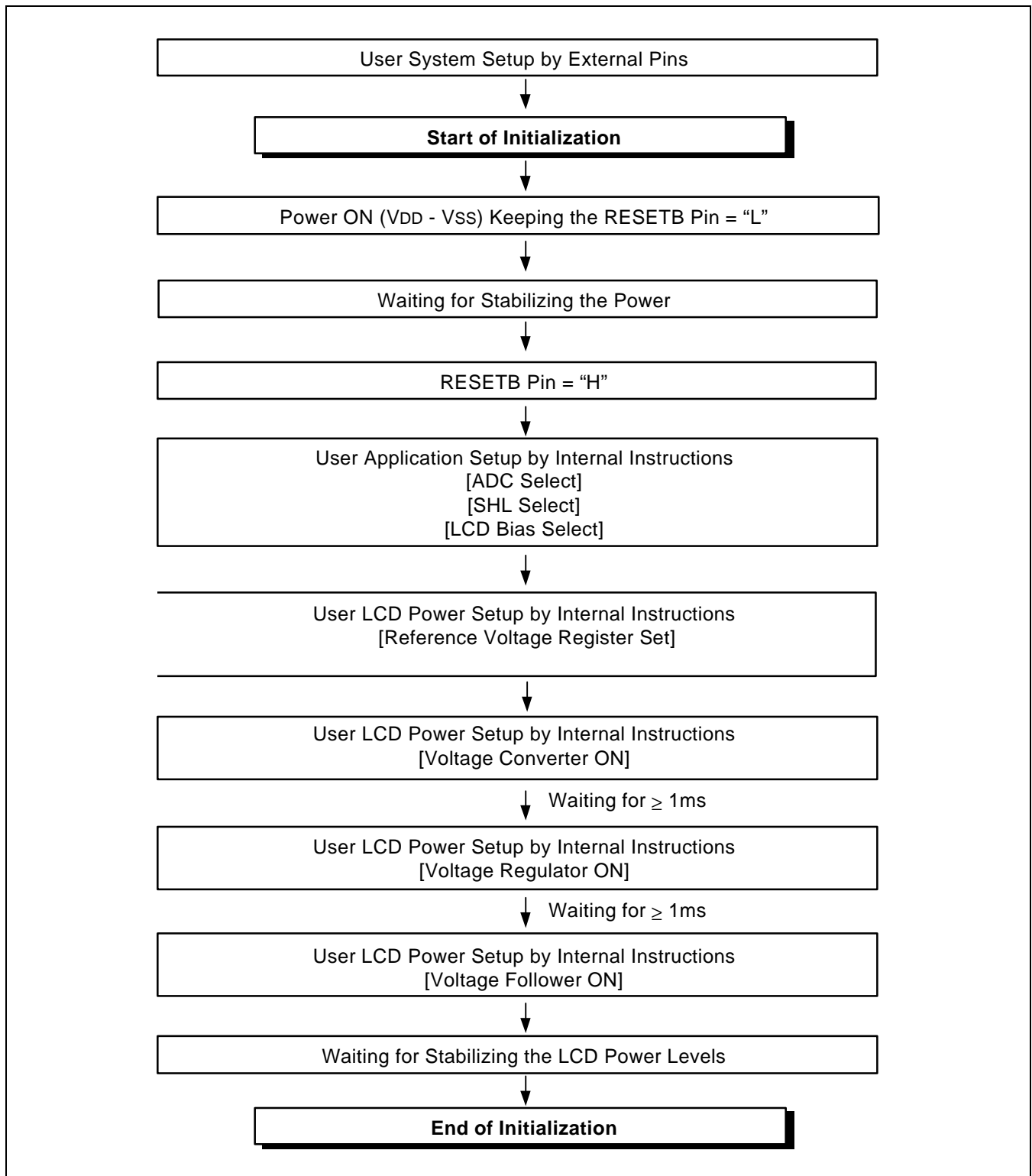


Figure 24. Initializing with the Built-in Power Supply Circuits

Referential Instruction Setup Flow (2)

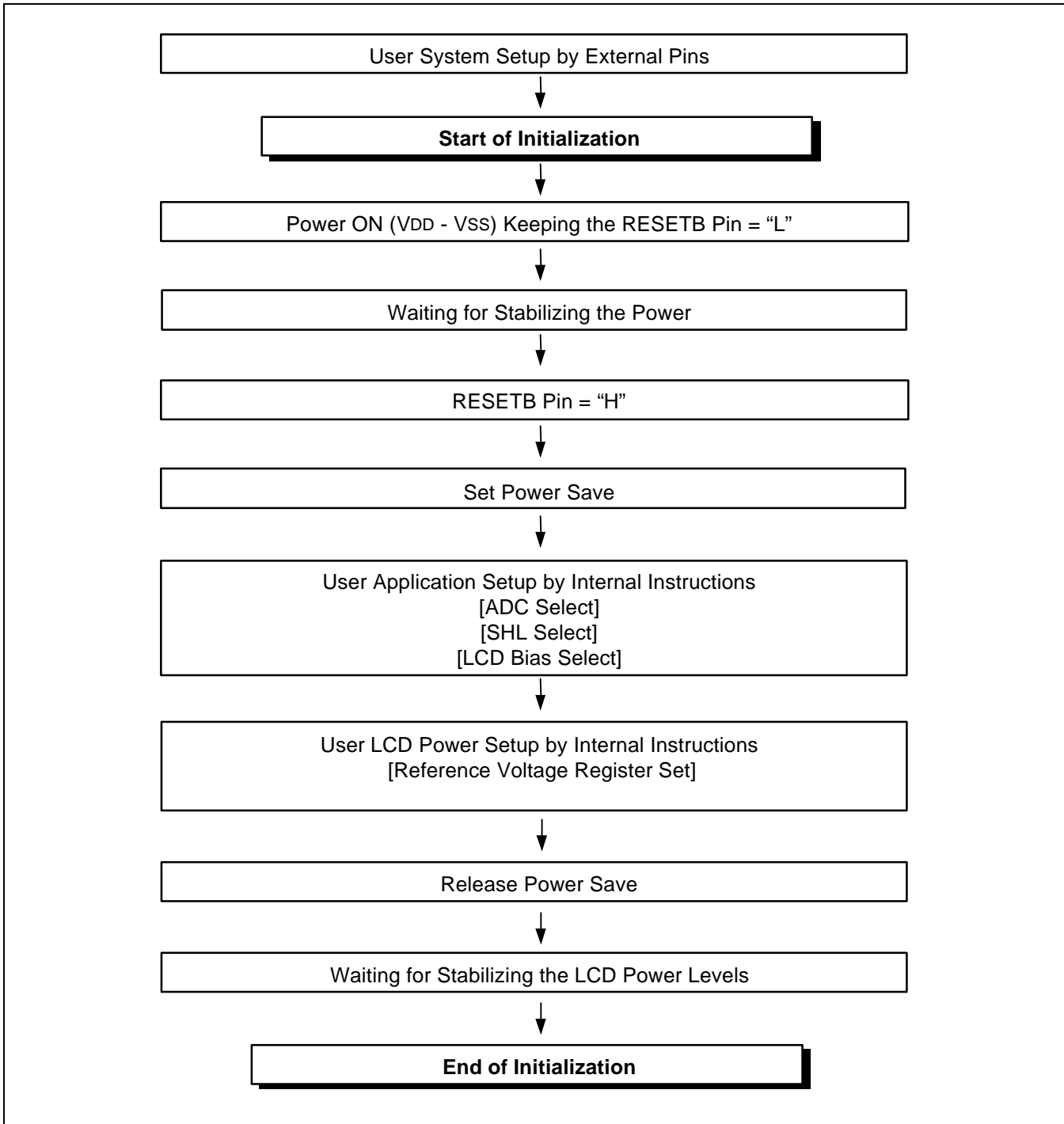


Figure 25. Initializing without the Built-in Power Supply Circuits

Referential Instruction Setup Flow (3)

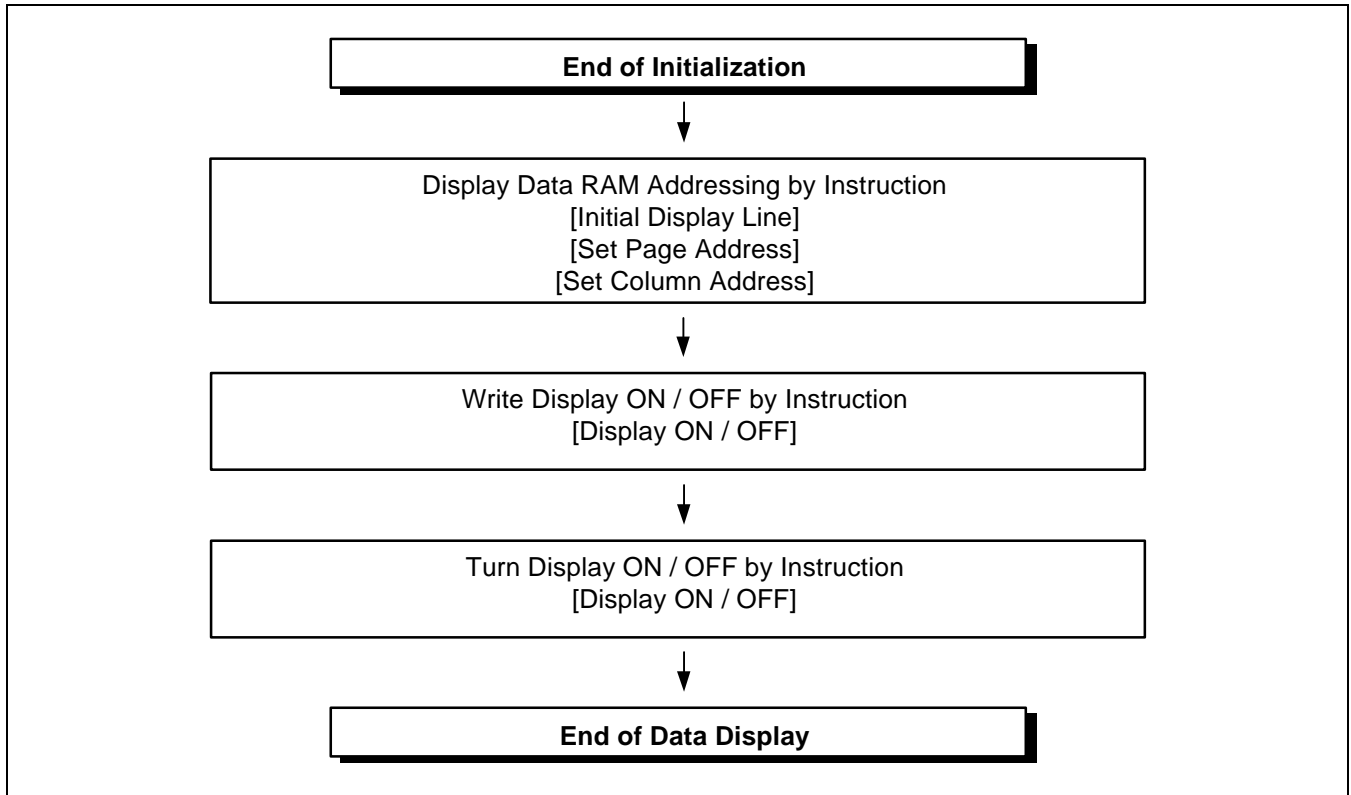


Figure 26. Data Displaying

Referential Instruction Setup Flow (4)

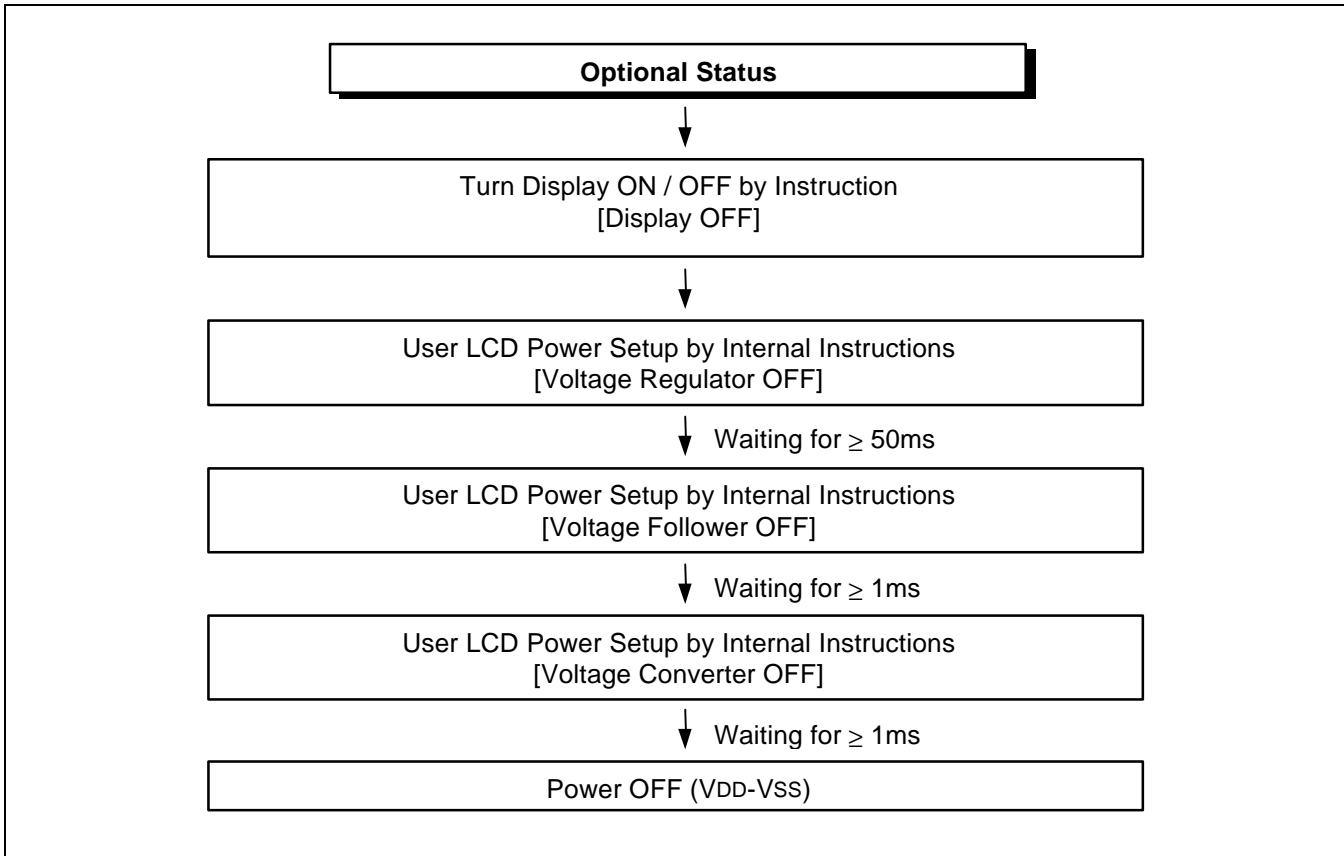


Figure 27. Power OFF

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Table 19. Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|-----------------------------|------------------|-------------------------------|------|
| Supply voltage range | V _{DD} | - 0.3 to +7.0 | V |
| | V _{LCD} | - 0.3 to +17.0 | V |
| Input voltage range | V _{IN} | - 0.3 to V _{DD} +0.3 | V |
| Operating temperature range | T _{OPR} | - 40 to +85 | °C |
| Storage temperature range | T _{STR} | - 55 to +125 | °C |

NOTES:

1. V_{DD} and V_{LCD} are based on V_{SS} = 0V.
2. Voltages V₀ ≥ V₁ ≥ V₂ ≥ V₃ ≥ V₄ ≥ V_{SS} must always be satisfied. (V_{LCD} = V₀ – V_{SS})
3. If supply voltage exceeds its absolute maximum range, this LSI may be damaged permanently.
It is desirable to use this LSI under electrical characteristic conditions during general operation.
Otherwise, this LSI may malfunction or reduced LSI reliability may result.

DC CHARACTERISTICS

Table 20. DC Characteristics

($V_{SS} = 0V$, $V_{DD} = 2.4$ to $3.6V$, $T_a = -40$ to $85^{\circ}C$)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used | | | |
|-------------------------------------|------------|--|---------------------|-------------|-------------|-------------|-----------------|-----|-----|-------|
| Operating voltage (1) | V_{DD} | | 2.4 | - | 3.6 | V | V_{DD} *1 | | | |
| Operating voltage (2) | V_0 | | 4.0 | - | 15.0 | V | V_0 *2 | | | |
| Input voltage | High | V_{IH} | $0.8V_{DD}$ | - | V_{DD} | V | *3 | | | |
| | Low | V_{IL} | V_{SS} | - | $0.2V_{DD}$ | | | | | |
| Output voltage | High | V_{OH} | $I_{OH} = -0.5mA$ | $0.8V_{DD}$ | - | V_{DD} | V | *4 | | |
| | Low | V_{OL} | $I_{OL} = 0.5mA$ | V_{SS} | - | $0.2V_{DD}$ | | | | |
| Input leakage current | I_{IL} | $V_{IN} = V_{DD}$ or V_{SS} | - 1.0 | - | + 1.0 | μA | *5 | | | |
| Output leakage current | I_{OZ} | $V_{IN} = V_{DD}$ or V_{SS} | - 3.0 | - | + 3.0 | μA | *6 | | | |
| LCD driver ON resistance | R_{ON} | $T_a = 25^{\circ}C$, $V_0 = 8V$ | - | 2.0 | 3.0 | $k\Omega$ | SEGn COMn *7 | | | |
| Oscillator frequency (1) | Internal | f_{OSC} | $T_a = 25^{\circ}C$ | | | 17 | 22.5 | 27 | kHz | CL *8 |
| | External | f_{CL} | 2.13 | 2.81 | 3.37 | | | | | |
| Voltage converter input voltage | V_{DD} | $\times 2$ | 2.4 | - | 3.6 | V | V_{DD} | | | |
| | | $\times 3$ | 2.4 | - | 3.6 | | | | | |
| | | $\times 4$ | 2.4 | - | 3.6 | | | | | |
| Voltage converter output voltage | V_{OUT} | $\times 2 / \times 3 / \times 4$ voltage conversion (no-load) | 95 | 99 | - | % | V_{OUT} | | | |
| Voltage regulator operating voltage | V_{OUT} | | 4.0 | - | 15.0 | V | V_{OUT} | | | |
| Voltage follower operating voltage | V_0 | | 4.0 | - | 15.0 | V | V_0 *9 | | | |
| Reference voltage | V_{REF0} | $T_a = 25^{\circ}C$ | -0.05%/°C | 1.84 | 1.9 | 1.96 | V | *10 | | |
| | V_{REF1} | | -0.2%/°C | 2.04 | 2.1 | 2.16 | V | *10 | | |

Dynamic Current Consumption (1): when the Built-in Power Circuit is OFF (At Operate Mode)

(Ta = 25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used |
|---------------------------------|--------|---|------|------|------|------|----------|
| Dynamic current consumption (1) | IDD1 | VDD = 3.0V V0 – VSS = 8.0V Display OFF, checker pattern | - | 5 | 20 | μA | *11 |

Dynamic Current Consumption (2): when the built-in power circuit is ON (At operate mode)

(Ta = 25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used |
|---------------------------------|--------|--|------|------|------|------|----------|
| Dynamic current consumption (2) | IDD2 | VDD = 3.0V, quad boosting, V0 – VSS = 8.0V, 1/65 duty ratio, Display OFF, checker pattern Normal power mode | - | 47 | 70 | μA | *12 |
| | | VDD = 3.0V, quad boosting, V0 – VSS = 8.0V, Display ON, checker pattern Normal power mode | - | 75 | 100 | | |

Current Consumption during Power Save mode

(Ta = 25°C)

| Item | Symbol | Condition | Min. | Typ. | Max. | Unit | Pin used |
|--------------|--------|----------------|------|------|------|------|----------|
| Sleep mode | IDDS1 | During sleep | - | - | 2.0 | μA | |
| Standby mode | IDDS2 | During standby | - | - | 10.0 | μA | |

Table 21. The relationship between oscillation frequency and frame frequency

| Duty ratio | Item | fCL | fM |
|------------|--|----------------------|--------------------------------|
| 1/33 | On-chip oscillator circuit is used | $\frac{f_{osc}}{8}$ | $\frac{f_{osc}}{16 \times 33}$ |
| | On-chip oscillator circuit is not used | External input (fCL) | $\frac{f_{osc}}{2 \times 33}$ |

(fosc: oscillation frequency, fCL: display clock frequency, fM: LCD AC signal frequency)

[* Remark Solves]

- *1. Though the wide range of operating voltages is guaranteed, a spike voltage change may affect the voltage assurance during access from the MPU.
- *2. In case of external power supply is applied.
- *3. CS1B, CS2, RS, DB0 to DB7, E_RD, RW_WR, RESETB, MS, MI, PS, TEMPS, CL, M, DISP pins.
- *4. DB0 to DB7, M, FRS, DISP, CL pins.
- *5. CS1B, CS2, RS, DB[7:0], E_RD, RW_WR, RESETB, MS, MI, PS, TEMPS, CL, M, DISP pins.
- *6. Applies when the DB[7:0], M, DISP, and CL pins are in high impedance.
- *7. Resistance value when ± 0.1 [mA] is applied during the ON status of the output pin SEGn or COMn.
RON= $\Delta V / 0.1$ [k Ω] (ΔV : voltage change when ± 0.1 [mA] is applied in the ON status.)
- *8. See table 21 for the relationship between oscillation frequency and frame frequency.
- *9. The voltage regulator circuit adjusts V0 within the voltage follower operating voltage range.
- *10. On-chip reference voltage source of the voltage regulator circuit to adjust V0.
- *11,12. Applies to the case where the on-chip oscillation circuit is used and no access is made from the MPU.
The current consumption, when the built-in power supply circuit is ON or OFF.
The current flowing through voltage regulation resistors (Ra and Rb) is not included.
It does not include the current of the LCD panel capacity, wiring capacity, etc.

REFERENCE DATA

IDD1 vs. VDD

- Test Condition: Temperature (25°C & 85°C), V0 = 8V (External), TEMPS = 'L', 1/33 Duty, Ra = 1 [MΩ], Rb = 3 [MΩ], Normal Power Mode

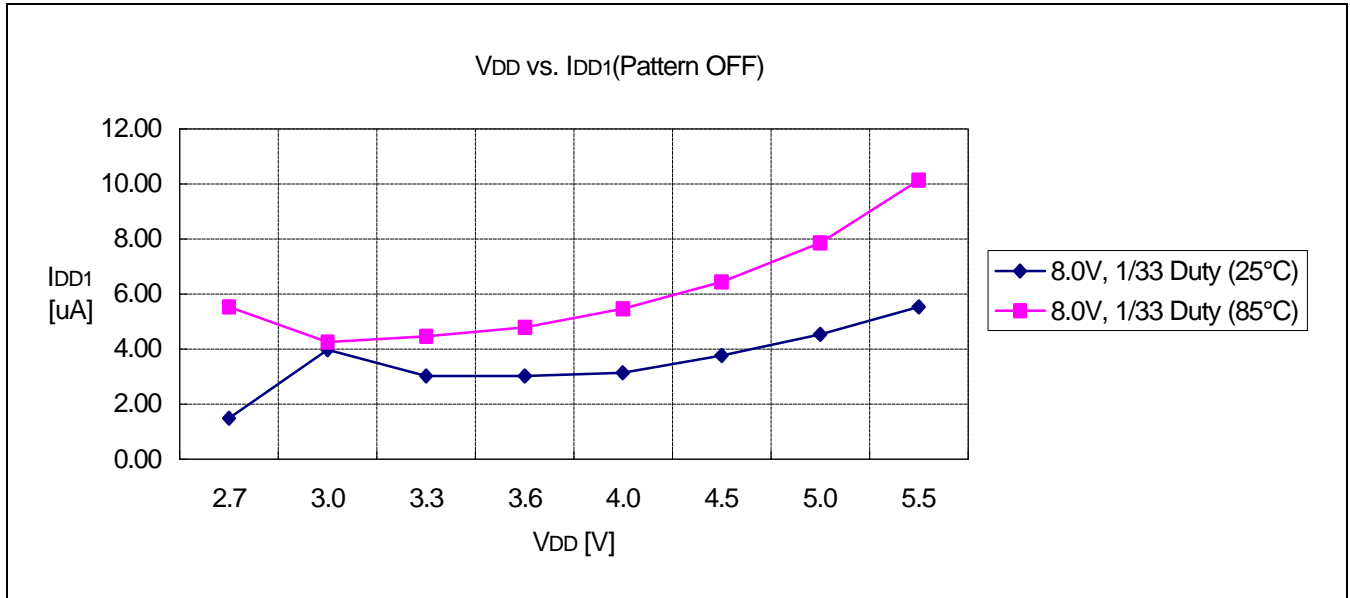


Figure 28. Display Pattern is OFF

IDD2 vs. VDD

- Test Condition: Temperature (25°C & 85°C), Quad boosting, RR = 6, EV = 32, TEMPS = 'L', 1/33 duty, Ra = 1 [MΩ], Rb = 3 [MΩ], Normal Power Mode

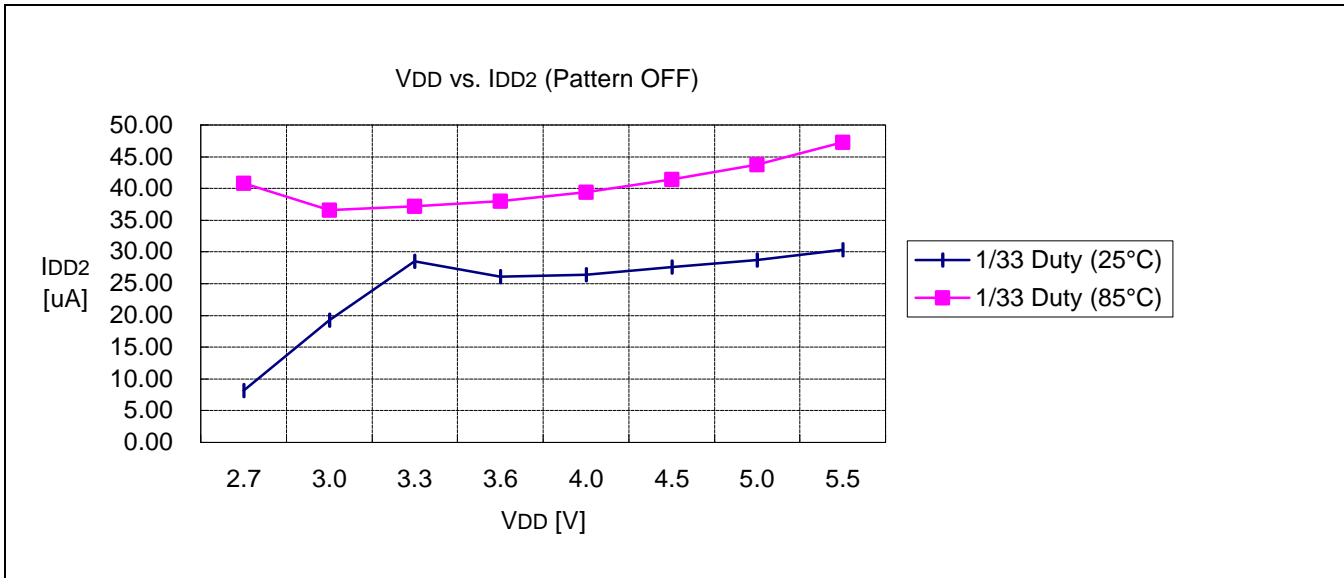


Figure 29. Display Pattern is OFF

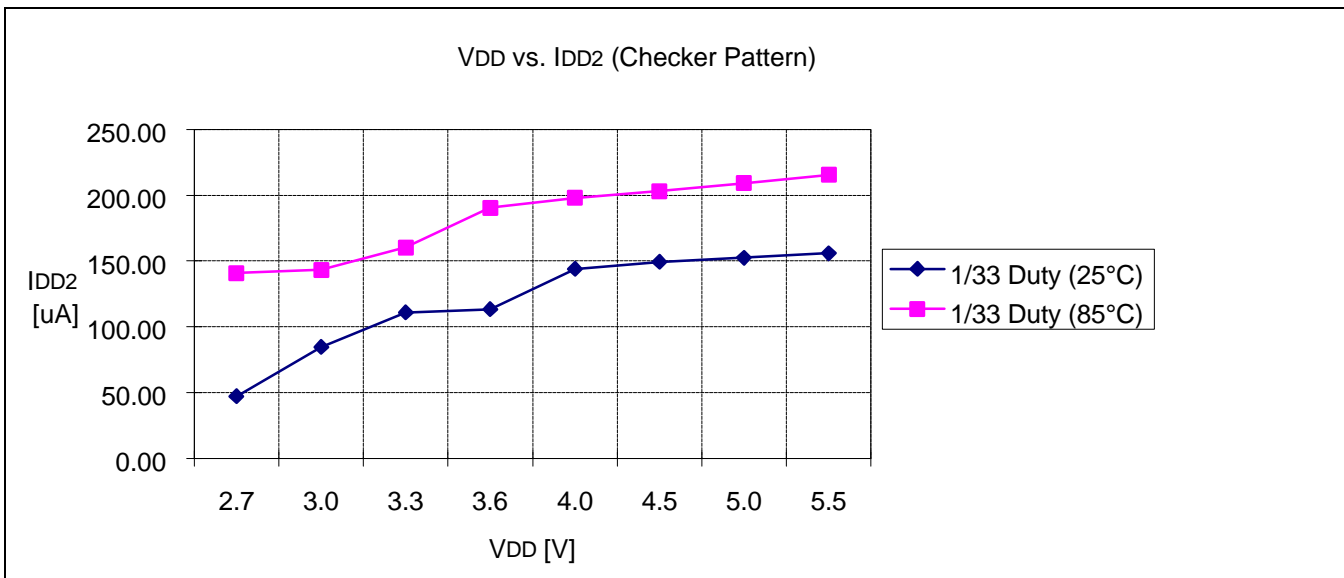


Figure 30. Display Pattern is Checker

AC CHARACTERISTICS

Read / Write Characteristics (8080-series MPU)

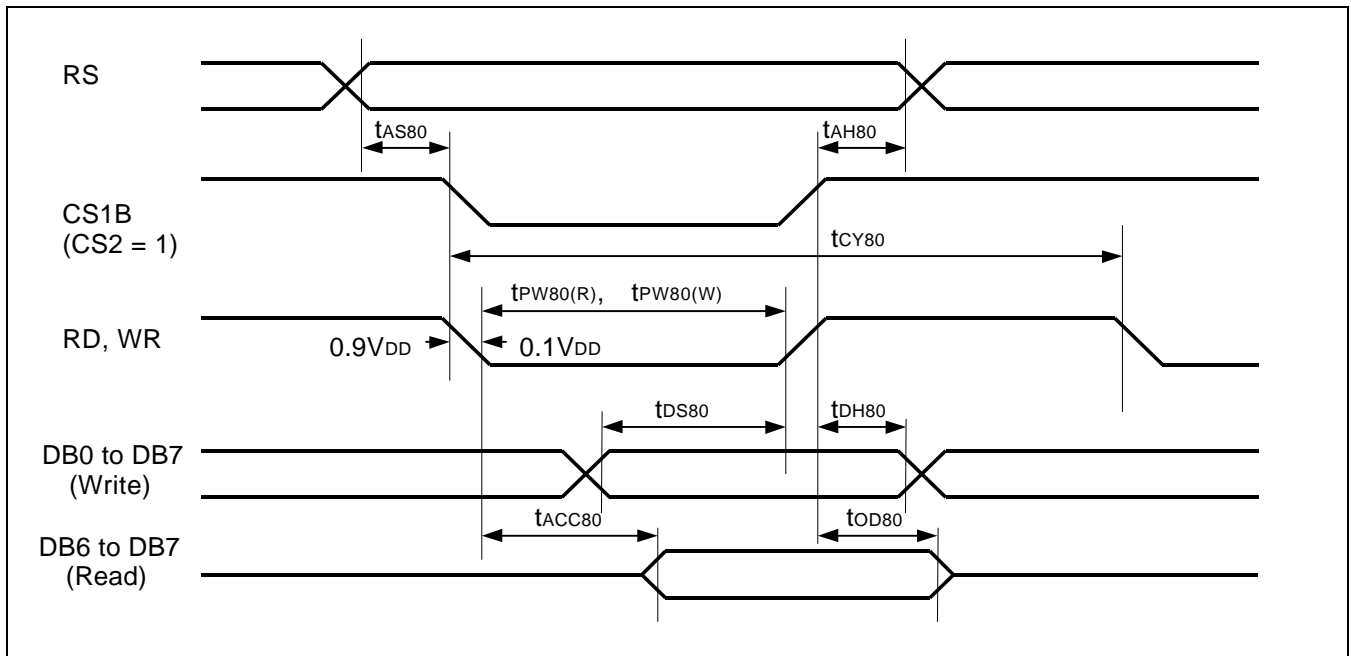


Figure 31. Read / Write Characteristics (8080-series MPU)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

| Item | Signal | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------------|------------|----------|------|------|------|------|-------------|
| Address setup time | RS | tAS80 | 13 | - | - | ns | |
| Address hold time | RS | tAH80 | 17 | - | - | ns | |
| System cycle time | RS | tCY80 | 400 | - | - | ns | |
| Pulse width (WR) | RW_WR | tPW80(W) | 55 | - | - | ns | |
| Pulse width (RD) | E_RD | tPW80(R) | 125 | - | - | ns | |
| Data setup time | DB7 to DB0 | tDS80 | 35 | - | - | ns | |
| Data hold time | | tDH80 | 13 | - | - | ns | |
| Read access time | DB0 | tACC80 | - | - | 125 | ns | CL = 100 pF |
| Output disable time | | tOD80 | 10 | - | 90 | ns | |

Read / Write Characteristics (6800-series Microprocessor)

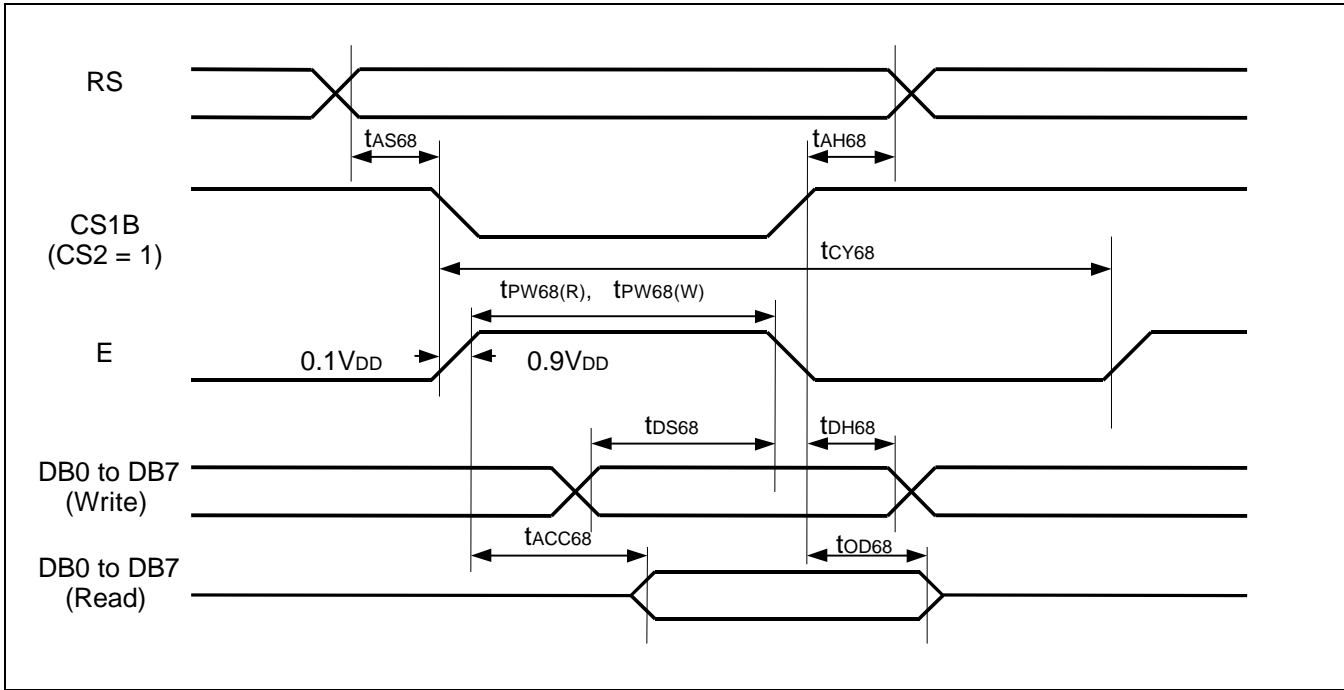


Figure 32. Read / Write Characteristics (6800-series Microprocessor)

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

| Item | Signal | Symbol | Min. | Typ. | Max. | Unit | Remark |
|---------------------|------------|----------|------|------|------|------|-------------|
| Address setup time | RS | tAS68 | 13 | - | - | ns | |
| Address hold time | RS | tAH68 | 17 | - | - | ns | |
| System cycle time | RS | tCY68 | 400 | - | - | ns | |
| Data setup time | DB7 to DB0 | tDS68 | 35 | - | - | ns | |
| Data hold time | | tDH68 | 13 | - | - | ns | |
| Access time | DB7 to DB0 | tACC68 | - | - | 125 | ns | CL = 100 pF |
| Output disable time | | tOD68 | 10 | - | 90 | | |
| Enable pulse width | Read | tPW68(R) | 125 | - | - | - | |
| | Write | tPW68(W) | 55 | - | - | - | |

Serial Interface Characteristics

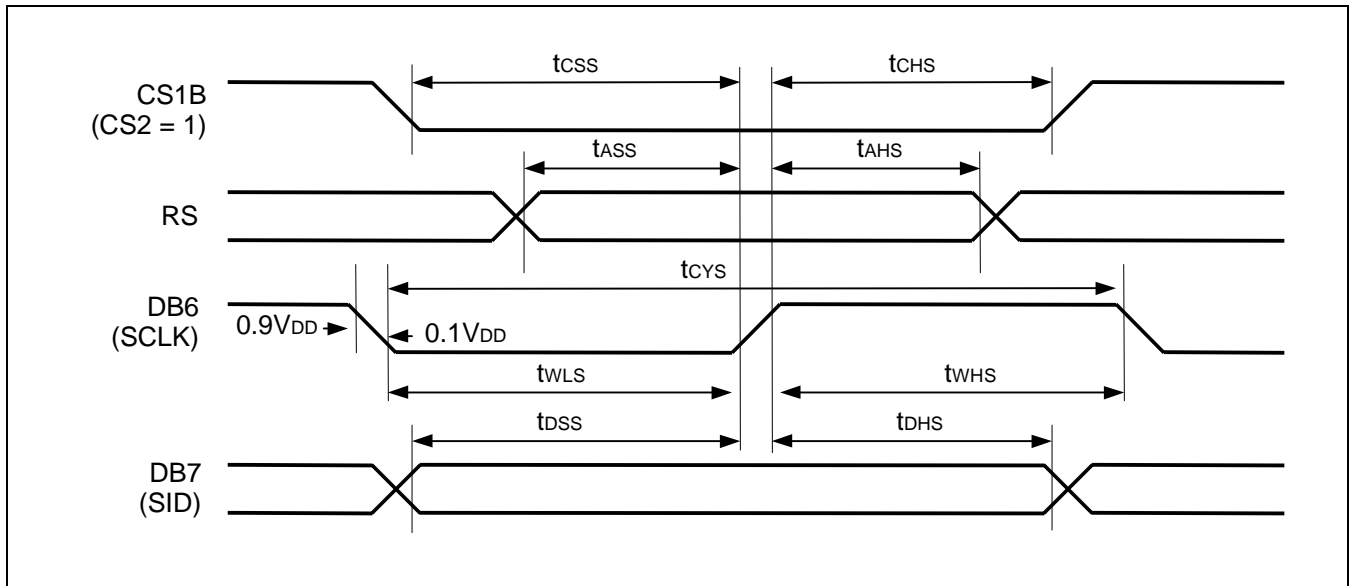


Figure 33. Serial Interface Characteristics

(VDD = 2.4 to 3.6V, Ta = -40 to +85°C)

| Item | Signal | Symbol | Min | Typ | Max | Unit | Remark |
|-----------------------|---------------|--------|-----|-----|-----|------|--------|
| Serial clock cycle | DB6 (SCLK) | tcYS | 450 | - | - | ns | |
| SCLK high pulse width | | twHS | 180 | - | - | | |
| SCLK low pulse width | | twLS | 135 | - | - | | |
| Address setup time | RS | tASS | 90 | - | - | ns | |
| Address hold time | | tAHS | 360 | - | - | | |
| Data setup time | DB7 (SID) | tdSS | 90 | - | - | ns | |
| Data hold time | | tdHS | 90 | - | - | | |
| CS1B setup time | CS1B | tcSS | 55 | - | - | ns | |
| CS1B hold time | | tCHS | 180 | - | - | | |

Reset Input Timing

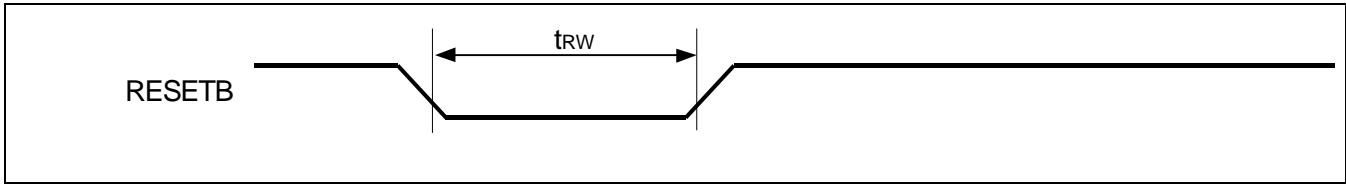


Figure 34. Reset Input Timing

(V_{DD} = 2.4 to 3.6V, T_a = -40 to +85°C)

| Item | Signal | Symbol | Min. | Typ. | Max. | Unit | Remark |
|-----------------------|--------|--------|------|------|------|------|--------|
| Reset low pulse width | RESETB | trw | 900 | - | - | ns | |

Display Control Output Timing

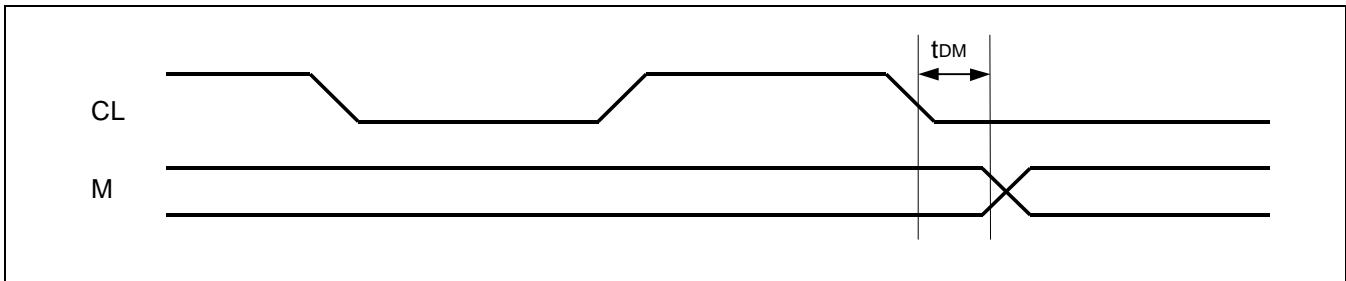


Figure 35. Display Control Output Timing

(V_{DD} = 2.4 to 3.6V, T_a = -40 to +85°C)

| Item | Signal | Symbol | Min. | Typ. | Max. | Unit | Remark |
|--------------|--------|--------|------|------|------|------|--------|
| M delay time | M | tDM | - | 13 | 70 | ns | |

REFERENCE APPLICATIONS

MICROPROCESSOR INTERFACE

In Case of Interfacing with 6800-series (PS = "H", MI = "H")

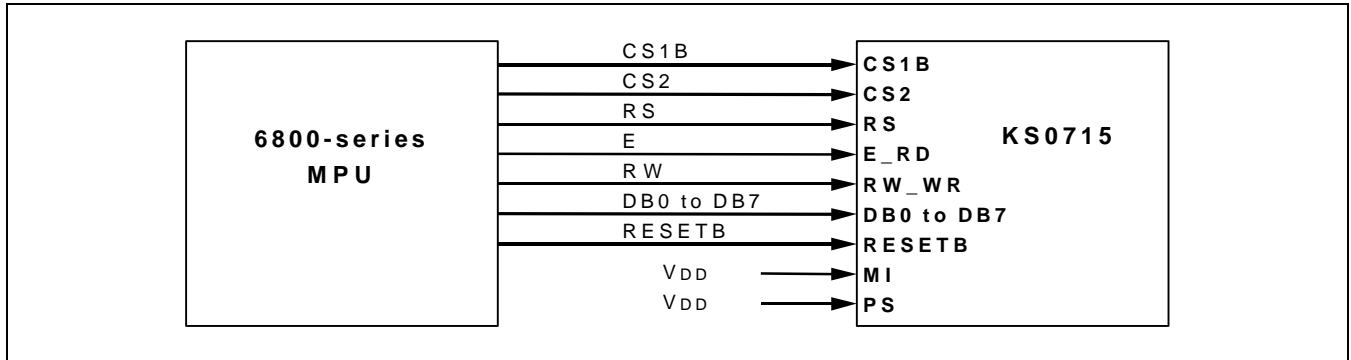


Figure 36. Interfacing with 6800-series (PS = "H", MI = "H")

In Case of Interfacing with 8080-series (PS = "H", MI = "L")

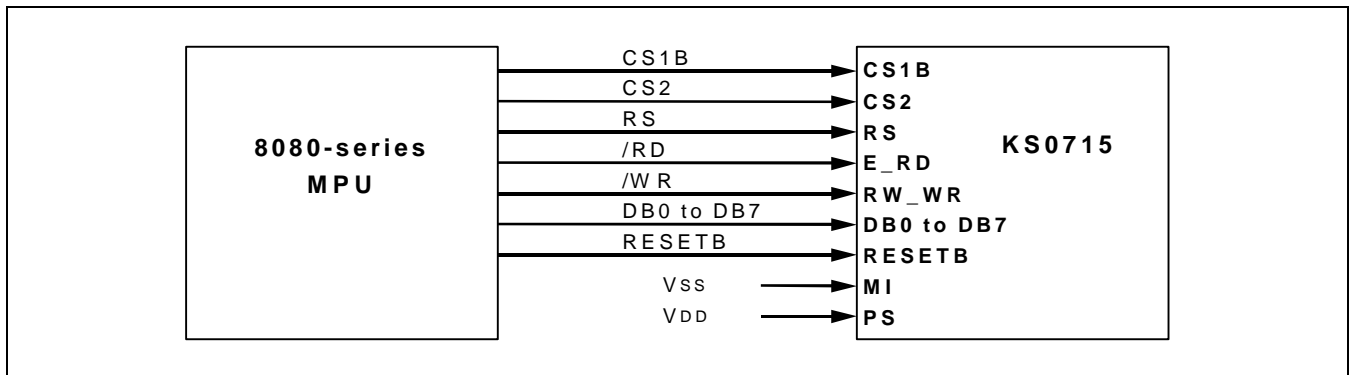


Figure 37. Interfacing with 8080-series (PS = "H", MI = "L")

In Case of Serial Interface (PS = "L", MI = "H/L")

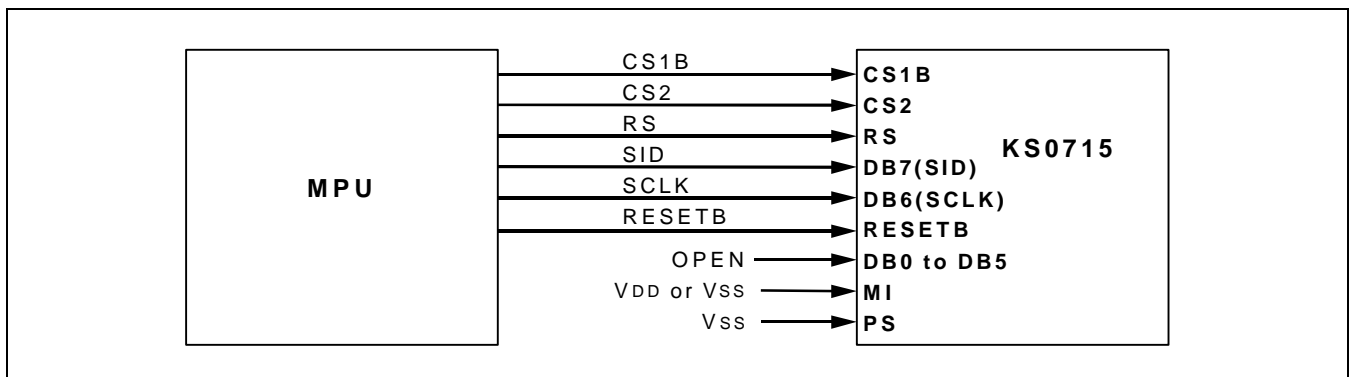


Figure 38. Serial interface (PS = "L", MI = "H/L")

CONNECTIONS BETWEEN KS0715 AND LCD PANEL

Single Chip Configuration (1/33 Duty Configurations)

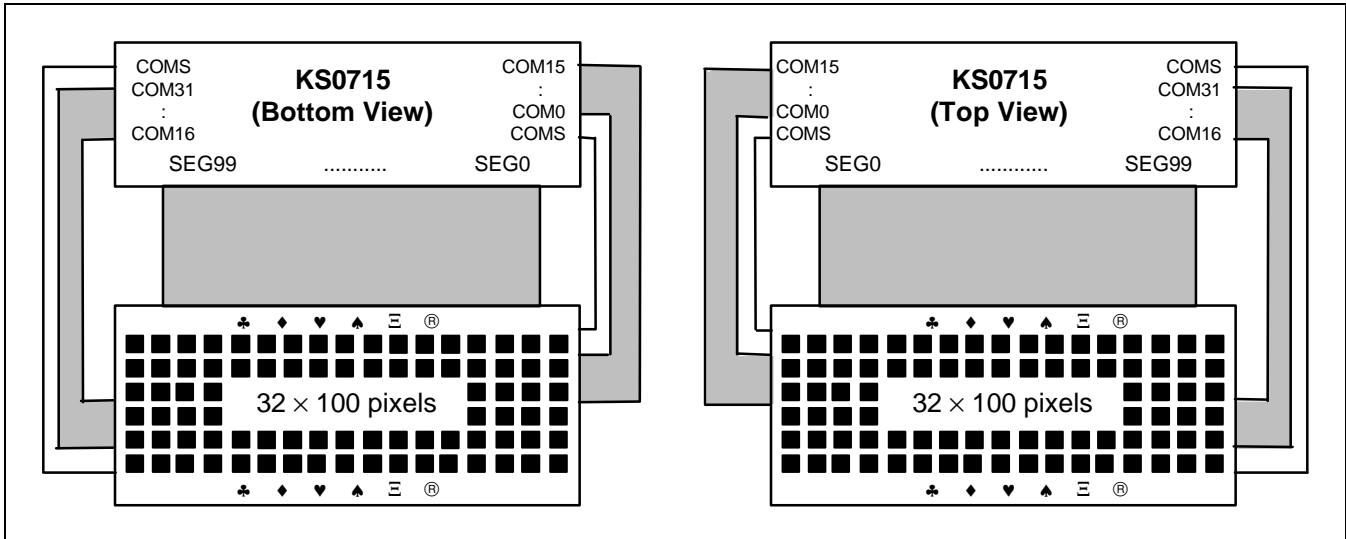


Figure 39. SHL = 0, ADC = 1

Figure 40. SHL = 0, ADC = 0

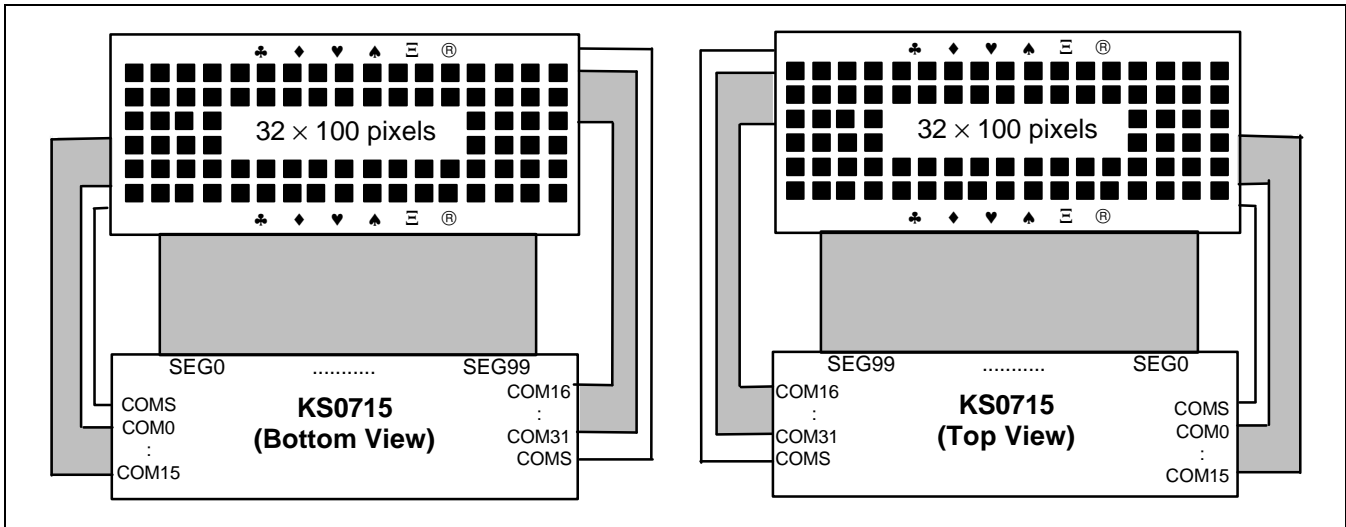


Figure 41. SHL = 1, ADC = 0

Figure 42. SHL = 1, ADC = 1

Multiple Chip Configuration

- 33COM (32COM + 1COMS) × 200SEG (100SEG × 2)

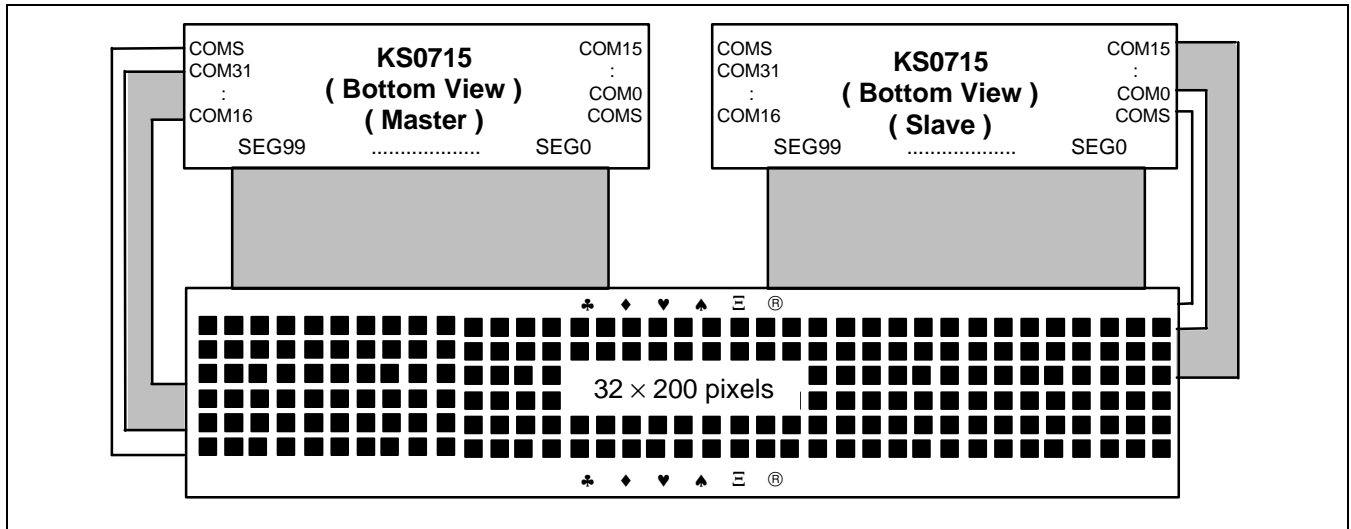


Figure 43. SHL = 0, ADC = 1

- ◆ Connect the following pins of two chips each other
 - Display clock pins: CL, M
 - Display control pin: DISP
 - LCD power pins: V0, V1, V2, V3, V4

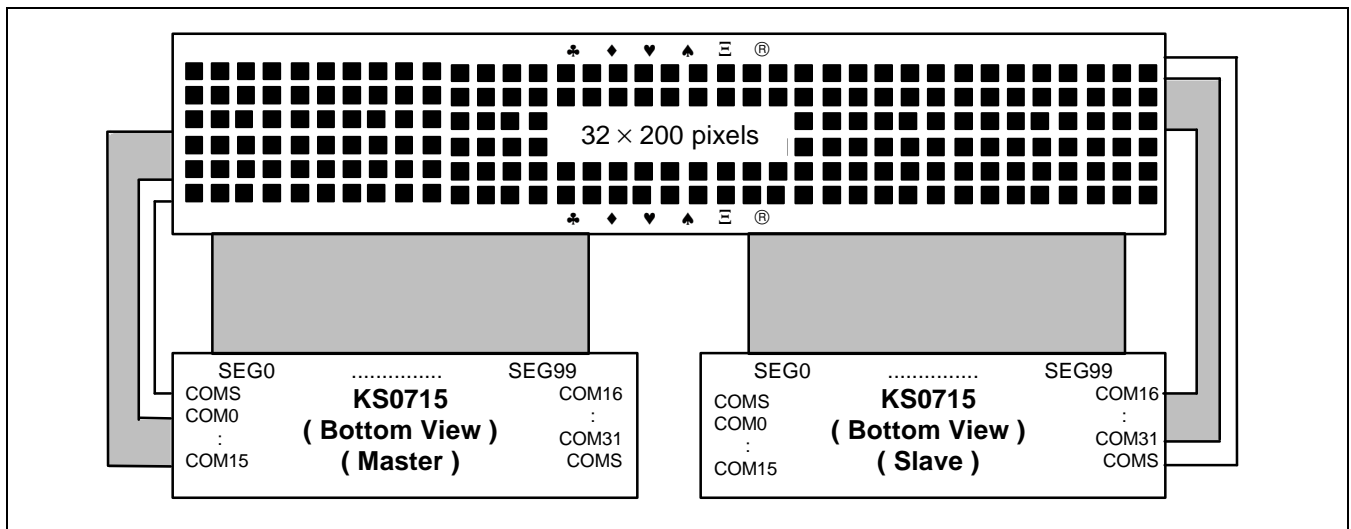


Figure 44. SHL = 1, ADC = 0

- ◆ Connect the following pins of two chips each other
 - Display clock pins: CL, M
 - Display control pin: DISP
 - LCD power pins: V0, V1, V2, V3, V4

- 66COM (64COM + 2COMS) × 100SEG

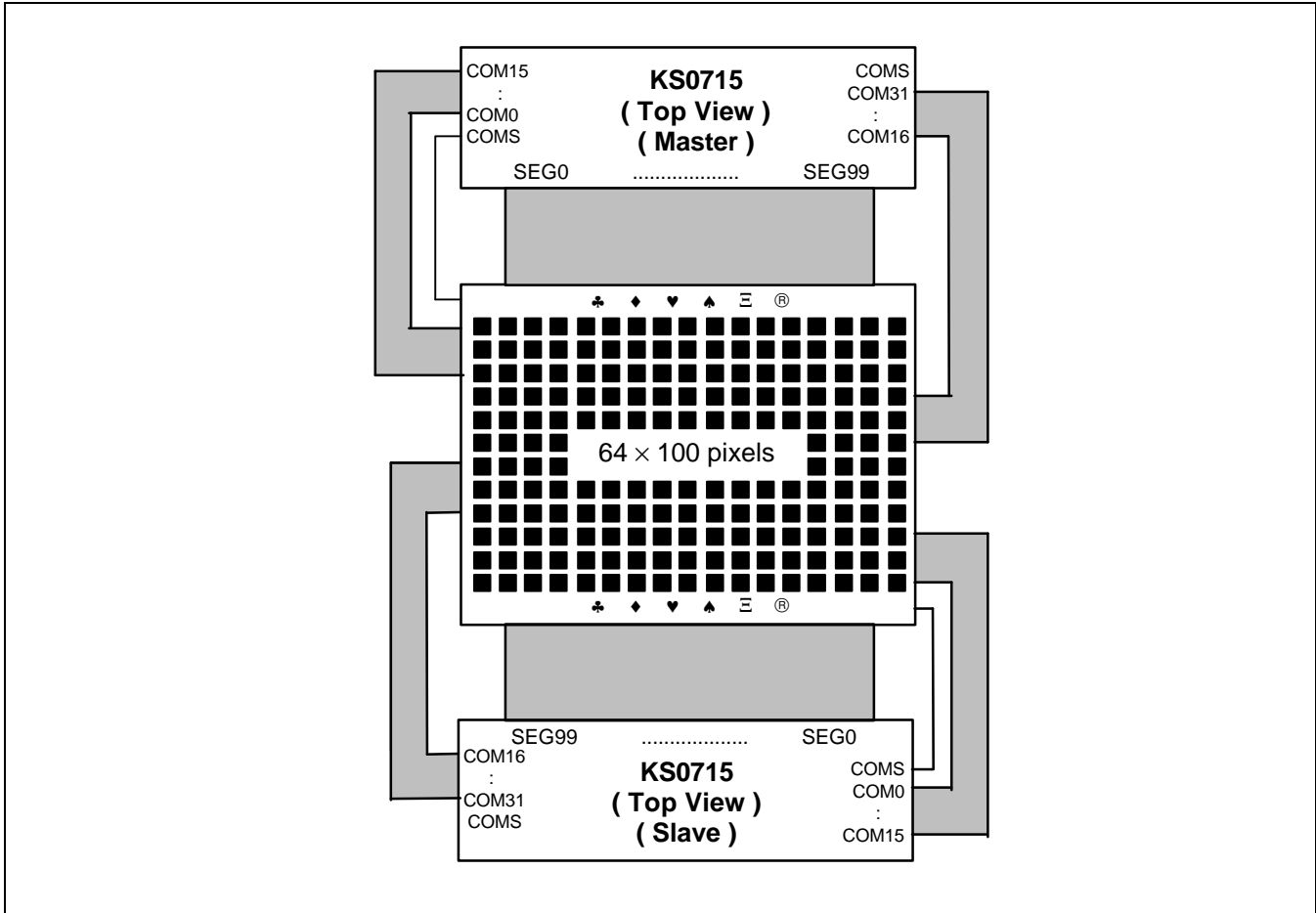


Figure 45. 66COM (64COM + 2COMS) × 100SEG

- ◆ Connect the following pins of two chips each other
 - Display clock pins: CL, M
 - Display control pin: DISP
 - LCD power pins: V0, V1, V2, V3, V4
- ◆ Common / Segment output direction select
 - Master chip: SHL = 0, ADC = 0
 - Slave chip: SHL = 1, ADC = 1

TCP PIN LAYOUT (SAMPLE)

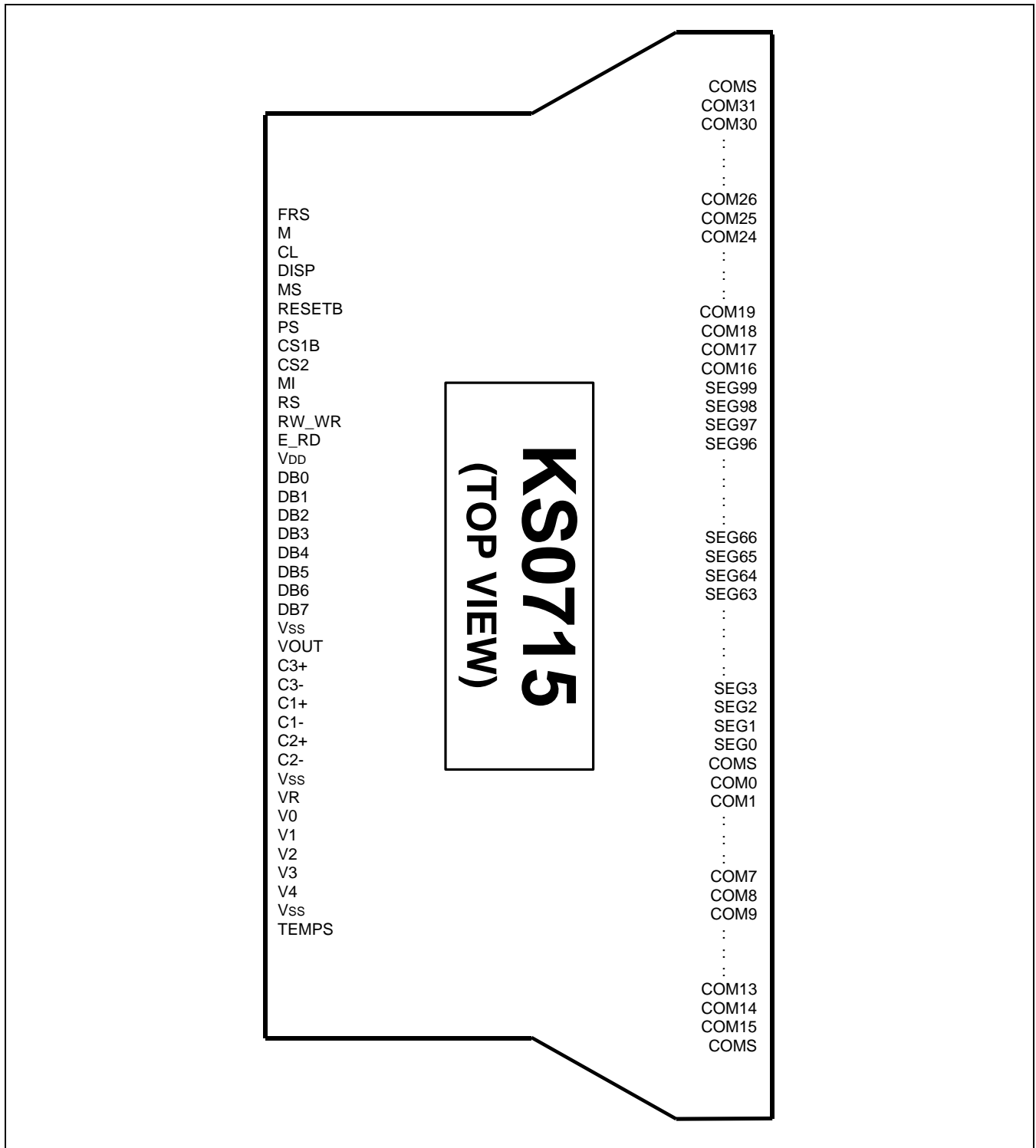


Figure 46. TCP Pin Layout