KS16112/4 9600/14400 bps FAX MODEM

INTRODUCTION

The KS16112 and KS16114 are synchronous, half - duplex modems capable of speeds up to 9600 bps (KS16112) or up to 14400 bps (KS16114).

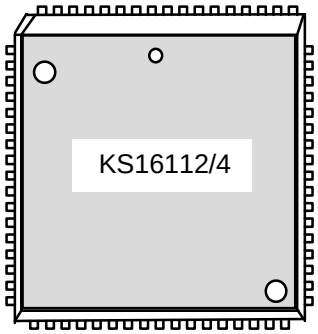
These modem devices can operate over the public switched telephone network (PSTN) with the addition of the appropriate data access arrangement (DAA).

These modems satisfy the requirements specified in ITU-T re - commendations V.17 (KS16114), V.29, V.27 ter, V.21 Channel 2 and T.4, and meet the binary signaling requirements of T.30.

These products are intended to be used in Group 3 facsimile machines or fax processing boards and can operate at 14400 (KS16114), 12000 (KS16114), 9600, 7200, 4800, 2400 or 300 bps depending on the selected configuration.

These devices also feature V.17 short train (KS16114) and V.27 ter short train and three programmable tone detectors as well as a pro - grammable DTMF receiver. Additionally, HDLC framing (according to T.30) at 14400 (KS16114), 12000 (KS16114), 9600, 7200, 4800, 2400 or 300 bps is also featured.

68 - PLCC - SQ



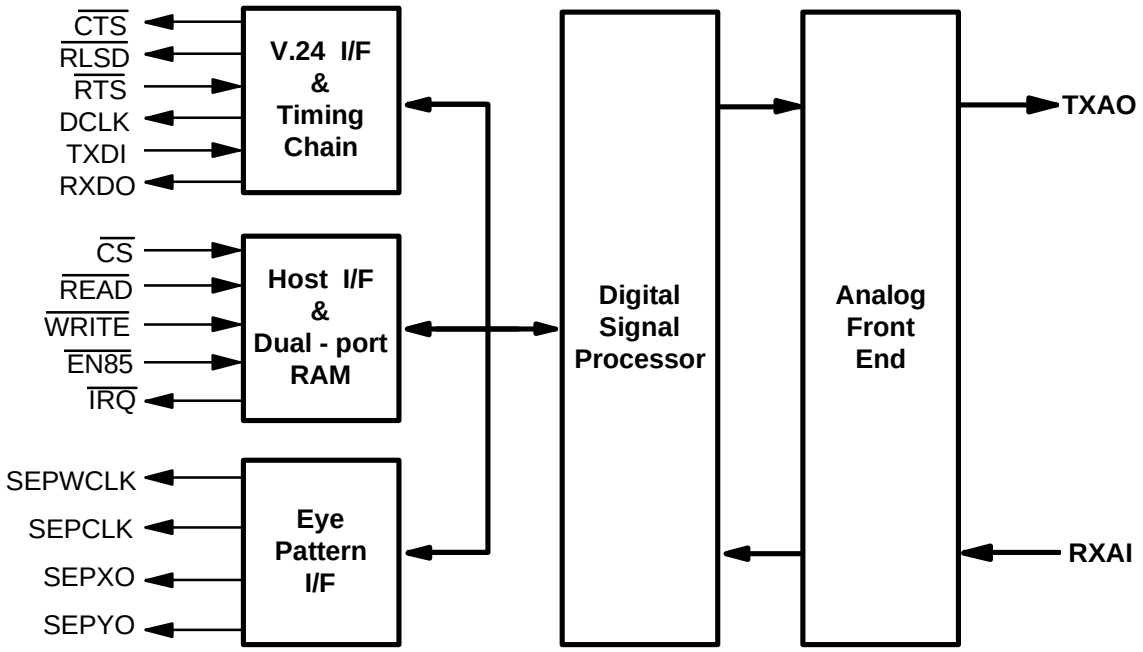
ORDERING INFORMATION

Device	Package	Operating Temperature
KS16112	68-PLCC-SQ	0 ~ +70 ° C
KS16114	68-PLCC-SQ	

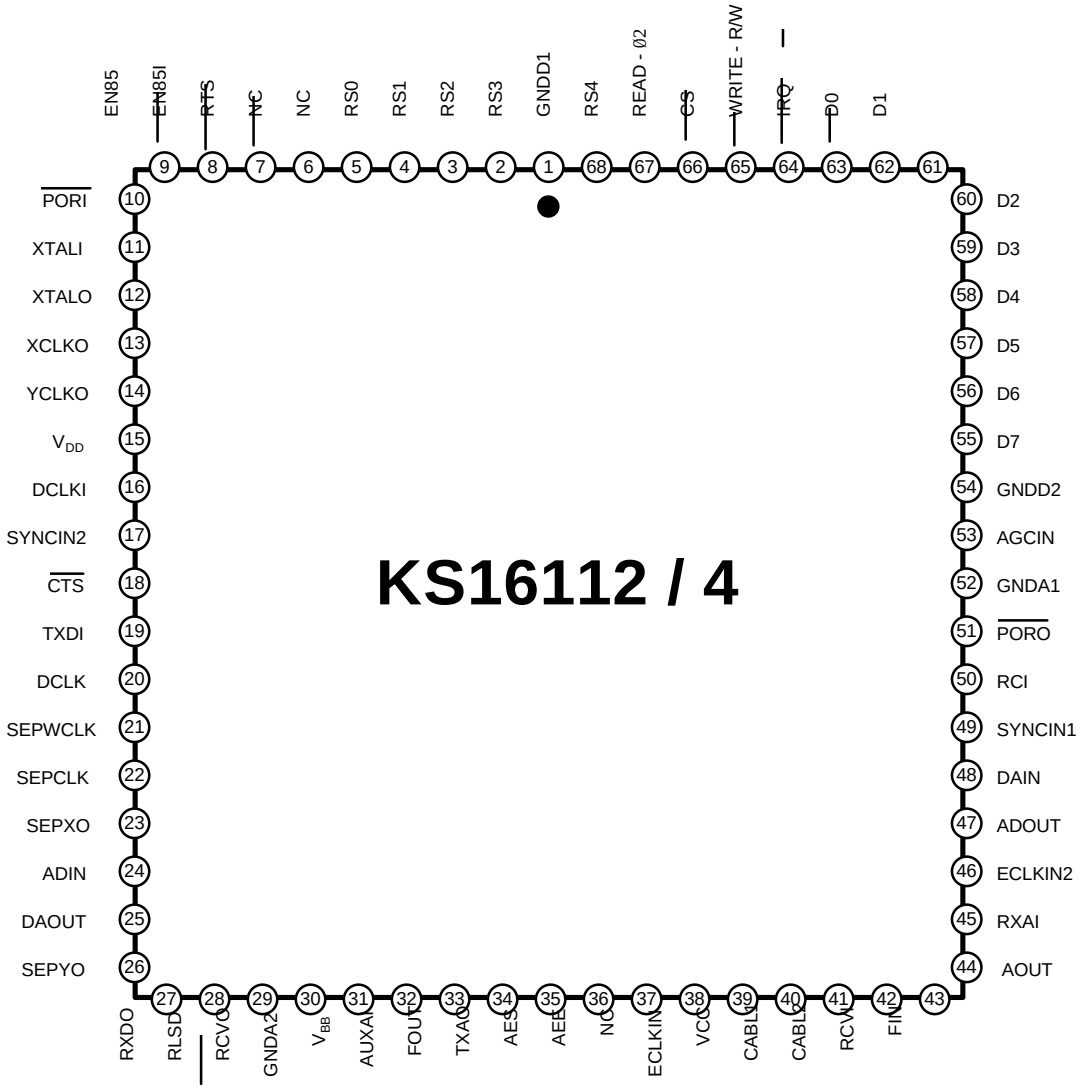
FEATURES

- Group 3 facsimile transmission / reception according to :
  - ITU-T V.17 short and long train (KS16114)
  - ITU-T V.29, V.27 ter short and long train, V.21 Ch.2, T.30 and T.4
- Half - duplex operation
- Receiver dynamic range : 0 dBm to - 43 dBm
- Programmable transmit level : 0 dBm to - 15 dBm
- Programmable dual tone generation
- Programmable tone detection
- Programmable interface memory interrupt
- Programmable turn on and turn off thresholds
- Automatic T/ 2 adaptive equalizer
- HDLC capability at all speeds
- Diagnostic capability allowing telephone line quality monitoring
- ITU-T V.24 compatible interface
- TTL and CMOS compatible
- Low power consumption, KS16112 : 400mW typical, KS16114 : 550mW typical
- Programmable compromise filter for high speed RX modes

BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	Type	Description
67 1 2 3 4	RS4 RS3 RS2 RS1 RS0	I	• **Register select bus** These lines are used to address interface memory registers within the modem. When $\overline{CS}$ is active, the modem decodes RS0 through RS4 to address one of its 32 internal interface memory registers. RS4 is the most significant bit. In a typical design, RS0 - RS4 are connected to A0 - A4 address lines of the host microprocessor.
55 56 57 58 59 60 61 62	D7 D6 D5 D4 D3 D2 D1 D0	I/O	• **Data bus** These bi-directional data bus lines provide parallel data transfer between the modem and the host microprocessor. D7 is the most significant bit. The direction of the D0 - D7 data bus is controlled by the $\overline{READ}$ - Ø 2and $\overline{WRITE}$ - R/$\overline{W}$ signals. When not being written into or read from, D0 - D7 assume the high impedance state.
65	$\overline{CS}$	I	• **Chip select** The modem is selected and decodes RS0 - RS4 when $\overline{CS}$ becomes active at which time data transfer between the modem and the host can take place over the parallel data bus. Typically, $\overline{CS}$ is driven by address decode logic.
66	$\overline{READ}$ - Ø 2	I	• **Read enable (bus mode) or phase2 (6500 bus mode)** If 8085 bus mode is selected ($\overline{EN85}$ is connected to ground), this signal acts as the $\overline{READ}$ input. If 6500 bus mode is selected ($\overline{EN85}$ is pulled - up to +5V), this signal acts as the Phase 2 clock input.
64	$\overline{WRITE}$ -R/$\overline{W}$	I	• **Write enable (bus mode) or R/$\overline{W}$ (6500 bus mode)** If 8085 bus mode is selected ($\overline{EN85}$ is connected to ground), this signal acts as the $\overline{WRITE}$ input. If 6500 bus mode is selected ($\overline{EN85}$ is pulled - up to +5V), this signal acts as the R/$\overline{W}$ strobe.

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Type	Description
63	$\overline{IRQ}$	O	• **Interrupt request** The modem can use $\overline{IRQ}$ to interrupt the host microprocessor program execution. $\overline{IRQ}$ can be enabled in the modem interface memory to be asserted in response to a specified change of conditions in the modem status. $\overline{IRQ}$ is an open drain output and must be connected to an external pull up resistor of suitable value (typically, a 5.6 KΩ, 1/4 watt, 5% resistor is adequate).
19	TXDI	I	• **Transmit data input** TXDI is the modem' stransmit data serial input. When configured for serial data mode (PDME bit is reset) the modem accepts data bits for transmission via this input. When transmitting data, the modem reads the TXDI pin on the rising edge of DCLK. When the modem is con - figured for parallel data mode (PDME bit is set), the TXDI pin is ig - nored and transmit data is accepted by the modem via the DBFR register.
27	RXDO	O	• **Receive data output** RXDO is the modem receive data output. Received data is output to the DTE via the RXDO pin in both serial and parallel data modes (PDME bit set or reset). When receiving data, the modem outputs a data bit on the falling edge of DCLK. The center of RXDO bits coincides with the rising edge of DCLK, thus, the DTE should read RXDO on the rising edge of DCLK.
7	$\overline{RTS}$	I	• **Request to send** When the $\overline{RTS}$ input is forced low, the transmitter starts transmitting the modem training sequence according to the selected configuration. Once the training sequence has been transmitted (signaled by the $\overline{CTS}$ pin and CTSB bit becoming active), data present at either the TXDI input pin in serial mode (PDME bit is reset) or written into the DBFR register in parallel mode (PDME bit is set) is modulated and transmitted. The $\overline{RTS}$ input pin is logically ORed with the RTSB bit in the interface memory.

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Type	Description
18	$\overline{CTS}$	O	• **Clear to send** $\overline{CTS}$ is used to indicate of that the training sequence transmission has been completed and the modem is ready to transmit any data present at either the TXDI input pin in serial mode (PDME bit is reset) or in DBFR in parallel mode (PDME bit is set).
28	$\overline{RLSD}$	O	• **Received line signal detector** $\overline{RLSD}$ becomes active at the end of the reception of the training sequence indicating the beginning of data reception. If no training is detected but the received energy level is above the $\overline{RLSD}$ off - to - on threshold, $\overline{RLSD}$ will become active.
20	DCLK	O	• **Data clock** DCLK acts as received data clock or transmit data clock depending on the state of the modem (transmit or receive mode). The frequency of the clock corresponds to the data rate of the selected modem configuration and is accurate to ± 0.01%. In receive mode the RXDO pin is clocked out by the modem on the rising edge of DCLK. In transmit mode, TXDI is clocked in by the modem on the falling edge of DCLK.
11 12	XTALI XTALO	I O	• **Oscillator In / Out** An external 24.00014 MHz (KS16112) or 38.00053 MHz (KS16114) crystal and two capacitors are connected to the XTALI and XTALO. Alternatively, an external crystal oscillator of the appropriate frequency can be connected to the XTALI input leaving XTALO unconnected. In order to minimize electromagnetic emissions and ensure proper oscillator start up and operation, the crystal and the capacitors should be placed as close as possible to the XTALI and XTALO pins. Further, the circuit board traces connecting the crystal and capacitors to XTALI and XTALO should be as short as possible. The use of circuit board vias should be avoided in the crystal oscillator circuitry and circuit board traces should be routed using curved turns.

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Type	Description
10 51	$\overline{PORI}$ $\overline{PORO}$	I O	• **Power On reset In/Out** $\overline{PORI}$ and $\overline{PORO}$ must be connected together forming a bi-directional modem reset signal ($\overline{POR}$). When power is first applied to the modem, $\overline{POR}$ is held low for approximately 350 ms. The modem is then ready for normal operation 15 ms after the low to high transition of $\overline{POR}$.
15	V_{DD}	Power	• **+ 5V Digital voltage supply** This pin must be connected to +5V ± 5% supply. The + 5V Digital power supply voltage ripple should not exceed $100mV_{P-P.}$
39	V_{CC}	Power	• **+ 5V Analog voltage supply** This pin must be connected to +5V ± 5% supply. The + 5V Analog power supply voltage ripple should not exceed $100mV_{P-P.}$
31	V_{BB}	Power	• **- 5V Analog voltage supply** This pin must be connected to -5V ± 5% supply. The - 5V Analog power supply voltage ripple should not exceed $100mV_{P-P.}$
68 54	GNDD1 GNDD2	GND	• **Digital ground** These pin must be connected to digital ground.
52 30	GNDA1 GNDA2	GND	• **Analog ground** These pin must be connected to analog ground.
9	$\overline{EN85}$	I	• **Enable 8085 bus mode** When $\overline{EN85}$ is connected to ground, 8085 bus mode is selected and the modem can interface directly to an 8085 compatible microprocessor bus using $\overline{READ}$ and $\overline{WRITE}$. When $\overline{EN85}$ is pulled - up to + 5V, 6500 bus mode is selected and the modem can interface directly to a 6500 compatible micro - processor using Ø 2and R/$\overline{W}$.

PIN DESCRIPTION (Continued)

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Type</th><th>Description</th></tr>
<tr><td>40
41</td><td>CABL1
CABL2</td><td>I</td><td>• Cable 1 and Cable 2 equalizer select
These two inputs are used to select equalization for the following cable lengths :
<table>
<tr><th colspan="2">CABLE TYPE</th><th>LENGTH</th><th colspan="4">Gain (dB)</th></tr>
<tr><td>CABL2</td><td>CABL1</td><td>LENGTH</td><td>700Hz</td><td>1500Hz</td><td>2000Hz</td><td>3000Hz</td></tr>
<tr><td>low</td><td>low</td><td>0.0Km</td><td>0.00</td><td>0.00</td><td>0.00</td><td>0.00</td></tr>
<tr><td>low</td><td>high</td><td>1.8Km</td><td>-0.99</td><td>-0.20</td><td>0.15</td><td>1.43</td></tr>
<tr><td>high</td><td>low</td><td>3.6Km</td><td>-2.39</td><td>-0.65</td><td>0.87</td><td>3.06</td></tr>
<tr><td>high</td><td>high</td><td>7.2Km</td><td>-3.93</td><td>-1.22</td><td>1.90</td><td>4.58</td></tr>
</table></td></tr>
<tr><td>13</td><td>XCLKO</td><td>O</td><td>• XCLK output
This output pin is a 12MHz (KS16112) or 19MHz (KS16114) square wave output derived from XTALI.</td></tr>
<tr><td>14</td><td>YCLKO</td><td>O</td><td>• YCLK output
This output pin is a 6MHz (KS16112) or 9.5MHz (KS16114) square ware output derived from XTALI.</td></tr>
<tr><td>23
26</td><td>SEPXO
SEPYO</td><td>O
O</td><td>• Serial eye pattern bit data
These two outputs provide two serial bit streams containing eye pattern display data for the oscilloscope X and Y axis.
The data words are 9 bits long with the sign bit shifted out first and the bits clocked by the rising edge of SEPCLK.</td></tr>
<tr><td>22</td><td>SEPCLK</td><td>O</td><td>• Serial eye pattern bit clock
SEPCLK is a 230.4KHz clock used to shift the eye pattern data into the serial-to-parallel converters.
SEPXO and SEPYO are shifted out by the modem on the rising edge of SEPCLK.</td></tr>
<tr><td>21</td><td>SEPWCLK</td><td>O</td><td>• Serial eye pattern word clock
SEPWCLK (9600Hz) provides SEPXO and SEPYO 9 - bit word timing and its rising edge is used for copying the output of the serial to parallel converters into the X and Y digital-to-analog converters.</td></tr>
</table>

PIN DESCRIPTION (Continued)

Pin No.	Symbol	Type	Description
34	TXAO	O	• **Transmitter analog output** The TXAO can supply a maximum of 3.03 V_{PK} into a load resistance of 10KΩ (minimum). An external analog smoothing filter with transfer function 28735.63 / (S + 11547.34) is required.
45	RXAI	I	• **Receiver analog input** The input impedance of RXAI is greater them 1MΩ. An external analog anti - aliasing filter with transfer function 21551.72 / (S + 11547.43) is required between the line interface and the modem RXAI input. The maximum input signal level into the anti-aliasing filter should not exceed 0 dBm.
32	AUXAI	I	• **Auxiliary analog input** The transmitter output (TXAO) can be accessed by user equipment through AUXAI. Since this is a sampled input any signals with frequency components higher than 4800Hz (half of the sampling rate) will cause aliasing errors. The input impedance of AUXAI is 1MΩ and the gain to TXAO is 0 dB ± 1dB.

ABSOLUTE MAXIMUM RATINGS (Ta = 25 ° C)

Characteristic	Symbol	Value	Unit
Positive Digital Supply Voltage	V_{DD}	5V ± 5%	V
Positive Analog Supply Voltage	V_{CC}	5V ± 5%	V
Negative Analog Supply Voltage	V_{BB}	-5V ± 5%	V
Power Dissipation	P_D	400 (KS16112) 550 (KS16114)	mW
Operating Temperature	T_{OPR}	0 ~ 70	° C
Storage Temperature	T_{STG}	-55 ~ 150	° C

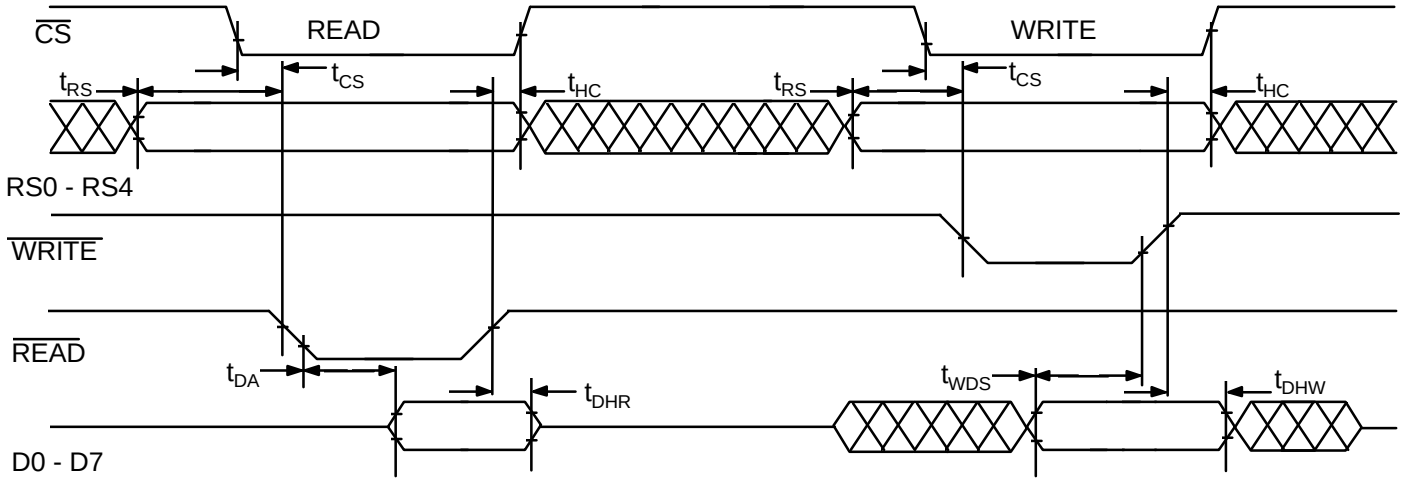
ELECTRICAL CHARACTERISTICS

(Ta = 25 ° Ç V_{CC} = 5V, V_{BB} = -5V, Unless otherwise specified)

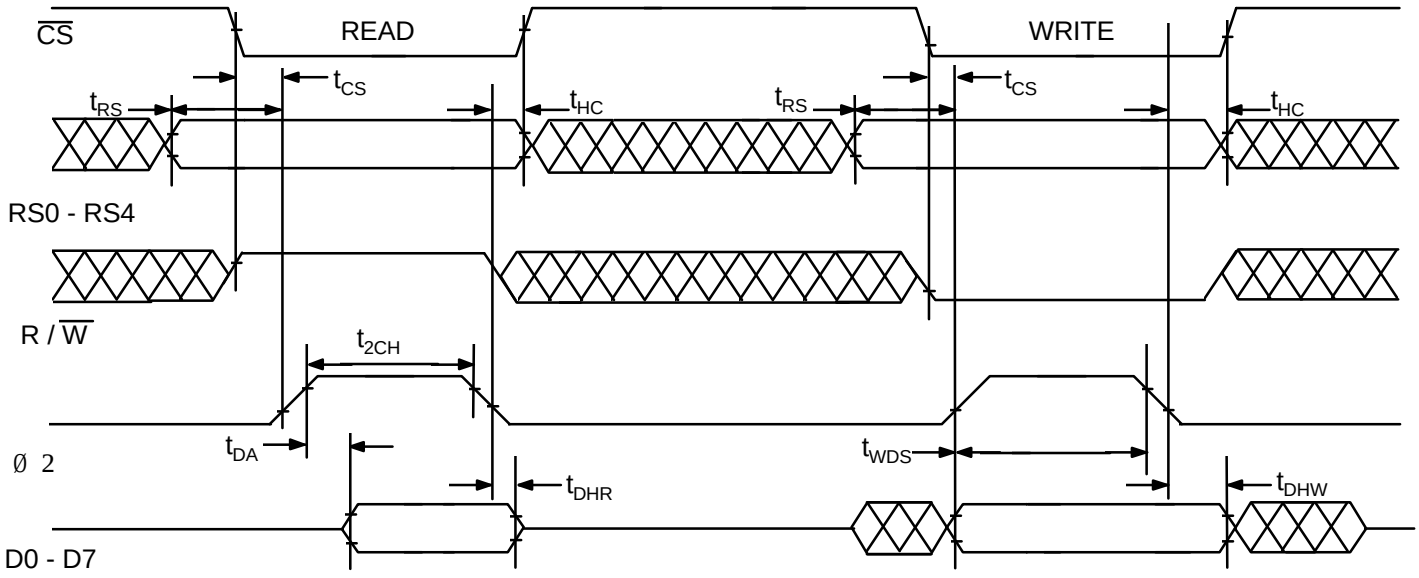
Characteristic		Symbol	Test Condition	Min	Typ	Max	Unit
Input Voltage	$\frac{\text{TTL}}{\overline{\text{PORI}}}$	V_{IH}		2.0 $0.8V_{CC}$		V_{CC} V_{CC}	V
		V_{IL}		-0.3		0.8	V
Input Current	TTL	I_{IH}	V_{CC} = 5.25V, Vin = 5.25V			40	µ A
	TTL w / p - up	I_{IL}	V_{CC} = 5.25V			-400	µ A
Input Leakage		$I_{I(LKG)}$	V_{CC} = 5.25V				µ A
Current	TTL and $\overline{\text{PORI}}$		Vin = 0 to 5V			± 2.5	
Output Leakage		$I_{O(LKG)}$	Vin = 0.4 to V_{CC} - 1				µ A
Current	TTL 3 - S					± 10	
Output Voltage							
V.24 Signals,	TTL 3 - S	V_{OH}	I_{LOAD} = -100 µ A	3.5			V
	$\overline{\text{PORO}}$		I_{LOAD} = -40 µ A	2.4			
V.24 Signals,	$\overline{\text{IRQ}}$		I_{LOAD} = 1.6mA			0.4	
	D0 - D7	V_{OL}	I_{LOAD} = 0.8mA			0.4	V
	$\overline{\text{PORO}}$		I_{LOAD} = 0.4mA			0.4	
Clock Output		$I_{OH(CLK)}$				-0.1	mA
Current		$I_{OL(CLK)}$				100	µ A
Capacitive Load	TTL and $\overline{\text{PORI}}$	C_L			5		PF
	TTL w / p - up				20		
Capacitive Drive	TTL 3-S and Open	C_D			100		PF
	Drain CLOCK				50		

MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS (Ta = 25 ° C)

Characteristics	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ Set up time	t_{CS}	0			nSec
RSI Set up time	t_{RS}	25			nSec
Data access time	t_{DA}			75	nSec
Data hold time	t_{DHR}	10			nSec
Control hold time	t_{HC}	10			nSec
Write data set up time	t_{WDS}	20			nSec
Write data hold time	t_{DHW}	10			nSec
Phase 2 Clock high	t_{2CH}	100			nSec



a. 8085 Bus Compatible ($\overline{EN85}$ = " L)



b. 6500 Bus Compatible ($\overline{EN85}$ = " H)

Figure 1. MICROPROCESSOR BUS INTERFACE TIMING DIAGRAM

TECHNICAL SPECIFICATIONS

1 Configurations, Signaling Rates and Data Rates

The various modem configurations with the corresponding modulation specifications are shown in Table 7.

Table 7. Modulation Specifications

Configuration	Modulation Scheme	Carrier Frequency (Hz)	Data Rate (bps)	Data Rate (Symbols/Sec.)	No of Bits per Symbol	No. of Signal Points
V.17 14400 (KS16114)	TCM	1800	14400	2400	6	128
V.17 12000 (KS16114)	TCM	1800	12000	2400	5	64
V.17 9600 (KS16114)	TCM	1800	9600	2400	4	32
V.17 7200 (KS 16114)	TCM	1800	7200	2400	3	16
V.29 9600	QAM	1700	9600	2400	4	16
V.29 7200	QAM	1700	7200	2400	3	8
V.29 4800	QAM	1700	4800	2400	2	4
V.27 ter 4800	DPSK	1800	4800	1600	3	8
V.27 ter 2400	DPSK	1800	2400	1200	2	4
V.21 Ch2 300	FSK	1650, 1850	300	300	1	

2 Transmitted Data Spectrum

The transmitted data spectrum is shaped with the following characteristics:
At 2400 baud a square root of 25% raised cosine filter is used.
At 1600 baud a square root of 50% raised cosine filter is used.
At 1200 baud a square root of 90% raised cosine filter is used.

3 Turn - On Sequence

The transmitter turn - on sequence times are shown in Table 8.

Table 8. Turn - On Sequence Duration

Configuration	EPTE OFF	EPTE ON
V.17 long train (all speeds) (KS16114)	1393 ms	1600 ms
V.17 short train (all speeds) (KS16114)	142 ms	350 ms
V.29 (all speeds)	253 ms	441 ms
V.27 ter 4800 bps long train	708 ms	915 ms
V.27 ter 4800 bps short train	50 ms	257 ms
V.27 ter 2400 bps long train	943 ms	1150 ms
V.27 ter 2400 bps short train	67 ms	274 ms
V.21 Ch2 300 bps	< 400 us	< 400 us

4 Turn - Off Sequence

The turn - off sequence consists of:

- for V.17 (KS16114) approximately 14 ms of remaining data and scrambled ones followed by 20 ms of silence.
- for V.29 approximately 5 ms of remaining data and scrambled ones followed by 20 ms of silence
- for V.27 ter approximately 10 ms of remaining data and scrambles ones (1200 baud) and 7 ms of data and scrambled ones (1600 baud) and 20 ms of silence.
- for V.21 ch 2 the transmitter turns-off within 7 ms after RTS goes inactive.

5 Data Encoding

The data encoding is in accordance with ITU-T recommendations V.17 (KS16114), V.29, V.27 ter, V.21 Channel 2, and T.3.

6 Equalization

Required line equalization is implemented in V.17 (KS16114), V.29 and V.27 ter modes with an adaptive 48 - tap T/2 transversal equalizer.

7 Tone Generation

The modem is capable of generating single or dual tones in the frequency range of 400 to 3200 Hz with a resolution of 0.15 Hz and accuracy of 0.01%. This feature allows the modem to function as a DTMF dialer.

8 Transmit Level

The transmitter output level is programmable from 0 dBm to - 15.0 dBm and is accurate to ± 1.0 dB.

9 Scrambler / Descrambler

The scrambler and descrambler are in accordance with ITU-T recommendations V.17 (KS16114), V.29 and V.27ter.

10 Receiver Dynamic Range

The receiver can operate with line signal levels from 0 dBm to - 43 dBm at the receiver analog input (RXAI). The $\overline{\text{RLSD}}$ threshold levels are programmable as follows:

Turn on: - 10 dBm to - 47 dBm (default = - 43 dBm)
Turn off: - 10 dBm to - 52 dBm (default = - 48 dBm)

11 Receiver Timing

The receiver can track a timing error of up to ± 0.035%

12 Carrier Recovery

The receiver can track a frequency offset up to ± 10 Hz.

13 Received Data

The serial received data output (RXDO) is clamped to a constant mark whenever $\overline{\text{RLSD}}$ is off.

14 Tone Detection

The modem features three tone detectors two of which operate in all non - high speed modes. The third tone detector operates in all receive modes. The three tone detectors can be cascaded to form a single 12th order filter. The filter coefficients of each tone detector are programmable by the host.

15 Power Requirements

The power requirements are as follows:

+ 5V ± 5% @ 60 mA (typical : KS16112), @95mA (typical : KS16114)
- 5V ± 5% @ 14 mA (typical)

16 Environmental Requirements

The environmental requirements are as follows:

Temperature operating range from 0 - 70 ° C

17 Differences Between the Samsung KS16112/4 and Rockwell R96DFX/R144EFX

The KS16112/4 are pin - to- pin and software compatible modem devices that can be used to replace the Rockwell R96DFX /R144EFX modem. Functionally, the Samsung and Rockwell modems are nearly identical. However, there are a few differences between the two that the user should be aware of.

- The KS16112/4 feature an improved equalizer with 48 taps thus allowing better performance without a compromise equalizer. The KS16112/4 work over 7 Japanese links as well as over all EIA lines. The equalizer is always T/2 fractionally spaced and there is no provision for a T-spaced equalizer. Also when reading the equalizer taps from the DSP it should be noted that the direction of the time axis is different from Rockwell's (i.e the smallest address corresponds to the oldest data). The tap coefficients between the Samsung KS16112/4 and Rockwell R96DFX / R144EFX are not interchangeable (i.e taps stored from the R96DFX / R144EFX cannot be loaded into the KS16112/4).

- Instantaneous energy detector (IED) does not include state 2.

- During DTMF detection the DEDT bit is the same as the DTDT bit.

- The following DTMF parameters are not available:

  Minimum cycle time
  Minimum dropout time (is always set to 5 ms)
  Frequency deviation, low group
  Frequency deviation, high group
  Maximum energy hit time

- Programmable Interrupt does not include dual port interface memory locations 0 and 10.

- The signal level should be derived from the AGC gain word since the average energy is not implemented.
- The carrier detect turn - on and carrier detect turn - off thresholds function differently from the R96DFX / R144EFX .
  The carrier thresholds should be changed by changing MAXG (MAXG is R96DFX /R144EFX compatible).
- Samsung modem does not support squelch extend.
- The host should complete high speed configuration change prior to 30mS before receiving data.
- The host should not write data into DBFR during $\overline{RTS}$ to $\overline{CTS}$ in HDLC mode
- Maximum speed energy (CR1=1 , ADDR1=1E) works differently from Rockwell. Maximum speech energy sets the ratio between the total energy and the DTMF tone energy before valid DTMF digits are detected.
  The default is 4000 hex which is 3dB.
- 1800pF capacitor must be connected between AGCIN and GNDA1 OR GNDA2.
- Data speed detection of V.33 is not supported (KS16114).
- 1700 HZ carrier for V.17 is not supported (KS16114).
- Samsung modem provides a host programmable receiver compromise filter.
- G2 mode is not supported (KS16114).
- Voice mode is not supported (KS16114).
- IRQ2 is not supported (KS16114).

• DSP memory bits that are not supported

KS16112 does not support Rockwell R96DFX DSP memory

- 07:2 SQEXT
- 07:1 T2

KS16114 does not support R144EFX DSP memory

- 1E:4 B2I2E
- 1E:1 B1I2E
- 1D:7 SHPR
- 1D:6 ASPEED
- 1D:5 PR
- 1D:4 PRDET
- 15:6 AREX2
- 15:4 DR2
- 0E:7 FSKFLS
- 0D:3 G2FGC
- 08:2 FSK7E
- 08:1 G2CTK
- 07:2 SQEXT
- 05:6 AREX1
- 05:5 PIDR
- 05:4 DR1

SOFTWARE INTERFACE

Communication between the modem and the host microprocessor is accomplished by means of a dual port interface memory. The dual port memory consists of 32 8-bit registers that both the host microprocessor and the modem have access to. The host can control modem operation by writing control bits or parameter values to the dual port interface memory. The host can also monitor modem operation by reading status bits or data values (such as the eye quality monitor value or EQM) from the interface memory. The dual port read and write procedures are described in section 3.

1. Dual - Port Memory Map

The memory map for the 32 - byte interface memory registers is shown in Table 1. These registers can be accessed during any host read or write cycle. In order to operate on a single bit or a group of bits, the host microprocessor must first read the desired register, set or reset the desired bits and then write the modified and unmodified bits back into the interface memory register.

2 Modem Interface Memory Bit Definitions

This section describes in detail the function of all bits, fields and registers in the interface memory. All bit, field or register names are listed in alphanumeric order. For each bit, field or register the convention R :B (D) is used to indicate the location of the term and its power up default value. R is the register number (hexadecimal), B is the bit or group of bits within that register and D is the associated power up default value. A default value of ' - ' indicates that the bit state depends on modem operating conditions, thus, these bits do not truly have a power up default value.

ABORT **Abort/Idle** **09 : 3 (-)**

In the transmit mode when ABORT is set the modem will finish sending the current DBFR byte after which it will send continuous ones (if ZCLMP is reset) or continuous zeros (if ZCLMP is set). When ABORT is reset the modem will not send continuous ones or zeros.

In the receive mode when ABORT is set the modem has received a minimum of seven consecutive ones. ABORT must then be reset by the host.

ADR 1 **Address 1** **04 : 0 - 7 (17h)**

ADR1 is used to specify the modem's internal RAM address to be read or written (data RAM if CRAM1=0 or coefficient RAM if CRAM1=1) during a RAM access cycle. The 16-bit real and imaginary data to be writter into RAM or read out of RAM is placed in XDM1, XDL1 and YDM1, YDL1. The address value in ADR1 also determines the data to be output by the modem via the eye pattern interface (SEPXO and SEPYO). At power-up, ADR1 defaults to 17h which corresponds to the rotated equalizer output (normal eye pattern output).

ADR2 **Address2** **14 : 0 - 7 (-)**

ADR2 is used to specify the modem' sinternal RAM address to be read or written (data RAM if CRAM2 = 0 or coefficient RAM if CRAM2 = 1) during a RAM access cycle. The 16 - bit real and imaginary data to be written into RAM or read out of RAM is placed in XDM2, XDL2 and YDM2, YDL2.

Table 1. Dual Port Interface Memory Map

Register Function	Reg. Addr. (Hex)	Default Value (Bin)	Bit							
			7	6	5	4	3	2	1	0
Interrupt Handling	1F	- XX0 - XX0	PINTA	-	-	PINTE	PIRQ	-	-	CSET
	1E	- - 0X - 0X -	INTA2	INTA1	INTE2	-	BDA2	INTE1	-	BDA1
Not Used	1D	XXXXXXXX	-	-	-	-	-	-	-	-
DTMF Status	1C	- - - - - - - -	DEDT	DTDT	DOTS	DSDET	DTMFW			
Not Used	1B	XXXXXXXX	-	-	-	-	-	-	-	-
	1A	XXXXXXXX	-	-	-	-	-	-	-	-
	19	XXXXXXXX	-	-	-	-	-	-	-	-
	18	XXXXXXXX	-	-	-	-	-	-	-	-
	17	XXXXXXXX	-	-	-	-	-	-	-	-
	16	XXXXXXXX	-	-	-	-	-	-	-	-
RAM Access2 Control and Status and Parallel Data Buffer	15	00000000	RA2	-	AHEOF	-	-	BRT2	WT2	CRAM2
	14	- - - - - - - -	RAM ADDRESS2 (ADR2)							
	13	- - - - - - - -	X RAM DATA2 MSB (XDM2)							
	12	- - - - - - - -	X RAM DATA2 LSB (XDL2)							
	11	- - - - - - - -	Y RAM DATA2 MSB (YDM2)							
	10	- - - - - - - -	Y RAM DATA2 LSB (YDL2) / DATA BUFFER (DBFR)							

Table 1. Dual Port Interface Memory Map (Continued)

Register Function	Reg. Addr. (Hex)	Default Value (Bin)	Bit							
			7	6	5	4	3	2	1	0
Modem Status	0F	- - XXXX - -	IED		-	-	-	-	CTSB	DCDB
Not Used	0E	XXXXXXXX	-	-	-	-	-	-	-	-
High Speed Status	0D	- - XXXXXX	REC	PNDT	-	-	-	-	-	-
	0C	XX - - - - - -	-	-	DATM	SCR1S	PNS	P2S	P1S	SILIDL
Programmable	0B	00000000	INTMSK							
Interrupt Control	0A	00000000	ITRG		INTML	INTADR				
High Speed Control and HDLC Control and Status	09	- 000 - - - -	ORUR	SAVEQ	FRZEQ	ZCLMP	ABORT	EOHF	CRCE	FLG
Tone Detect and High Speed Control & Status	08	- - - 0 - XXX	TD3	TD2	TD1	CASC	PNSX	-	-	-
Mode Control	07	00001000	RTSB	TRND	PDME	SHTRN	EPTE	-	-	HDLCE
	06	00010100	CONFIG							
RAM Access1	05	10000101	RA1	-	-	-	-	BRT1	WT1	CRAM1
Control & Status	04	00010111	RAM ADDRESS1 (ADR1)							
and Programmable	03	- - - - - - - -	X RAM DATA1 MSB (XDM1)							
Interrupt Control	02	- - - - - - - -	X RAM DATA1 LSB (XDL1)							
	01	- - - - - - - -	Y RAM DATA1 MSB (YDM1)							
	00	- - - - - - - -	Y RAM DATA1 LSB (YDL1)							

AHEOF Automatic HDLC End of Frame 15 : 5 (0)

When AHEOF is set while in HDLC transmit mode, the modem automatically generates and transmits the FCS (frame check sequence) and at least one closing flag upon detecting an underrun condition in the transmission of data. AHEOF is valid only when the modem is configured for HDLC mode (HDLCE is set).

BDA 1 Buffer Data Available No.1 1E : 0 (-)

When BDA1 has been set by the modem, the modem has either written or read buffer data to/from the YDL1 register. The setting of the BDA1 bit can be setup to cause an $\overline{IRQ}$ interrupt (see INTE1 and INTA1 bit descriptions). When the host microprocessor reads or writes the YDL1 register, the modem automatically resets the BDA1 bit.

BDA 2 Buffer Data Available No.2 1E : 3 (-)

When BDA2 has been set by the modem and the modem is in parallel data mode (PDME is set), with or without HDLC enabled, transmit data has been read from DBFR by the modem (transmit mode) or received data has been written by the modem into DBFR (receive mode). When the modem is in serial mode (PDME is reset), the modem sets BDA2 whenever data has been read from or written into YDL2. The setting of the BDA2 bit can be setup to cause an $\overline{IRQ}$ interrupt (see INTE2 and INTA2 bit descrip - tions). When the host microprocessor reads or writes the YDL2/DBFR register, the modem automatically resets the BDA2 bit.

BRT 1 Baud Rate 1 05 : 2 (1)

When BRT1 is set, RAM access for ADR1 takes place at the baud rate (the baud rate depends on the se - lected configuration), otherwise it occurs at the sample rate (9600Hz). This bit must be zero in FSK, Tone or DTMF receive modes.

BRT 2 Baud Rate 2 15 : 2 (0)

When BRT2 is set RAM access for ADR2 takes place at the baud rate (the baud rate depends on the se - lected configuration). Otherwise it occurs at the sample rate (9600Hz). This bit must be zero in FSK, Tone or DTMF receive modes.

CASC Select 12th Order Filter Cascade 08 : 4 (0)

When CASC is set, the tone detectors are cascaded to form one 12th order filter (TD3 is the output status bit for the 12th order filter cascade). When CASC is reset, the three tone detectors operate as three parallel independent 4th order filters. The 12th order mode is only valid in the FSK , FSK and DTMF receiver modes when $\overline{RTS}$ is off and RTSB is reset.

CONFIG Configuration 06 : 0 - 7 (14th)

The contents of CONFIG determine the modem operating configuration. The following table lists all valid 8 - bit configuration codes and the corresponding selected configuration.:

CONFIG (Hexadecimal)	Selected Modem Configuration
31	V.17 14,400 bps TCM (KS16114)
32	V.17 12,000 bps TCM (KS16114)
34	V.17 9,600 bps TCM (KS16114)
38	V.17 7,200 bps TCM (KS16114)
14	V.29 9,600 bps
12	V.29 7,200 bps
11	V.29 4,800 bps
0A	V.27 ter 4,800 bps
09	V.27 ter 2,400 bps
20	Transmit : V.21 Ch 2 300 bps (FSK) Receive : V.21 Ch 2 300 bps (FSK) and tone detector
21	Transmit : V.21 Ch 2 300 bps (FSK) Receive : V.21 Ch 2 300 bps (FSK), tone detector and DTMF receiver
80	Transmit : Dual tone Receive : Tone detector

At power up, the modem defaults to V.29 9,600 bps. After changing the contents of CONFIG, the host must set the CSET bit to instruct the modem to carry out the configuration change. When the configu - ration change has been completed, the modem resets the CSET bit.

CRAM1 Coefficient RAM 1 Select 05 : 0 (1)

When CRAM1 is set, ADR1 addresses coefficient RAM and when CRAM1 is reset, ADR1 addresses data RAM. This bit must be set according to the desired RAM address.

CRAM2 Coefficient RAM 2 Select 15 : 0 (1)

When CRAM2 is set, ADR2 addresses coefficient RAM and when CRAM2 is reset, ADR2 addresses data RAM. This bit must be set according to the desired RAM address.

CRCE Cyclic Redundancy Check Error 09 : 1 (-)

When CRCE and EOHF are both set, the received frame is erroneous. If CRCE is reset and EOHF is set the received frame is correct. CRCE becomes valid immediately before EOHF is set.

CSET Configuration Setup 1F : 0 (0)

The host informs the modem to implement a configuration change by setting the CSET bit. The host sets the CSET bit after writing a configuration code into the CONFIG bits (register 6:0-7).
The CSET bit is reset by the modem after the configuration change has been completed.

CTSB Clear to Send Bit 0F : 1 (-)

When CTSB is set the modem has completed the training sequence transmission and any data present at TXDI (if PDME is reset) or DBFR (if PDME is set) will be transmitted. CTSB parallels the operation of the $\overline{\text{CTS}}$ output pin.

DATM Data Mode 0C : 5 (-)

Status bit DATM is set by the modem to indicate that the transmitter or receiver is in data mode. Data mode implies that the modem is in a state where user data may be transmitted or received.

DBFR Transmit/Receive Data Buffer 10 : 0 - 7 (-)

When the modem is configured in parallel data mode (PDME is set), the host microprocessor reads parallel received data from DBFR or writes parallel transmit data into DBFR. DBFR data is transmitted bit 0 first. Transmission and reception of data is synchronized by polling the BDA2 status bit or by $\overline{\text{IRQ}}$ interrupts (see INTE2 and INTA2 bit descriptions).

DCDB Data Carrier Detect Bit 0F : 0 (-)

Status bit DCDB is set by the modem when the receiver has completed the reception of a training sequence or has detected energy above the $\overline{\text{RLSD}}$ turn on threshold and is receiving data. DCDB parallels the operation of the $\overline{\text{RLSD}}$ output pin.

DEDT DTMF Early Detection 1C : 7 (-)

Status bit DEDT is the same as DTDT.

DOTS DTMF On Time Satisfied 1C : 5 (-)

Status bit DOTS is set by the modem when the on - time requirements for a DTMF signal is satisfied. The modem resets this bit either after DSDET is set or if the received signal fails to meet the DTMF signal requirements.

DSDET DTMF Signal Detected 1C : 4 (-)

Status bit DSDET is set by the modem when a DTMF signal that satisfies all the detection requirements has been detected. After detection, this bit must be reset by the host.

DTDT Dual Tone Detected 1C : 6 (-)

When a signal that meets all DTMF requirements except on - time, off - time and cycle time is detected, the modem sets status bit DTDT. The encoded DTMF value is available at this time in DTMFW. This bit is reset by the modem either after DSDET is set or if the signal fails to meet the DTMF detection requirements.

DTMFW DTMF Output Word 1C : 0 - 3 (-)

The encoded DTMF output is written into this field when a DTMF tone is being received (status bit DSDET is set by the modem). The DTMF output codes are:

DTMF Symbol	Encoded Output	DTMF Symbol	Encoded Output
1	0	3	8
4	1	6	9
7	2	9	A
*	3	#	B
2	4	A	C
5	5	B	D
8	6	C	E
0	7	D	F

EOHF End of HDLC Frame 09 : 2 (-)

In the transmit mode when AHEOF is reset, the EOHF bit is used to instruct the modem to send the 16 - bit FCS and ending flag of a HDLC frame. The host must set the EOHF bit after the modem has read the last byte of the frame from DBFR. The modem will then reset EOHF after generating and sending the end of frame sequence. If AHEOF is set, the modem will set EOHF and output the 16 bits FCS and at least one ending flag when an underrun condition occurs. EOHF is reset when the frame closing flag is sent.

In the receive mode, the modem sets EOHF when it has received a frame ending flag and updates CRCE. The host must reset EOHF before the ending flag of the following frame.

EPTE Echo Protector Tone Enable 07 : 3 (1)

When this bit is set, the modem transmits unmodulated carrier for 187.5 ms followed by 20 ms of silence prior to sending the training sequence. With EPTE reset the modem will immediately send the training sequence except in the V.29 configuration. In the V.29 configuration the modem precedes the training sequence with 20 ms of silence.

FLG FLAG Mode 09 : 0 (0)

When FLG is set while in the HDLC transmitter mode, the modem transmits a flag sequence.
In the HDLC receive mode, the modem sets the FLG bit when it receives a flag sequence.

FRZEQ **Freeze Equalizer** **09 : 5 (0)**

When control bit FRZEQ is set, equalizer tap updating is disabled freezing the equalizer tap coefficients at their current value.

HDLCE **HDLC Enable** **07 : 0 (0)**

When control bit HDLCE is set, the modem performs HDLC framing. To activate or deactivate HDLC mode the host must set or reset HDLCE and PDME and then set the CSET bit to instruct the modem to carry out the configuration change.

IED **Instantaneous Energy Detector** **0F : 6 - 7(0)**

IED is a fast responding energy detection status indicator. The received signal level is indicated by the following codes:

IED	Energy Level
0	No Energy Present
1	Invalid
2	Invalid
3	Energy Above Turn - On Threshold

INTA 1 **Interrupt Active 1** **1E : 6 (-)**

If BDA 1 is set by the modem when INTE 1 is set, the modem asserts $\overline{IRQ}$ and sets status bit INTA 1 to indicate that BDA 1 caused the interrupt. The host resets INTA 1 by reading or writing register 0.

INTA 2 **Interrupt Active 2** **1E : 7 (-)**

If BDA 2 is set by the modem when INTE 2 is set, the modem asserts $\overline{IRQ}$ and sets status bit INTA 2 to indicate that BDA 2 caused the interrupt. The host resets INTA 2 by reading or writing register 10h.

INTADR **Interrupt Address** **OA : 0 - 4 (0)**

The contents of INTADR specify the register number on which the programmable interrupt will take effect on. The host register addresses and the corresponding INTADR 5 - bit codes are provided in the table.

Host Register (Hex)	INTADR (Hex)	Host Register (Hex)	INTADR (Hex)
01	10	11	18
02	01	12	09
03	11	13	19
04	02	14	0A
05	12	15	1A
06	03	16	0B
07	13	17	1B
08	04	18	0C
09	14	19	1C
0A	05	1A	0D
0B	15	1B	1D
0C	06	1C	0E
0D	16	1D	1E
0E	07	1E	0F
0F	17	1F	1F

INTE 1 Interrupt Enable 1 1E : 2 (0)

The modem will assert $\overline{IRQ}$ and set INTA 1 when BDA 1 is set by the modem if control bit INTE 1 is set (interrupt enabled). If INTE 1 is reset (interrupt disabled) $\overline{IRQ}$ and INTA 1 are unaffected by BDA 1.

INTE 2 Interrupt Enable 2 1E : 5 (0)

The modem will assert $\overline{IRQ}$ and set INTA 2 when BDA 2 is set by the modem if control bit INTE 2 is set (interrupt enabled). If INTE 2 is reset (interrupt disabled) $\overline{IRQ}$ and INTA 2 are unaffected by BDA 2.

INTML Interrupt Mask Logic (AND / OR Logic) 0A : 5 (0)

When control bit INTML is set when programmable interrupts are enabled (PINTE is set), the modem will logically AND the contents of the interface memory register specified by INTADR with the contents of INTMSK. Thus, the $\overline{IRQ}$ condition will be met if all the bits in the specified register masked by INTMSK are set. When control bit INTML is reset when programmable interrupts are enabled (PINTE is set), the modem will logically OR the contents of the interface memory register specified by INTADR with the contents of INTMSK. Thus, the $\overline{IRQ}$ condition will be met if any the bits in the specified register masked by INTMSK are set. Note that ITRIG places additional interrupt triggering requirements on the programmable interrupt which must also be met in order for $\overline{IRQ}$ to be asserted by the modem.

INTMSK Interrupt Bit Mask 0B : 0 - 7 (0)

A bit mask function is performed by this byte on the register specified by INTADR for the programmable interrupt. The INTML bit determines whether a logical AND or a logical OR masking operation is performed with the contents of the register specified by INTADR and the contents of INTMSK. Note that ITRIG places additional triggering requirements which must also be met in order for $\overline{IRQ}$ to be asserted by the modem. Additionally, programmable interrupts must be enabled (PINTE set) and PIRQ must have been reset by the host prior to the occurrence of the interrupt condition in order for $\overline{IRQ}$ to be asserted by the modem.

ITRIG Interrupt Triggering 0A : 6 -7 (0)

ITRIG places triggering polarity requirements on the programmable interrupt which must be met in order for the modem to assert $\overline{IRQ}$. The four possible ITRIG settings and their corresponding function are described below.

ITRIG (Bin)	Description
00	Continuous interrupt when interrupt condition
01	Interrupt when interrupt condition from false to true
10	Interrupt when interrupt condition from true to false
11	Interrupt when any change in interrupt condition

ORUR Overrun / Underrun 09 : 7 (-)

During HDLC parallel mode data transmission (HDLCE and PDME are set) the host microprocessor must load DBFR with consecutive transmit data bytes within eight bit times of each other. If more than eight bit times elapse between transmit data bytes being written into DBFR, an underrun condition is detected by the modem and is indicated by the ORUR and ABORT bits being set. When an underrun condition occurs, the modem clamps the transmit data to ones. The clamping of transmit data will continue until the host microprocessor resets the ABORT bit. When the host microprocessor resets the ABORT bit, the modem will complete the transmission of the current group of eight binary ones and will then proceed to start the transmission of the next frame if BA2 has been reset (the host reading or writing DBFR causes BA2 to reset). Otherwise, the modem will transmit continuous HDLC flags.

In the receive mode, the modem indicates an overrun condition by setting ORUR. An overrun condition occurs when the host microprocessor fails to read the received data in DBFR before it is overwritten by the next received byte. The host must reset the ORUR bit before the next received data overrun condition can be indicated by the modem setting ORUR.

The ORUR function is disabled if the AHEOF control bit is set. The ORUR bit is valid only while the modem is configured for HDLC mode (HDLCE is set).

P1S P1 Sequence 0C : 1 (-)

In the high speed transmit mode (all data configurations except FSK), the modem sets P1S to indicate that the P1 sequence is being transmitted. The P1 sequence is also referred to as the echo protector tone and consists of 187.5 ms of unmodulated carrier followed by 20 ms of silence. In the receive mode the P1S bit has no significance.

P2S P2 Sequence 0C : 2 (-)

In the high speed transmit mode (all data configurations except FSK), the modem sets P2S to indicate that the P2 sequence is being transmitted. In the receive mode, the modem sets P2S to indicate that the modem has detected an incoming P2 sequence and is in the process of searching for the P2 to PN transition.

PDME Parallel Data Mode Enable 07 : 5 (0)

When the PDME control bit is set, the modem is configured for parallel data mode. During parallel data mode transmission, the modem accepts transmit data from DBFR (10 : 0 - 7) rather than the TXDI serial input. During the receive mode the modem simultaneously outputs the received data to DBFR (10 : 0 - 7) and the RXDO serial output. HDLC framing is performed only in parallel data mode. When PDME is reset, the modem is in serial data mode and the modem accepts transmit data via the TXDI serial input and issues received data via the RXDO serial output.

PINTA Programmable Interrupt Active 1F : 7 (-)

When programmable interrupts are enabled (PINTE is set). PINTA is set by the modem when the interrupt condition specified by INTMSK, INTADR, ITRIG, and INTML is true. The modem asserts $\overline{IRQ}$ if PIRQ has been previously reset by the host. PINTA is automatically reset when the host resets PIRQ.

PINTE Programmable Interrupt Enable 1F : 4 (0)

When PINTE is set and the interrupt condition as specified by INTMSK, INTADR, ITRIG, and INTML is true, the modem asserts $\overline{IRQ}$ if control bit PIRQ has been previously reset by the host. Bits INTMSK, INTADR, ITRIG, INTML, and PIRQ have no effect on $\overline{IRQ}$ and PINTA when programmable interrupts are disabled (PINTE is reset).

PIRQ Programmable Interrupt Request 1F : 3 (-)

When PINTE is set and the interrupt condition is true as specified by INTMSK, INTADR, ITRIG, and INTML, the modem asserts $\overline{IRQ}$ if control bit PIRQ has been previously reset by the host, PIRQ is set by the modem when the programmable interrupt condition is true. The host must reset PIRQ after servicing the interrupt. The modem will not assert $\overline{IRQ}$ when an interrupt condition is met unless PIRQ is reset.

PNDT PN Detected 0D : 6 (-)

The modem receiver sets the PNDT status bit to indicate that it has detected the beginning of the PN segment of the training sequence. PNDT remains set during the reception of the PN segment and is reset at the end of the PN segment.

PNS PN Sequence 0C : 3 (-)

In the high speed transmit mode, the modem sets the PNS bit to indicate that the PN segment of the training sequence is being transmitted. In the high speed receive mode, the PNS bit is set by the modem while it is receiving the PN segment of the training sequence.

PNSX PN Success 08 : 3 (-)

The modem sets the PNSX status bit when it has successfully trained at the end of the PN segment of the high speed training sequence. If training fails, PNSX is reset. PNSX is valid after the DCDB bit is set.

RA1 RAM Access 1 05 : 7 (1)

When the host sets the RA1 control bit, the modem accesses the RAM addressed by ADR1 and the CRAM1 bit and performs a read or write as determined by the WT1 control bit.

RA2 RAM Access 2 15 : 7 (1)

When the host sets the RA2 control bit, the modem accesses the RAM addressed by ADR2 and the CRAM2 bit and performs a read or write as determined by the WT2 control bit.

REC Receive State 0D : 7 (-)

The modem sets the REC status bit to indicate that the modem is in the receive state. When the REC bit is reset, the modem is in the transmit state.

RTSB Request to Send Bit 07 : 7 (0)

The modem begins a transmit sequence when the RTSB bit is set or the $\overline{\text{RTS}}$ input pin is driven low. The modem will continue to transmit as long as RTSB is set or $\overline{\text{RTS}}$ is low.

SAVEQ Save Equalizer 09 : 6 (0)

When the SAVEQ bit is set by the host, the taps of the adaptive equalizer are not cleared when entering the training state, thus saving the equalizer tap coefficients obtained during the previous training.

SCR1S Scrambled Ones Sequence 0C : 4 (-)

In the high speed transmit mode, the modem sets the SCR1S status bit to indicate that the modem is sending the scrambled ones sequence. In the high speed receive mode, the modem sets the SCR1S status bit to indicate that the modem is receiving the scrambled ones sequence. In the receive mode, SCR1S is reset to indicate that the modem is not receiving the scrambled ones sequence.

SHTRN Short Train 07 : 4 (0)

The KS16114 supports V.17 and V.27ter short train while the KS16112 supports V.27ter short train.
To utilize these short train modes, the receiver must first be trained using a long training sequence at the same speed as the subsequent short training sequence. After the long training sequence has been successfully received, the host may configure the modem for short train mode by setting SHRTN. At this time the host must also set the SAVEQ bit to preserve the equalizer tap coefficients obtained during the long train.

SILIDL Silence / Idle 0C : 0 (-)

When in the high speed transmit mode, the modem sets the SILIDL status bit to indicate that the modem is transmitting silence. In the high speed receive mode, the modem sets the SILIDL status bit to indicate that the modem is in the idle state waiting for energy to be received.

TD1 Tone Detector No.1 08 : 5 (-)

The TD1 bit is set when the modem detects energy above the turn-on threshold of tone detector No 1.
As the default, tone detector No.1 is programmed to detect energy in the 2100 Hz ± 25 Hz frequency range.
All three tone detectors (TD1, TD2 and TD3) have host programmable filter coefficients.
Tone detector No. 1 is operational in FSK, FSK and DTMF receiver and Tone configurations and whenever the modem is not transmitting.

TD2 Tone Detector No.2 08 : 6 (-)

The TD2 bit is set when the modem detects energy above the turn on threshold of tone detector No 2.
As the default, tone detector No. 2 is programmed to detect energy in the 1100 Hz ± 30 Hz frequency range.
All three tone detectors (TD1, TD2 and TD3) have host programmable filter coefficients.
Tone detector No. 2 is operational in FSK, FSK and DTMF receiver and Tone configurations and whenever the modem is not transmitting.

TD3 Tone Detector No.3 08 : 7(-)

The TD3 bit is set when the modem detects energy above the turn on threshold of tone detector No. 3. As the default, tone detector No. 3 is programmed to detect energy in the 462Hz ± 14Hz frequency range. All three tone detectors (TD1, TD2 and TD3) have host programmable filter coefficients.
Tone detector No. 3 is operational in FSK, FSK and DTMF receiver and Tone configurations and whenever the modem is not transmitting. TD3 serves as the output status indicator when the CASC bit is set forming a 12th order filter using TD1, TD2, and TD3 (see CASC bit description).

TRND Training Disable 07 : 6(0)

When the host sets the TRND bit while in the receive mode, the modem will not recognize the training sequence and will not enter the training state. In the transmit mode, the modem will not transmit the training sequence when the $\overline{RTS}$ input is active or the RTSB bit is set.

WT1 RAM Write 1 05 : 1 (0)

When the WT1 control bit is set, the modem reads 16 bits of data from the Y RAM Data 1 registers (YDM 1, YDL 1) and writes it into its internal RAM as addressed by ADR1 and CRAM1 immediately following the host setting the RA1 control bit. If the MSB of ADR1 is a zero, the data is copied into X RAM, if the MSB of ADR1 is a one, the data is copied into Y RAM. When WT1 is reset the modem reads real and imaginary 16 - bit data from its internal RAM locations as addressed by ADR1 and CRAM1 and writes it into the X RAM Data 1 registers (XDM1, XDL1) and Y RAM Data 1 registers (YDM1, YDL1) immediately after the host sets the RA1 control bit.

WT2 RAM Write 2 15 : 1 (0)

When the WT2 control bit is set, the modem reads 16 bits of data from the Y RAM Data 2 registers (YDM1, YDL1) and writes it into its internal RAM as addressed by ADR2 and CRAM2 immediately following the host setting the RA2 control bit. If the MSB of ADR2 is a zero, the data is copied into X RAM. If the MSB of ADR2 is a one, the data is copied into Y RAM. When WT2 is reset, the modem reads real and imaginary 16bits data from its internal RAM locations as addressed by ADR2 and CRAM2 and writes it into the X RAM Data 1 registers (XDM1, XDL1) and Y RAM Data 1 registers (YDM1, YDL1) immediately after the host sets the RA2 control bit.

XDL1 X RAM Data 1 LSB 02 : 0 - 7 (-)

XDL1 contains the least significant byte of the 16-bit X RAM1 Data word used while reading XRAM locations.

XDL2 X RAM Data 2 LSB 12 : 0 - 7 (-)

XDL2 contains the least significant byte of the 16-bit X RAM2 Data word used while reading XRAM locations.

XDM1 **X RAM Data 1 MSB** **03 : 0 - 7 (-)**

XDM1 contains the most significant byte of the 16-bit X RAM1 Data word used while reading XRAM locations.

XDM2 **X RAM Data 2 MSB** **13 : 0 - 7 (-)**

XDM2 contains the most significant byte of the 16-bit X RAM2 Data word used while reading XRAM locations.

YDL1 **Y RAM Data 1 LSB** **00 : 0 - 7 (-)**

YDAL1 contains the least significant byte of the 16-bit Y RAM1 Data word used while reading YRAM locations.

YDL2 **Y RAM Data 2 LSB** **10 : 0 - 7 (-)**

YDAL2 contains the least significant byte of the 16-bit Y RAM2 Data word used while reading YRAM locations.

YDM1 **Y RAM Data 1 MSB** **01 : 0 - 7 (-)**

YDM1 contains the most significant byte of the 16-bit Y RAM1 Data word used while reading YRAM locations.

YDM2 **Y RAM Data 2 MSB** **11 : 0 - 7 (-)**

YDM2 contains the most significant byte of the 16-bit Y RAM2 Data word used while reading YRAM locations.

ZCLMP **Zero Clamp** **09 : 4 (0)**

When both ABORT and ZCLMP are set the modem will transmit continuous zeros. When ZCLMP is reset and ABORT is set the modem will send continuous ones. With ABORT reset ZCLMP is disabled.

3 Digital Signal Processor (DSP) RAM Access

The internal DSP random access memory (RAM) is organized into two parts : real (XRAM) and imaginary (YRAM). The host processor has access to both the XRAM and the YRAM.

3.1 Interface Memory Access of DSP RAM

The dual port interface memory is used during host-to-DSP RAM or DSP RAM-to-host data transfers. The DSP RAM address accessed is determined by the address stored in the DSP interface memory (ADR_X, where X =1 or 2). The words (16 bits each) are transferred once each baud or once each sampling period (determined by BRT_X bit, where X= 1 or 2). The sampling rate is 9,600 Hz for all configurations, but the baud rate or symbol rate is determined by the selected configuration (see Table 7). Two RAM access bits in the modem interface memory instruct the DSP to access the XRAM and/or the YRAM. The host first sets the RA1 and/or RA2 bits which are tested by the DSP each baud or sample period, as determined by the corresponding BRT_X bit setting. The DSP RAM access functions, codes and registers are listed in Table 2.

Table 2. Modem DSP RAM Access Codes

Item No.	Function	BRT_X	$CRAM_X$	ADR_X	X,Y
1	Received Signal Samples	0	0	15	X
2	AGC Gain Word	0	1	15	X
3	Carrier Detect Turn on Threshold	0	1	37	X
4	Carrier Detect Turn off Threshold	0	1	B7	X
5	Receiver Sensitivity, MAXG	0	1	24	X
6	Tone 1 Frequency	0	1	21	X
7	Tone 1 Transmit Output Level	0	0	22	X
8	Tone 2 Frequency	0	1	22	X
9	Tone 2 Transmit Output Level	0	0	23	X
10	Transmit Output Level	0	0	21	X
11	Equalizer Tap Coefficients	1	1	3A - 69	X,Y
12	Rotated Equalizer Output, Eye Pattern	1	1	17	X,Y
13	Decision Points, Ideal Points	1	0	17	X,Y
14	Error Vector	1	1	1D	X,Y

Table 2. Modem DSP RAM Access Codes (Continued)

Item No.	Function	BRT_X	$CRAM_X$	ADR_X	X,Y
15	Rotation Angle	1	1	0C	Y
16	Frequency Correction	1	1	18	X
17	Eye Quality Monitor, EQM	1	1	0D	X
18	Minimum DTMF On Time	0	1	1F	X
19	Minimum DTMF Off Time	0	0	1F	X
20	Negative Twist Control (DTMF)	0	0	1E	X
21	Positive Twist Control (DTMF)	0	0	9E	Y
22	Number of Additional Flags (HDLC)	0	1	85	Y
23	TD1 Tone Detector Coefficients	0	1	25 - 2A A5 - AA	X Y
24	TD2 Tone Detector Coefficients	0	1	2B - 30 AB - B0	X Y
25	TD3 Tone Detector Coefficients	0	1	31 - 36 B1 - B6	X Y
26	Maximum Speech Energy	0	1	IE	X
27	RX BPF compromise filter	0	1	6A-89 EA-09	X Y

3.2 Host DSP Read and Write Procedures

The modem DSP RAM consists of four memory banks : data RAM real, data RAM imaginary, coefficient RAM real, and coefficient RAM imaginary. When accessing the main RAM the desired RAM access code needs to be written into ADR_X (X = 1,2), with 1 and 2 referring to RAM access 1 and 2 respectively. The RAM location is specified by bits 0-6 and bit 7, when zero, specifies a real (XRAM) RAM location, and when one, an imaginary (YRAM) RAM location. The BRT_X (X = 1,2) bit controls whether the data access takes place at the baud rate or the sampling rate. The $CRAM_X$ controls whether the data RAM ($CRAM_X$ is reset) or the coefficient RAM ($CRAM_X$ is set) is accessed. In parallel data mode (PDME is set 1) only RAM access associated with RAM Address1 is available since register 10h is used as the transmit/receive data buffer (DBFR).

3.3 DSP RAM Read Procedure

The RAM read procedure is a 32 - bit transfer from the DSP RAM to the interface memory. Both the X and Y RAM data is transferred simultaneously. The sequence of events is as follows:

- Before accessing the DSP interface memory, first reset RA1 and/or RA2, then reset BDA1 and/or BDA2 by reading YDL1 and/or YDL2.
- Reset WT1 and/or WT2 to instruct the modem that a RAM read operation will take place when RA1 and/or RA2 is set.
- Load the RAM address into ADR1 and/or ADR2 and then set $CRAM_X$ and BRT_X to desired values, where x = 1 or 2
- Set RA1 and/or RA2 to instruct the modem to perform the RAM read operation.
- BDA1 and/or BDA2 will be set when the modem has completed the transfer from the DSP RAM to the interface memory RAM data registers.
- When the modem sets BDA1 and/or BDA2, $\overline{IRQ}$ is also asserted if INTE1 and/or INTE2 is set. INTA1 and/or INTA2 is set to inform the host that BDA1 and/or BDA2 was the source of the interrupt.
- In the order listed, read XDM1, XDL1, YDM1, and YDL1; and/or XDM2, XDL2, YDM2, and YDL2. Reading YDL1 resets INTA1 and BDA1 and/or reading YDL2 resets INTA2 and BDA2 causing $\overline{IRQ}$ to go inactive if no other interrupts are pending.

3.4 DSP RAM Write Procedure

The DSP RAM write procedure is a 16 - bit transfer from the interface memory to the DSP RAM. Thus X RAM data or Y RAM data can be transferred each baud or sample time. The sequence of events is as follows :

- Before writing to the DSP interface memory, first reset RA1 and/or RA2 and then reset BDA1 and/or BDA2 by reading YDL1 and/or YDL2, respectively.
- Write the RAM address into ADR1 and/or ADR2 and then set CRAM1 and BRT1 and/or CRAM2 and BRT2 to the desired values.

- Set WT1 and/or WT2 to instruct the modem that a RAM write operation will take place when RA1 and/or RA2 is set.

- Write the desired data into the interface memory RAM data registers YDL1 and YDM1 and/or YDL2 and YDM2.

- Set RA1 and/or RA2 to instruct the modem to perform the RAM write operation.

- BDA1 and/or BDA2 will be set when the transfer from the interface memory RAM data registers into RAM has been completed.

- When BDA1 and/or BDA2 is set, $\overline{IRQ}$ is also asserted if INTE1 and/or INTE2 is set.

- Reset INTA1 and BDA1 and/or INTA2 and BDA2 by reading or writing to YDL1 and/or YDL2. Reading or writing YDL1 and/or YDL2 also causes $\overline{IRQ}$ to return to the inactive state if no other interrupts are pending.

4 Parallel Data Transfers

Parallel data transfers use register 10h in the interface memory (DBFR). The modem and the host can synchronize data transfers by observing the BDA2 bit in the interface memory. Parallel data transfers may also be performed under $\overline{IRQ}$ interrupts (see INTE2 and INTA2 bit descriptions).

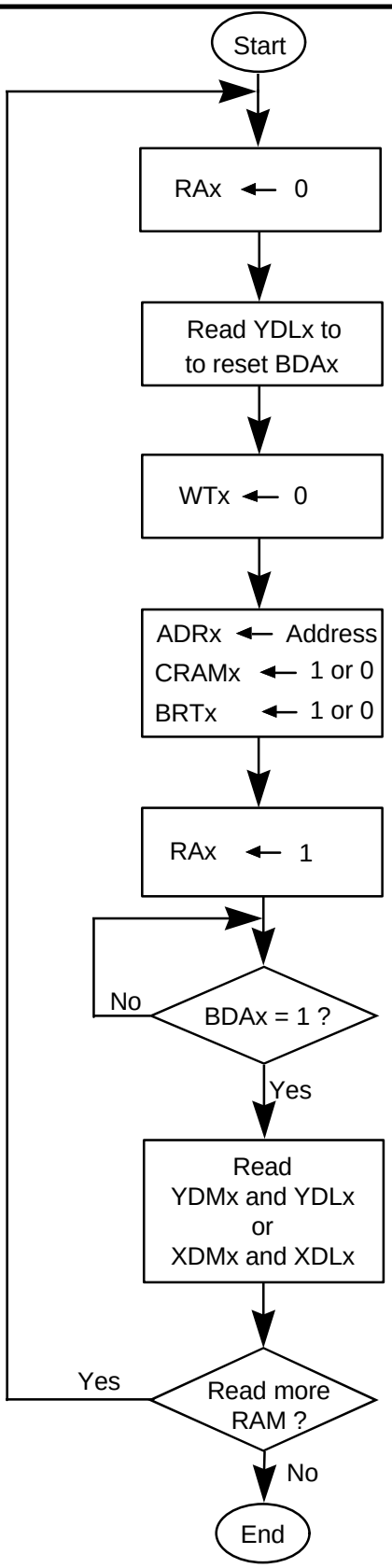
4.1 Receiving Parallel Data

During parallel data mode (PDME is set), the modem writes received data to DBFR once every eight bit times. When received data is available the modem sets the BDA2 bit. The BDA2 bit is automatically reset when the host reads DBFR. When BDA2 is set the host must take action within eight bit times or the data will be lost since the modem will overwrite DBFR (DBFR overrun condition).

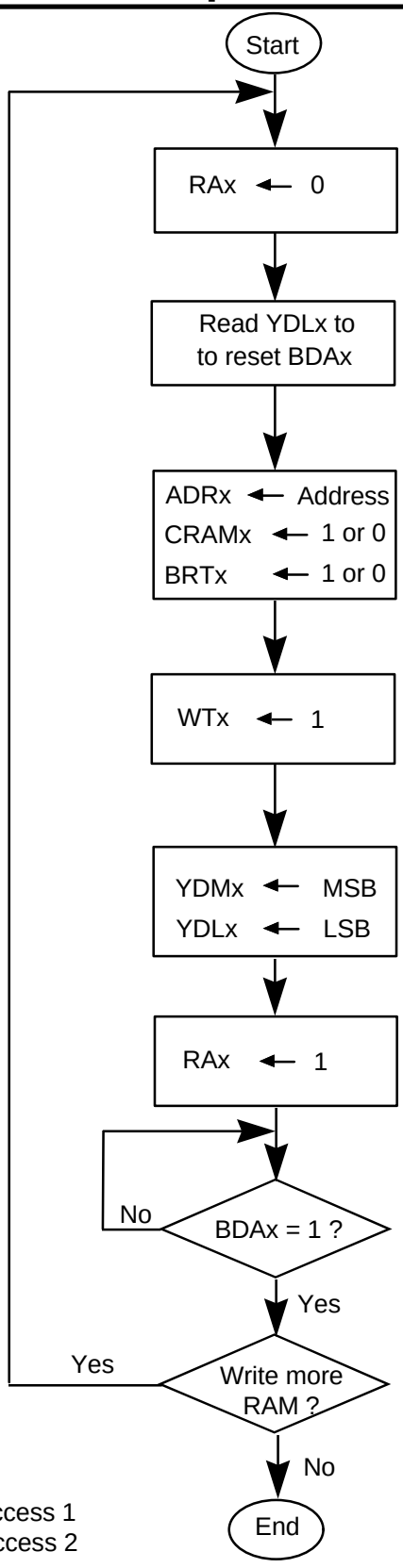
The least significant bit of register DBFR represents the oldest data and the most significant bit represents the newest data received.

4.2 Transmitting Parallel Data

During parallel data mode (PDME is set), the modem reads DBFR once every eight bit times. The BDA2 bit is set by the modem when DBFR has been read, thus requesting the next transmit data byte. The BDA2 bit is reset automatically when the host writes to DBFR. When BDA2 is set the modem must respond within eight bit times or the modem will retransmit the data in register DBFR (DBFR underrun condition).
The LSB (bit 0) in DBFR is transmitted first in time and the MSB (bit 7) is transmitted last.

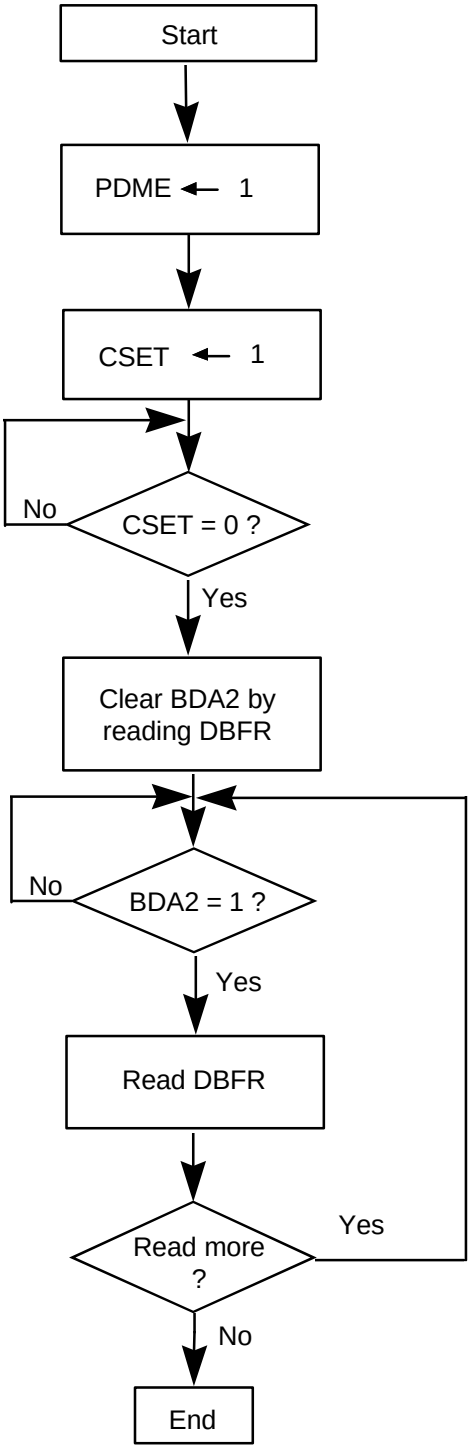


DSP Ram read

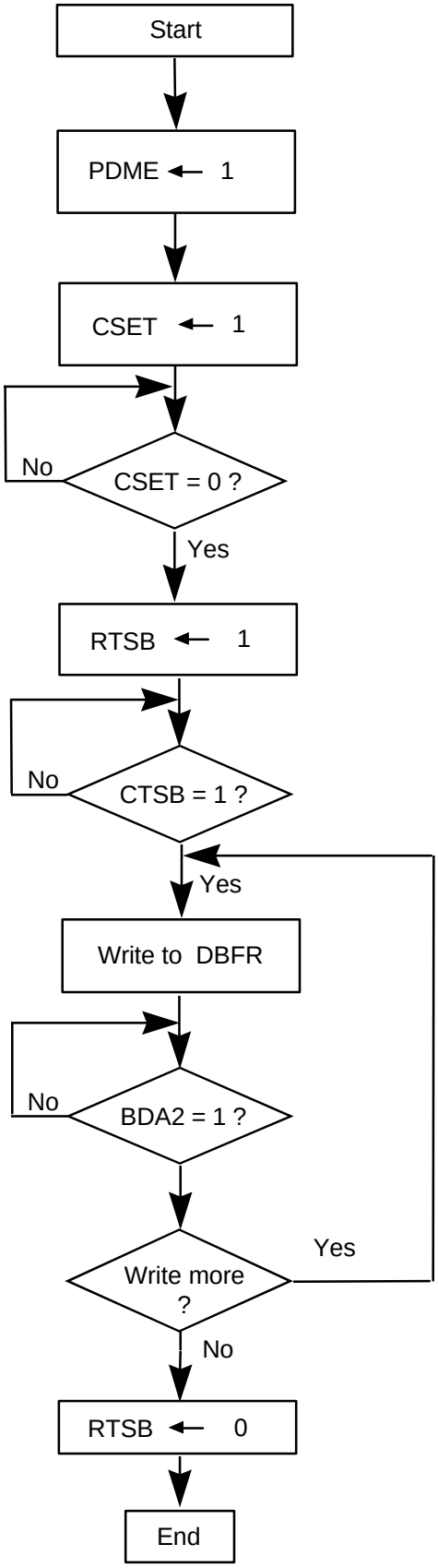


DSP RAM Write

Note: x is 1 for RAM access 1
x is 2 for RAM access 2



Parallel data receive



Parallel data transmit

5 Programmable Interrupt Feature

This feature makes it possible for the host to select an interrupt to occur on any combination of bits within an interface memory register.

5.1 Programmable Interrupt Bits

The programmable interrupt routine is executed at the sampling rate. (9,600Hz) in all configurations. When the host sets the PINTE bit and the modem sets the PINTA bit, $\overline{IRQ}$ goes active (low) when the interrupt condition is met. The PIRQ bit must be reset by the host after the interrupt service, since this bit will not be reset by the modem and no further interrupts will occur until PIRQ has been reset.

An interrupt may occur due to a single interface memory register based on any combination of bits. The register is selected by specifying the interrupt Address in the INTADR field. The interrupt bit mask register (INTMSK) selects the bits to be tested in the interface memory register specified by INTADR.

5.2 Programmable Interrupt Operation Modes

There are two operating logic modes (AND/OR) with each having four trigger options. The triggering option is selected by the ITRIG field and the logic (AND/OR) is selected by INTML.

6 DSP RAM Parameter Definitions and Scaling

In the following the DSP RAM parameters are described as they appear in Table 2

- **Received Signal Sample / Received Signal Sample (FSK)**

Format: 16 bits, signed two's complement

Equation: V_{INT} (V) = [(A / D Sample Word) h * (3.03/2 ^{15})]

$V_{EXT} = V_{INT} + LOG\ 10^{-1}$ {(AGC Gain (dB)) /20}

- **AGC Gain Word**

Format: 16 bits, unsigned

Equation: AGC Gain (dB) = 50 [1 - (AGC Gain Word) h / 2^{15}]

- **Carrier Detect Turn - On Threshold**
- **Carrier Detect Turn - Off Threshold**
- **Receiver Sensitivity, MAXG**

Format : 16 bits, two's complement, positive value

Equation: Carrier Detect Turn - on Threshold = $2185 [10^{(TON + MG)}]$

Carrier Detect Turn - off Threshold = $2185 [10^{(TOFF + MG)}]$

Receiver Sensitivity, MAXG = 655.36 [50 - Gain Limit (dB)]

Where: TON is the turn - on threshold in dB/10
TOFF is the turn - off threshold in dB/10
MG = $50 [1 - (MAXG)h/2^{15}] /10$
MAXG is programmable, default = 0FC0h

- **Tone 1 Frequency**
- **Tone 2 Frequency**

Format: 16 bits, unsigned

Equation: $N = 2^{16} / 9600 * (Frequency in Hz)$

- **Tone 1 Output Level**
- **Tone 2 Output Level**

Format: 16 bits. two's complement, positive value

Total power is the result of both tone 1 power and tone 2 power added together. These can be independently calculated using the equation for transmit output level (item 10).

- **Transmit Output Level**

  Format: 16 bits, two's complement, positive

  Equation: Transmit Output Level = 18426 [$10^{(PO/20)}$]

  Where: Po = Output Power (dBm) into 600 Ω

- **Equalizer Tap Coefficients**

  Format: 16 bits, signed two's complement, complex

  These numbers are complex and thus require two write operations per tap. One for the real part and one for the imaginary part.

- **Rotated Equalizer Output, Eye Pattern**

- **Decision Points, Ideal Points**

  Format: 16 bits, two's complement, complex

- **Error Vector**

  Format: 16 bits, two's complement, complex

  This is the difference between the received point and the nearest ideal point

- **Rotation Angle**

  Format: 16 bits, two's complement

  Equation: Rotation Angle (degree) = [(Rotation Angle Word)h/2^{16}] * 180 degrees

- **Frequency Correction**

  Format: 16 bits, two's complement

  Equation: Frequency Corr. (Hz) = [(Frequency Corr. Word)h/2^{16}] * baud in Hz

- **Eye Quality Monitor (EQM)**

  Format: 16 bits, two's complement, positive

  This is the filtered squared magnitude of the error vector.

- **Minimum DTMF On - Time**

  Format: 16 bits, two's complement, positive

  Range: 0 to 7FFFh

- **Minimum DTMF Off - Time**

  Format: 16 bits, two's complements, positive

  Range: 0 to 7FFFh

- **Negative Twist Control**

- **Positive Twist Control**

  Format: 16 bits, two's complements, Positive

  Range: 0 to 7FFFh

  These parameters control the acceptable twist (negative or positive) for the DTMF signals. To increase the acceptable twist (negative or positive) level decrease this parameters from its default value.

- **Number of Additional Flags (HDLC)**

  Format: 16 bits, two's complement, positive

  Equation: desired number of flags - 1

  This parameter specifies the number of flags between frames or at the end of the final frame in the HDLC mode.

- **TD1 Tone Detector Coefficient**

- **TD2 Tone Detector Coefficient**

- **TD3 Tone Detector Coefficient**

Format: 16 bits, two's complement

These parameters control the frequency responses of the three tone detectors. See Section Tone Detection for a detailed description of the structure of the tone detectors.

- **Maximum Speech Energy**

Format : 16 bits, two's complement

This parameter sets the ratio between the total energy (speech energy plus DTMF energy) and the DTMF tone energy before valid DTMF digits are detected. The default is 4000hex which is 3dB.

• RX compromise filter

The receiver's 32 tap complex FIR BPF filter can be host programmed to include a compromise filter. New filter taps can be downloaded from the host after the host has configured the modem for high speed operation.

HDLC OPERATION

The modem is capable of performing HDLC framing (High Level Data Link control). The modem uses the SDLC (Synchronous Data Link control) in an eight bit octet format which is a subset of HDLC.

1 HDLC Frames

Information on an HDLC link is transmitted by means of frames. The information is organized into a format specified by an international standard that enables the synchronization between the transmitter and the receiver. An HDLC frame has the following parts :

- Flags
- Address Field
- Control Field
- Information Field
- Fame Check Sequence

The frame check sequence computation uses the cyclic redundancy check (CRC) method and implement a polynomial specified in ITU-T T.30 and X.25 as follows :

$$X^{16} + X^{12} + X^{5} + 1$$

The HDLC is functional under the following transmitter and receiver modes:

- V.17 (KS16114)
- V.29
- V.27ter
- V.21 Ch. 2
- V.21 Ch. 2 with DTMF Receiver

TONE GENERATION AND DETECTION

1 DTMF Dialing

The modem includes two programmable tone generators that can be used to perform dual tone multifrequency (DTMF) dialing. The amplitude and frequency of each tone generator are programmable by the host.

1.1 DTMF Requirements

The DTMF tones consist of two sinusoidal signals, one from the high group of frequencies and the other from the low group of frequencies. The two groups of frequencies and the corresponding push button telephone characters are shown in Table 3. Signal power is defined for the combined as well as for the individual tones. The high frequency tone should be transmitted at approximately 2 dB higher power than the low frequency tone. The maximum combined power should not exceed +1 dBm and the minimum steady state power should not be less than -8 dBm. The required minimum DTMF pulse duration is 50ms, but approximately 95ms is recommended for better reliability. The required interval between DTMF pulses is 45 ms but 70 ms is preferred.

Table 3. DTMF Frequencies

	High Frequency Group			
Low Frequency Group	1209 Hz	1336 Hz	1477 Hz	1622 Hz
697 Hz	1	2	3	A
770 Hz	4	5	6	B
852 Hz	7	8	9	C
941 Hz	*	0	#	D

1.2 Setting DTMF Parameters

The amplitude and frequency of the two tones are set by the host in the DSP RAM. To generate a DTMF tone the modem needs to be in the TONE configuration (CONFIG = 80h). The host must then program the frequencies and levels of each tone. This procedure consists of writing a 16 - bit binary number into RAM using RAM access code 21h with $BRT_X = 0$ and $CRAM_X = 1$ for tone 1 and RAM access code 22h with $BRT_X = 0$ and $CRAM_X = 1$ for tone 2. The power levels are programmed by writing a 16 - bit binary number into RAM using RAM access code 22h with $BRT_X = 0$ and $CRAM_X = 0$ for tone 1 and RAM access code 23h with $BRT_X = 0$ and $CRAM_X = 0$ for tone 2. The hex numbers in these RAM location are scaled as follows :

Frequency Number = $6.8267 \times F$ (where F is the desired frequency in Hz)

Power Number = $18426^{[10(PO/20)]}$ (where P_O is the desired power level in dBm)

The hexadecimal numbers for DTMF generation are listed in Table 4. Power levels are selected to give each tone the desired output power while compensating for modem filter characteristics.

Table 4. DTMF Default Values

Digit	ADR_X	$CRAM_X$	BRT_X	Value (Hex)	Digit	ADR_X	$CRAM_X$	BRT_X	Value (Hex)
0	21	1	0	1918	8	21	1	0	16B8
	22	1	0	23A0		22	1	0	23A0
	22	0	0	65AB		22	0	0	65AB
	23	0	0	7FFF		23	0	0	7FFF
1	21	1	0	1296	9	21	1	0	16B8
	22	1	0	203D		22	1	0	2763
	22	0	0	65AB		22	0	0	65AB
	23	0	0	7FFF		23	0	0	7FFF
2	21	1	0	1296	*	21	1	0	1918
	22	1	0	23A0		22	1	0	203D
	22	0	0	65AB		22	0	0	65AB
	23	0	0	7FFF		23	0	0	7FFF
3	21	1	0	1296	#	21	1	0	1918
	22	1	0	2763		22	1	0	2763
	22	0	0	65AB		22	0	0	65AB
	23	0	0	7FFF		23	0	0	7FFF
4	21	1	0	1488	A	21	1	0	1296
	22	1	0	203D		22	1	0	2B8C
	22	0	0	65AB		22	0	0	65AB
	23	0	0	7FFF		23	0	0	7FFF
5	21	1	0	1488	B	21	1	0	1488
	22	1	0	23A0		22	1	0	2B8C
	22	0	0	65AB		22	0	0	65AB
	23	0	0	7FFF		23	0	0	7FFF
6	21	1	0	1488	C	21	1	0	16B8
	22	1	0	2763		22	1	0	2B8C
	22	0	0	65AB		22	0	0	65AB
	23	0	0	7FFF		23	0	0	7FFF
7	21	1	0	16B8	D	21	1	0	1918
	22	1	0	203D		22	1	0	2B8C
	22	0	0	65AB		22	0	0	65AB
	23	0	0.	7FFF		23	0	0.	7FFF

2 Tone Detection

2.1 Programmable Tone Detection

The modem includes three programmable independent tone detectors (called TD1, TD2, and TD3). All three tone detectors are operational when the modem is in a non - high speed mode. In the high speed mode only tone detector TD3 is operational. The default center frequencies for the tone detectors are 2100 Hz (TD1), 1100Hz (TD2), and 462 Hz (TD3). The three tone detectors can be cascaded to form a single 12th order filter by setting the CASC bit in the dual port interface memory.

Each tone detector consists of two second order filters with two zeros and two poles each, a first order energy averaging filter and a threshold comparator. A block diagram of a tone detector is shown in Figure 2.

Filter 1 has a transfer function :

$$\mathbf{H1}(z) = \frac{2\,(a0 + a1z^{-1} + a2z^{-2})}{1 + 2b1z^{-1} + 2b2z^{-2}}$$

Filter 2 has transfer function :

$$\mathbf{H2}(z) = \frac{2\,(a'0 + a'1z^{-1} + a'2z^{-2})}{1 + 2b'1z^{-1} + 2b'2z^{-2}}$$

The energy averaging filter has a transfer function :

$$\mathbf{H3}(z) = \frac{a\bullet}{1 - b''z^{1}}$$

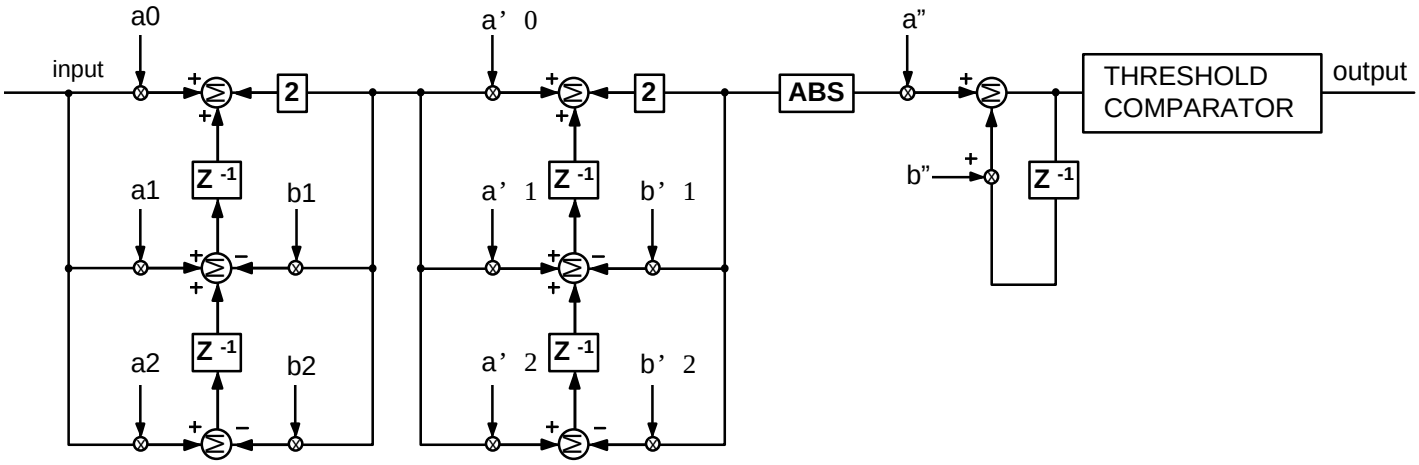


Figure 2. Tone Detector Block Diagram

The output of the threshold comparator controls the interface memory bits TD 1, TD 2, and TD3. The bits are set if the output of the energy averaging filter is equal to or greater than 1/8 of full scale. Otherwise the bits are reset.

Table 5 contains the default filter coefficient values that are loaded into RAM upon power - up. These default values correspond to default frequencies 2100 Hz (TD1), 1100 Hz (TD2), and 462Hz (TD3). Table 6 contains the RAM access codes for all filter coefficients.

Table 5. Default Tone Detector Filter Coefficients

Frequency Detected (Hz)	Bandwidth (Hz)	Freq. Offset (Hz)	Coeff. Name	Coeff. Value (Hex)	Coeff. Value (Decimal)
2100	25	18	a0 = a' 0	0198	0.01245
			b1	1A4A	0.20538
			b' 1	175A	0.18243
			b2 = b' 2	C0C4	-0.49402
1100	30	19	a0 = a' 0	011B	0.00854
			b1	60BE	0.75580
			b' 1	5E9C	0.73914
			b2 = b' 2	C0C4	-0.49402
462	14	10	a0 = a' 0	0048	0.00220
			b1	79F3	0.95273
			b' 1	7974	0.94885
			b2 = b' 2	C083	-0.49600

Table 6. Filter RAM Access Codes

Coefficient Name	RAM Access Code (Hex)			X, Y
	Tone1	Tone2	Tone3	
a0	25	2B	31	X
a1	27	2C	32	X
a2	27	2D	33	X
a' 0	28	2E	34	X
a' 1	29	2F	35	X
a' 2	2A	30	36	X
b1	A6	AC	B2	Y
b2	A7	AD	B3	Y
b' 1	A9	AF	B5	Y
b' 2	AA	B0	B6	Y
a•	A8	AE	B4	Y
b"	A9	AB	B1	Y

3 Fax Transmit/Receive

ITU-T T.30 recommendation provides procedures for facsimile transmission over the PSTN. T.30 recommendation supports two modes of transmission, low speed FSK with HDLC, and high speed data transmission for facsimile message. The high speed may or may not support HDLC which depends on implementations of ECM mode (Error Correction).

The error correction mode is negotiated in phase B of facsimile establishment phase, as shown below. If both the originating fax and the answering fax modem support error correction, then the high speed message transmission must be done using the HDLC.

Facsimile transmission is done in 5 phases as shown below,

Phase A. Call establishment. In phase A the originating fax unit will send the CalliNG (CNG) tone to indicate it is a non-speech terminal. CNG tone is a 1100 Hz tone for a duration of .5 second on and 3 off. The answering fax will send the CallED (CED) tone. CED tone is a 2100 Hz tone for a duration of 2.6 to 4 sec.

Phase B. Pre-message procedure. Phase B is for identification and selection of required facilities. In phase B the answering fax will send the DIS (Digital ID Signal) and the originating fax will send DCS (Digital Command Signal). The train check (TCF) is then transmitted by the originating fax for a duration of 1.5 second. If the answering fax receives the TCF, it will send CFR (Confirmation to Receive) and the two modem enter Phase C.

Phase C. Message Transmission. In Phase C the facsimile message will be transmitted form the originating fax to the answering fax unit.

Phase D. Post-message Procedure. In Phase D the transmitter of fax message will send EOM (End Of Message) and will wait for a response from the answering fax unit. The answering fax unit will in response return one of the following messages, MCF (Message Confirmation), RTP, RTN, PIP, or PIN.

Phase E. Call Release. After post message signals where exchanged, the two fax units enter phase E (after last page of message was transmitted) and the originating fax will send DCN (Disconnect) to indicate the Phase E. DCN message requires no response.

Phase B, D, and E are transmitted using 300 FSK and the messages are transmitted in HDLC frames. Phase C is either transmitted in HDLC frame, if error correction is required, or without HDLC. The flowcharts on next pages illustrate how to implement facsimile transmit and receive for HDLC frames and for normal high speed message transmission.

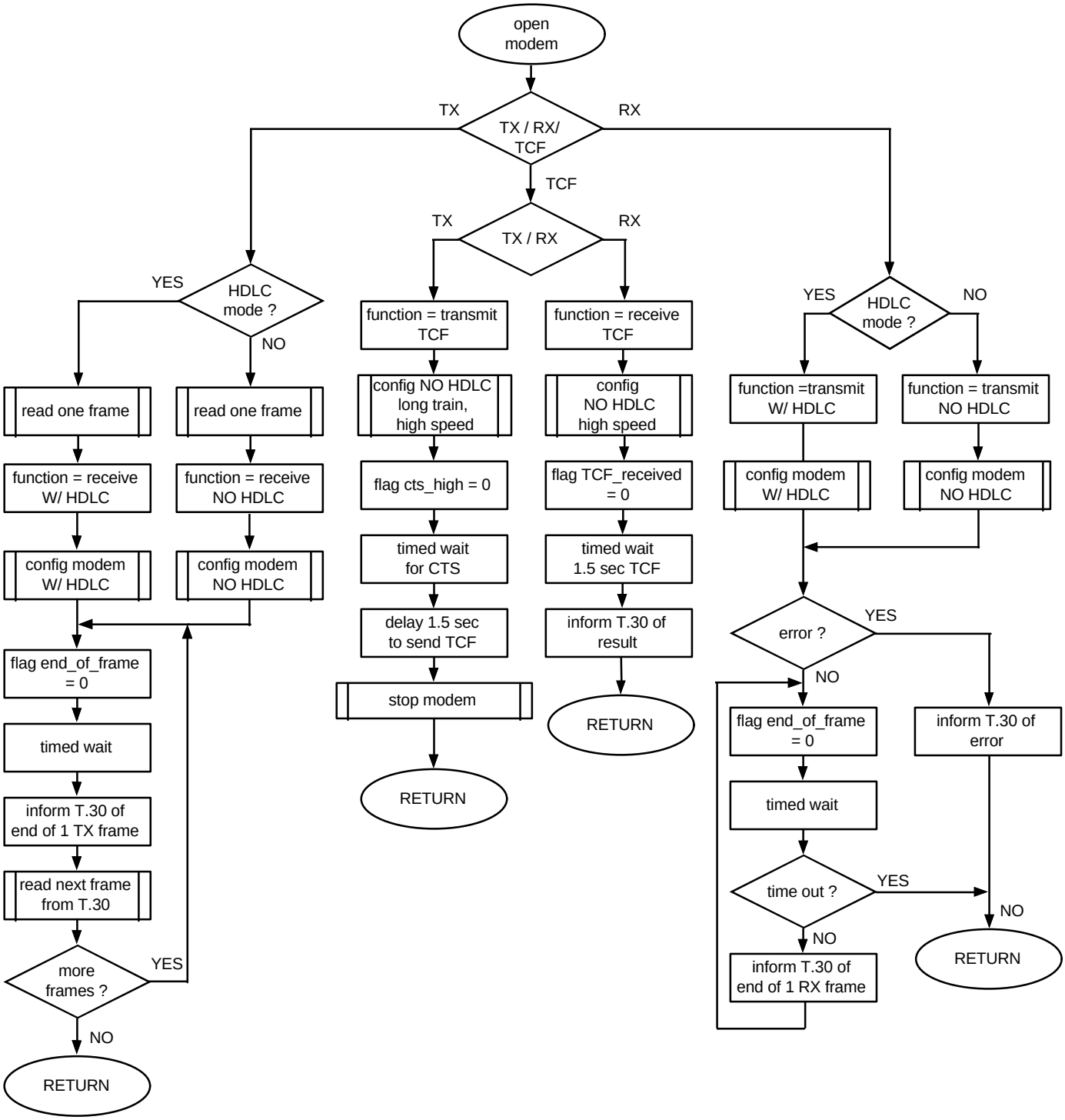


Figure 3. Transmitter and Reciever Flow Charts

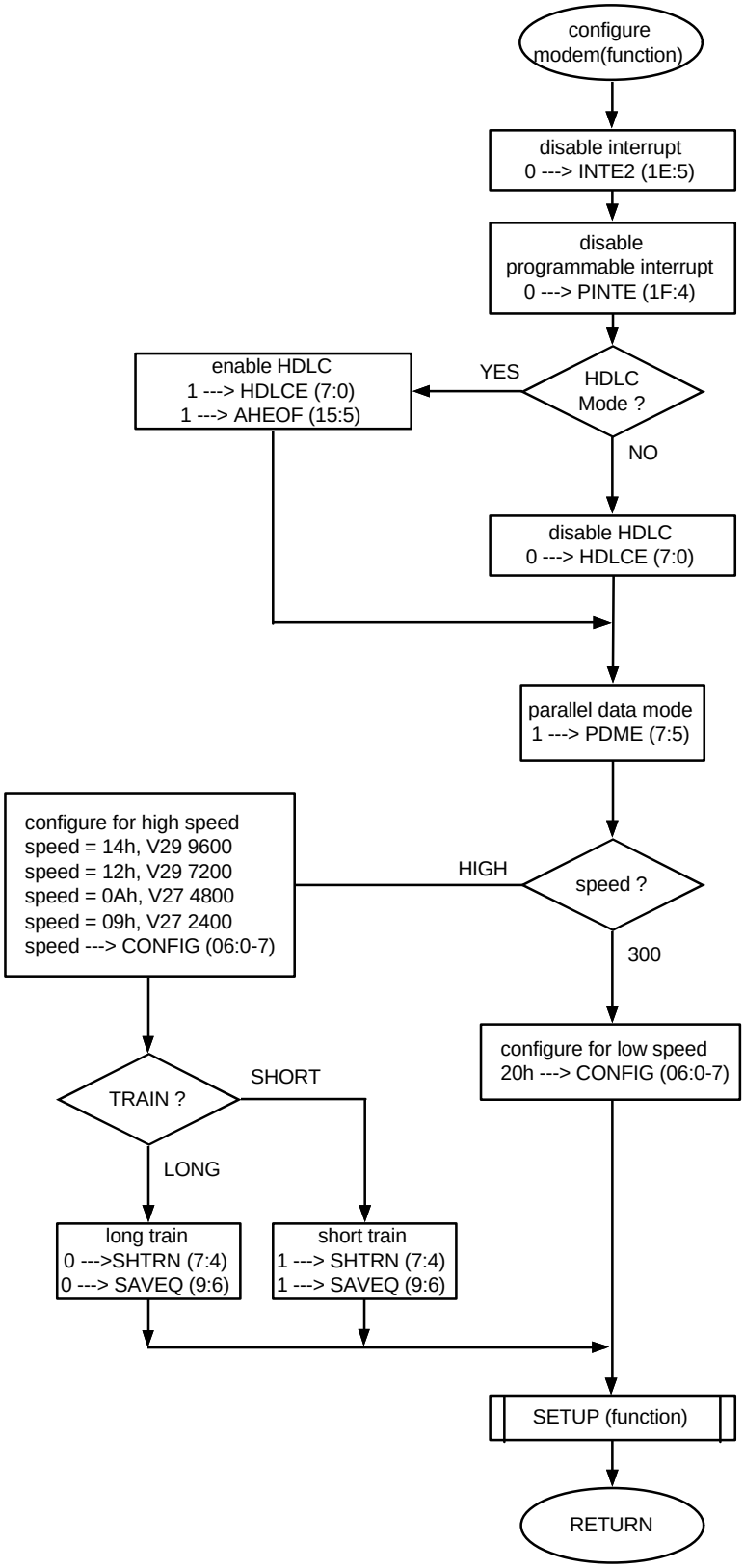
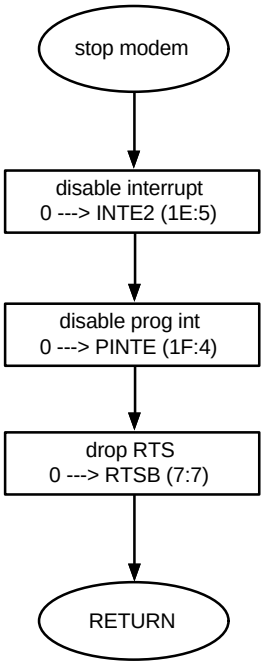
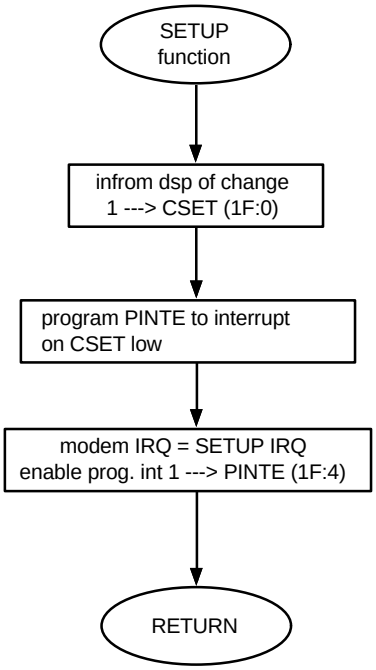
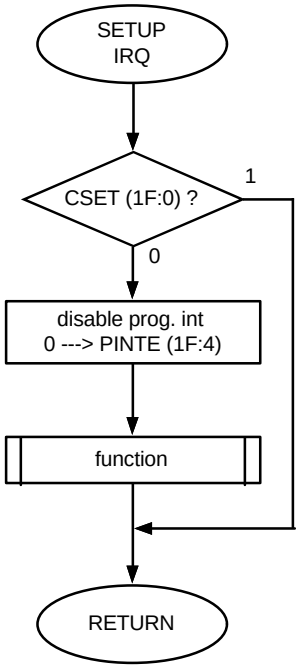


Figure 4. Modem Configuration







Modem Configuration Continued

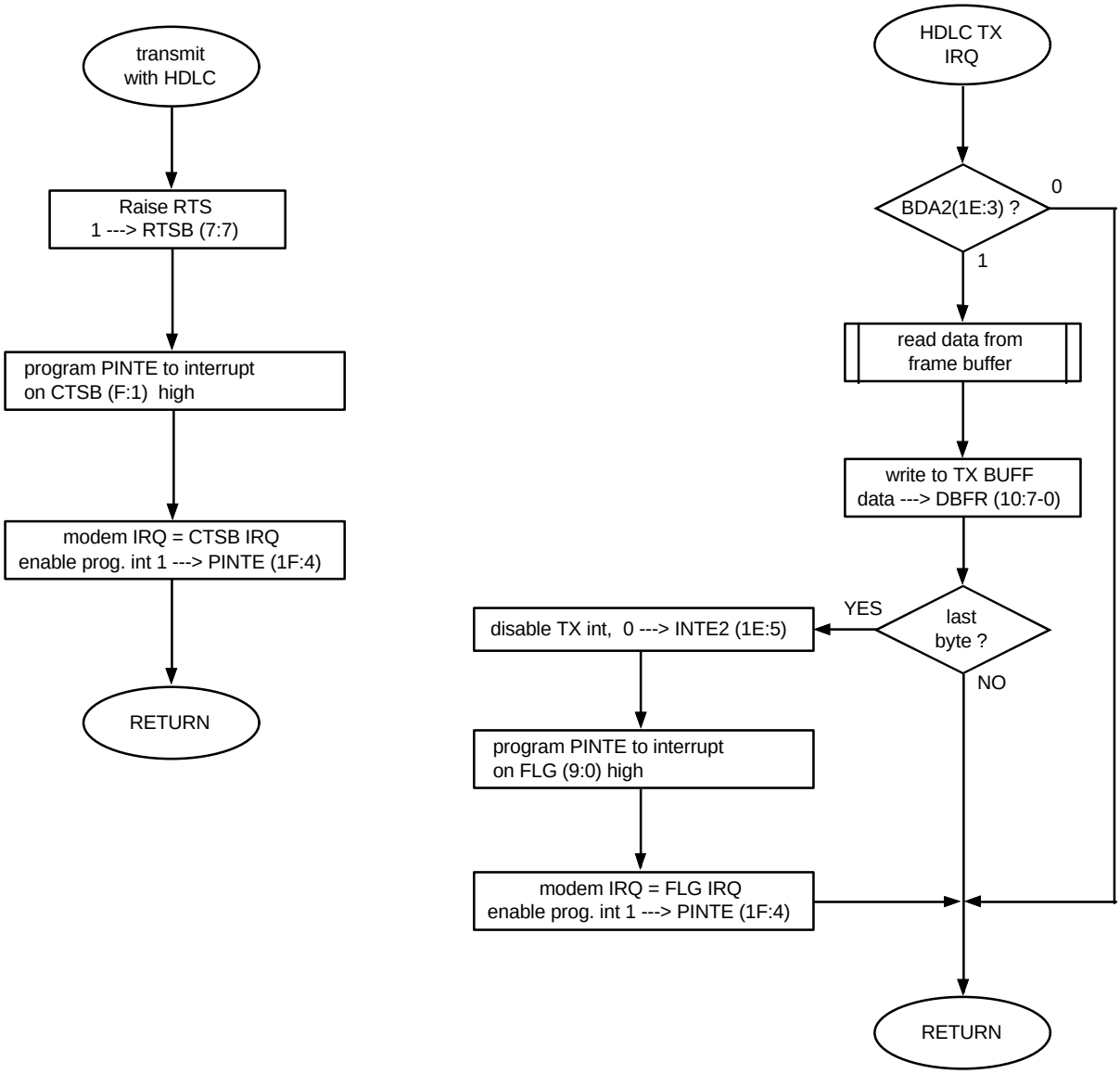
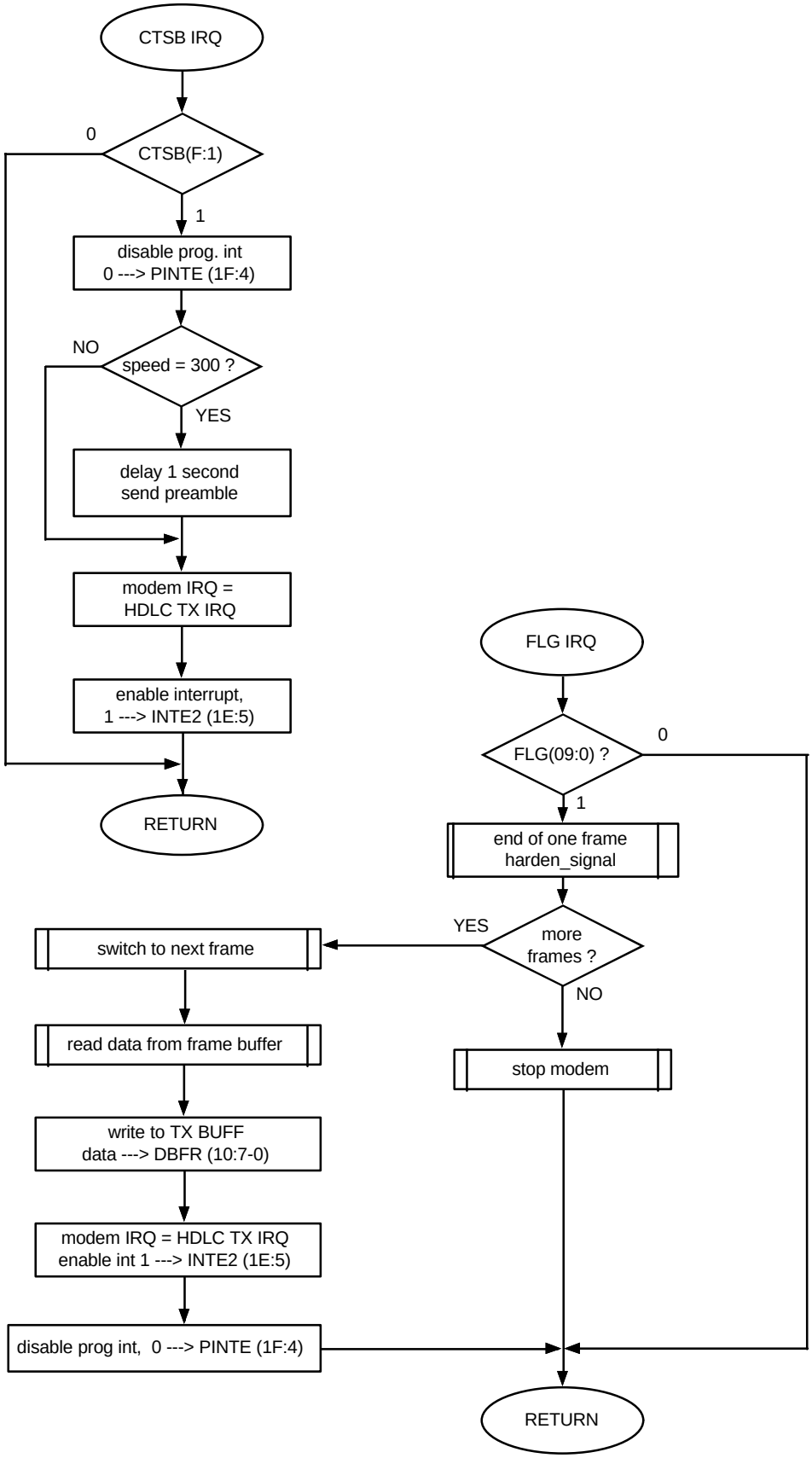
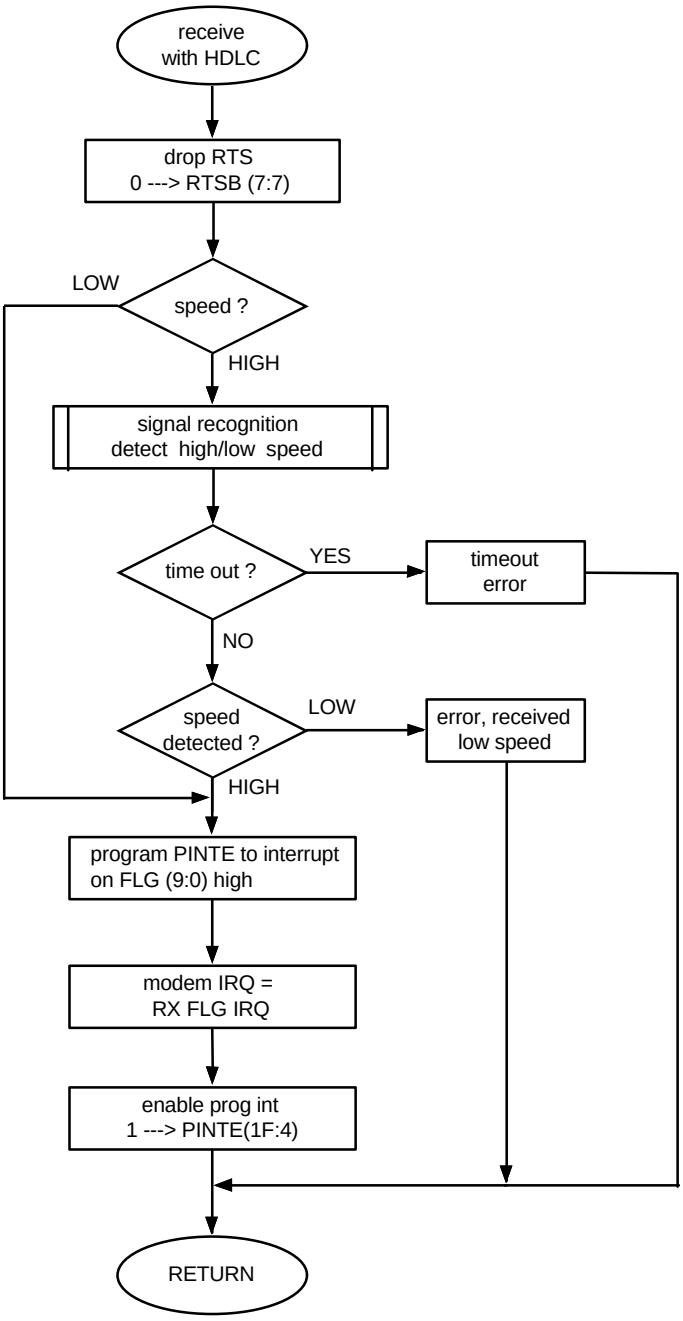
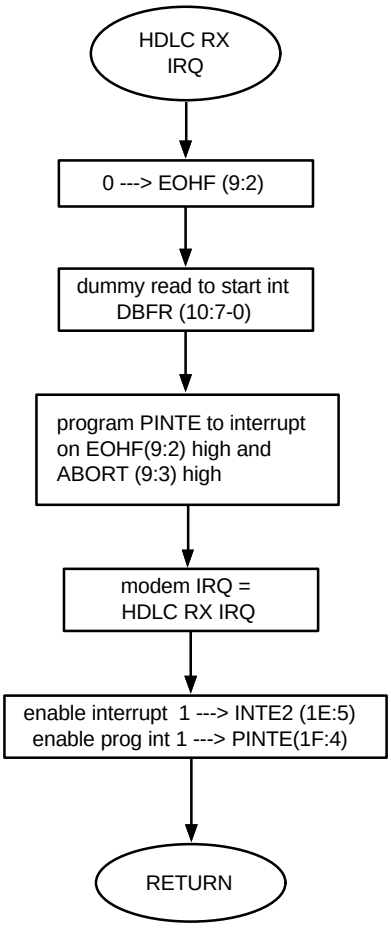


Figure 5. Transmit HDLC Frame


CTSB IRQ
CTSB(F:1)
0
1
disable prog. int
0 ---> PINTE (1F:4)
NO
speed = 300 ?
YES
delay 1 second
send preamble
modem IRQ =
HDLC TX IRQ
enable interrupt,
1 ---> INTE2 (1E:5)
RETURN
FLG IRQ
FLG(09:0) ?
0
1
end of one frame
harden_signal
YES
more
frames ?
NO
switch to next frame
read data from frame buffer
write to TX BUFF
data ---> DBFR (10:7-0)
modem IRQ = HDLC TX IRQ
enable int 1 ---> INTE2 (1E:5)
disable prog int, 0 ---> PINTE (1F:4)
stop modem
RETURN


receive
with HDLC
drop RTS
0 ---> RTSB (7:7)
LOW
speed ?
HIGH
signal recognition
detect high/low speed
time out ?
YES
timeout
error
NO
speed
detected ?
LOW
error, received
low speed
HIGH
program PINTE to interrupt
on FLG (9:0) high
modem IRQ =
RX FLG IRQ
enable prog int
1 ---> PINTE(1F:4)
RETURN


HDLC RX
IRQ
0 ---> EOHF (9:2)
dummy read to start int
DBFR (10:7-0)
program PINTE to interrupt
on EOHF(9:2) high and
ABORT (9:3) high
modem IRQ =
HDLC RX IRQ
enable interrupt 1 ---> INTE2 (1E:5)
enable prog int 1 ---> PINTE(1F:4)
RETURN

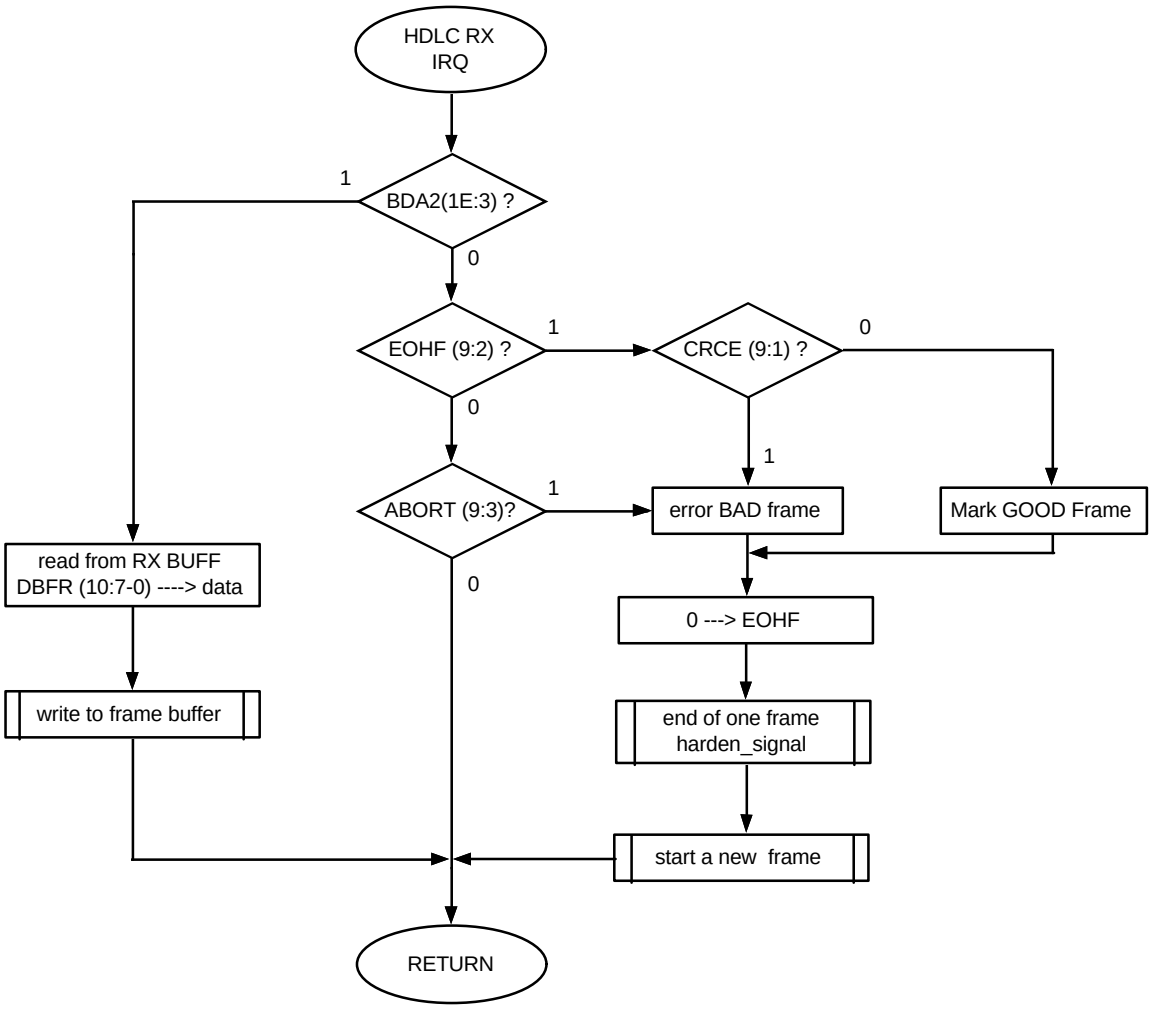


Figure 6. Receive HDLC Frame

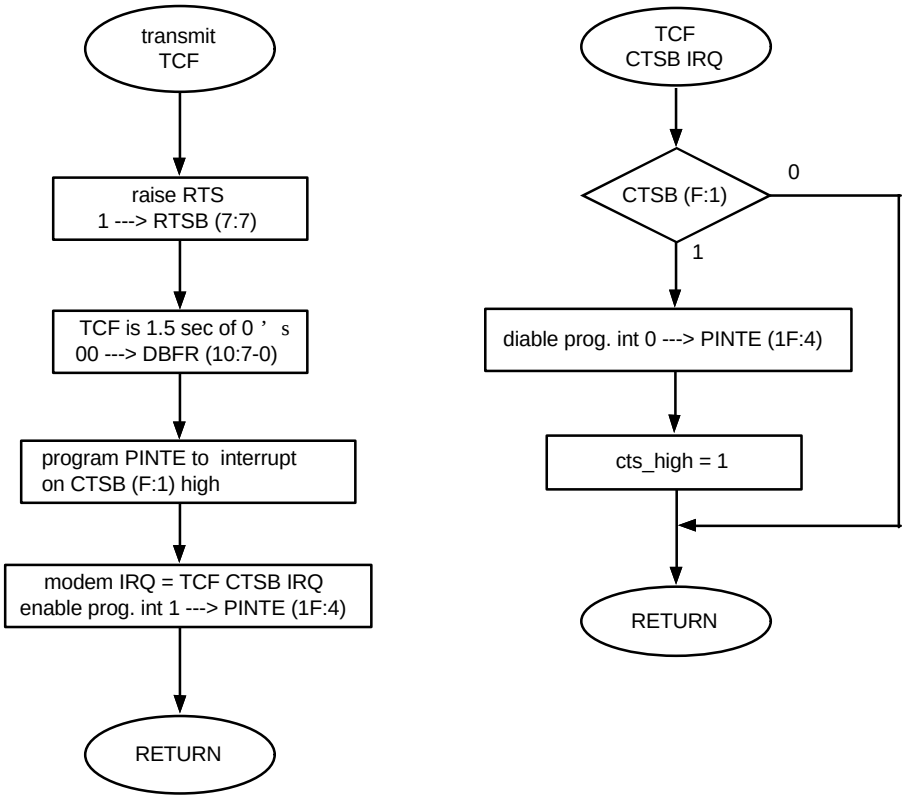


Figure 7. Transmit TCF - Training Check

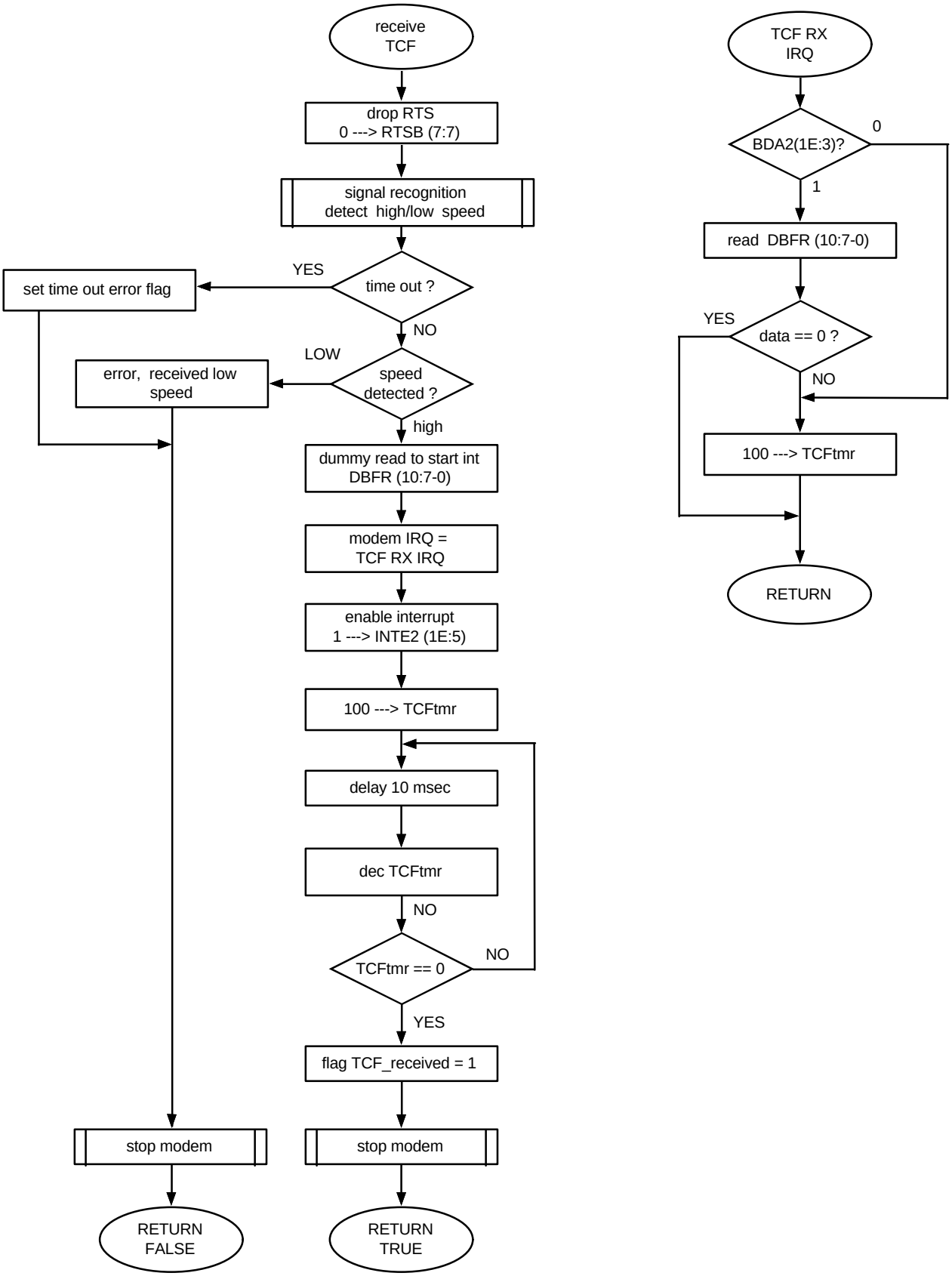


Figure 8. Receive TCF - Training Check

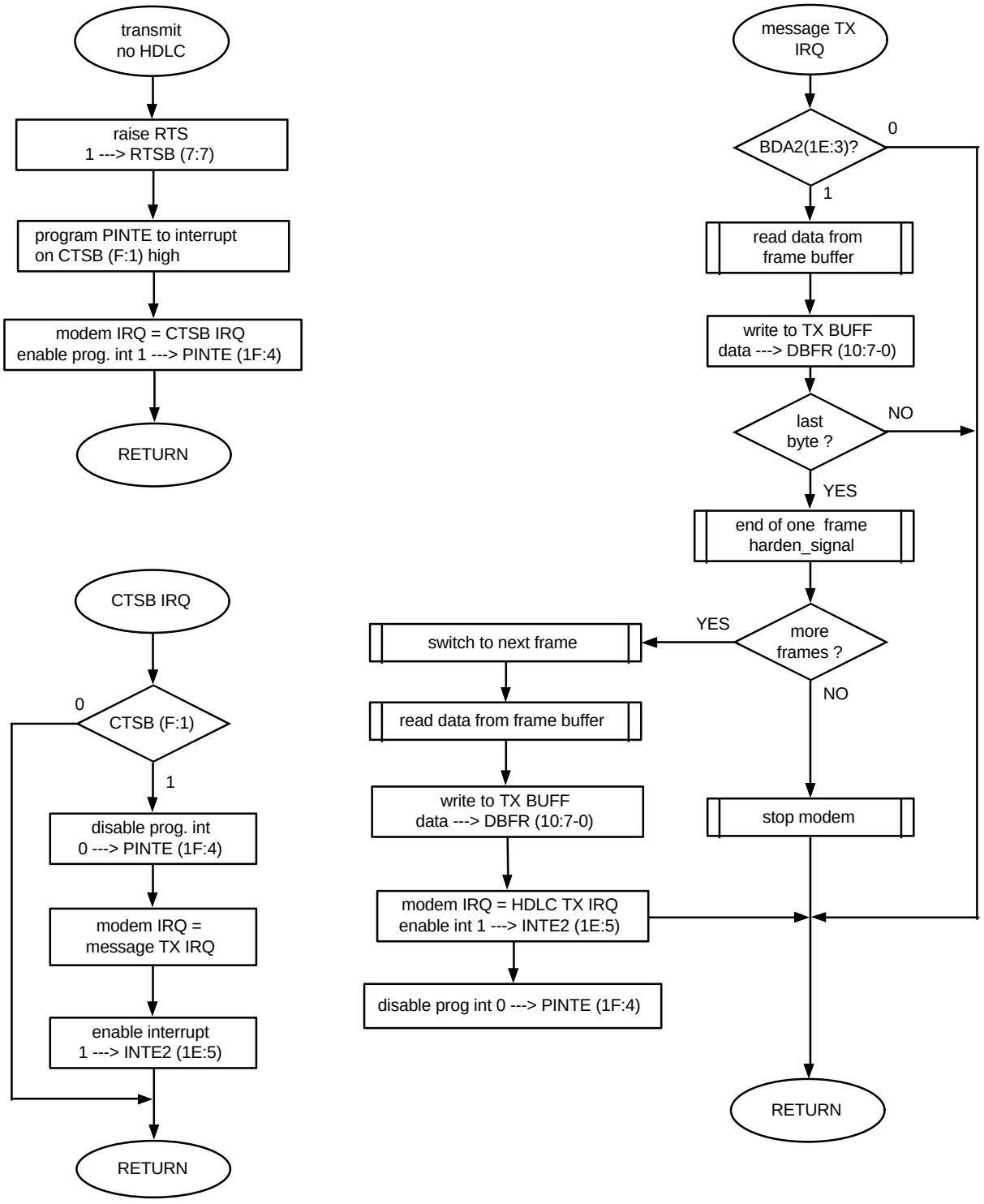


Figure 9. Transmit FAX message (NO HDLC)

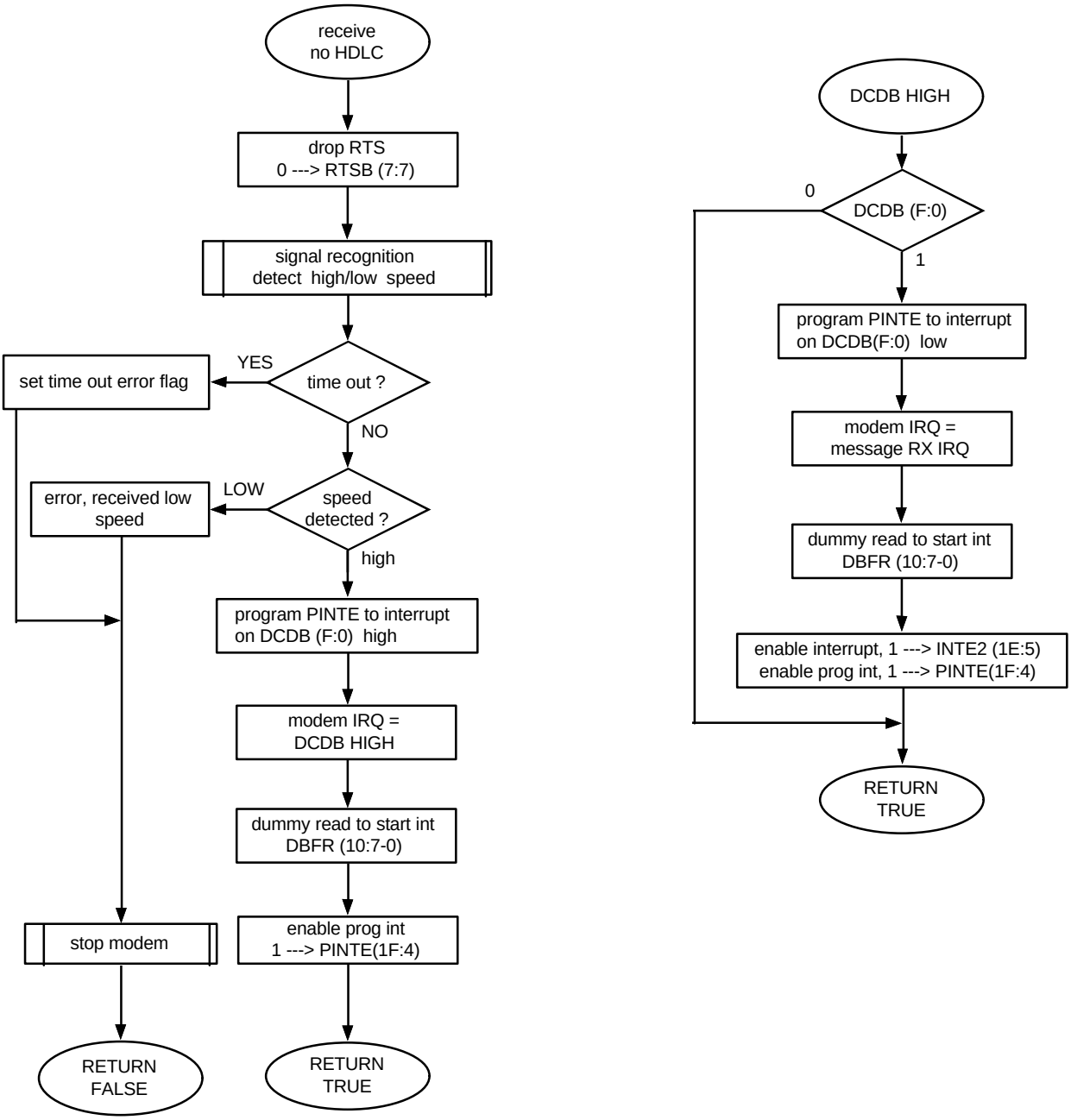


Figure 10. Receive FAX message (NO HDLC)

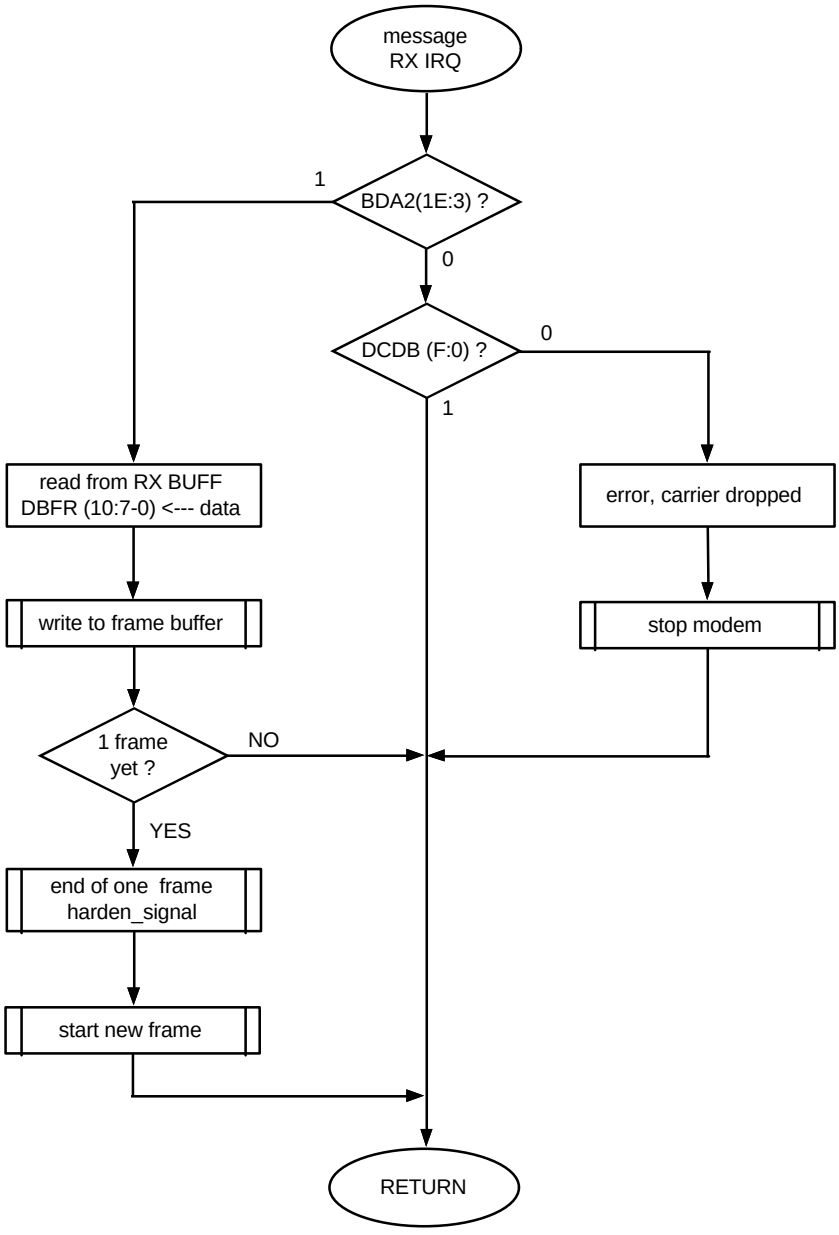

message
RX IRQ
BDA2(1E:3) ?
1
0
DCDB (F:0) ?
0
1
read from RX BUFF
DBFR (10:7-0) <--- data
error, carrier dropped
write to frame buffer
stop modem
1 frame
yet ?
NO
YES
end of one frame
harden_signal
start new frame
RETURN

Table 9. KS16112 Crystal Specifications

Parameter	Value
Nominal Frequency (25 ° C)	24.00014 MHz
Frequency Tolerance (25 ° C)	± 0.0015 %
Operating Temperature	0 ° C to 60 ° C
Storage Temperature	-55 ° C to 85 ° C
Temperature Stability (0 ° C to 60 ° C)	± 0.003 %
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF (max.)
Load Capacitance	18 ± 0.2 pF
Drive Level (at 20 nW)	2.5 mW (max.)
Aging per Year	0.0005 %
Oscillation Mode	Fundamental
Series Resistance	25 Ω (max.)
Maximum Frequency Variation (16.5pF or 19.5pF load capacitance)	± 0.0035 %

Table 10. KS16114 Fundamental Crystal Specifications

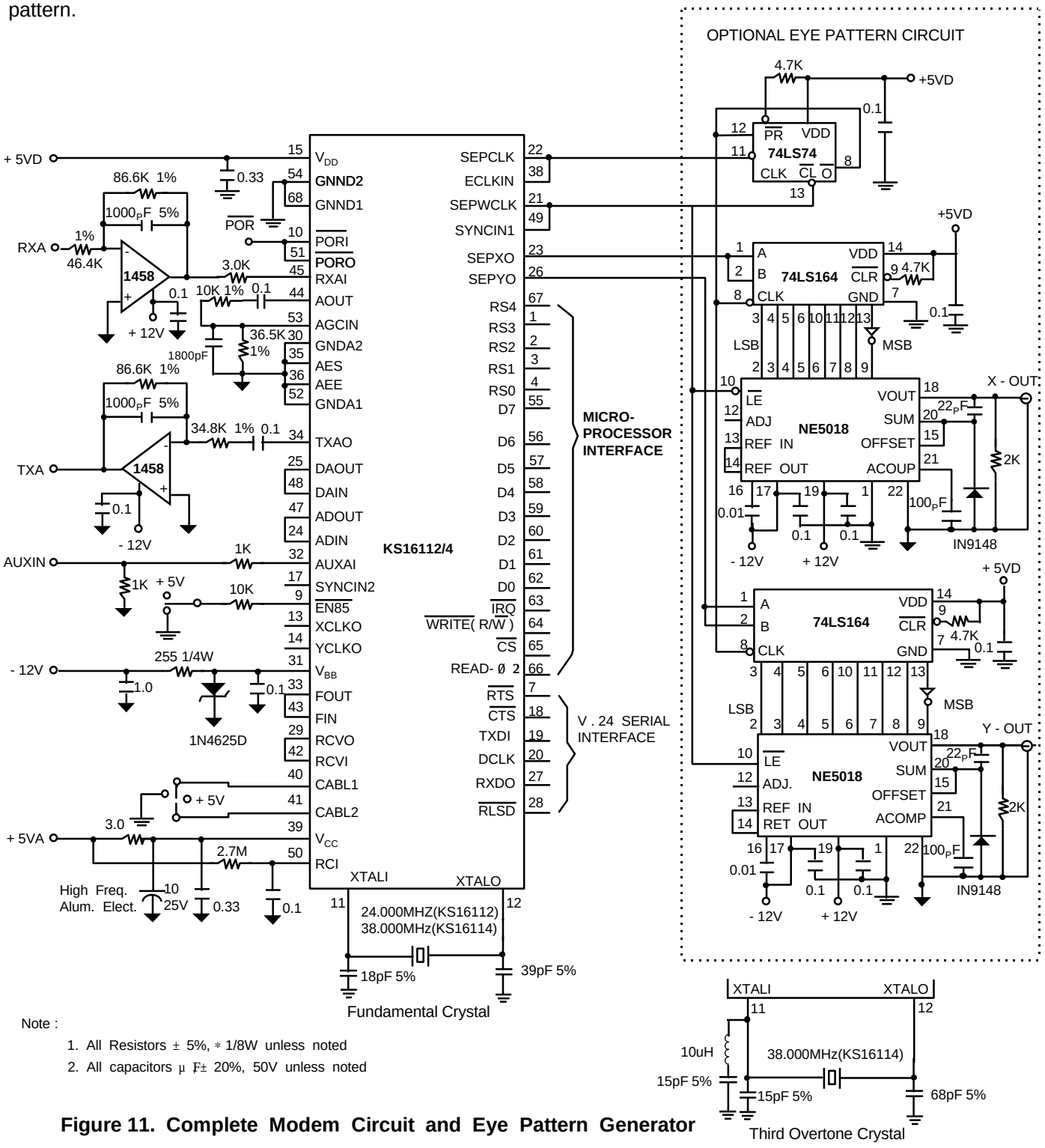
Parameter	Value
Nominal Frequency (25 ° C)	38.000530 MHz
Frequency Tolerance (25 ° C)	± 0.0015%
Operating Temperature	0 ° C to 60 ° C
Storage Temperature	-55 ° C to 85 ° C
Temperature Stability (0 ° C to 60 ° C)	± 0.003%
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF (max)
Series Capacitance: at 12.7 MHz at 38.00053 MHz	0.024 pF (typ.) 0.0022 pF (typ.)
Series Inductance : at 12.7 MHz at 38.00053 MHz	6.58 mH (typ.) 7.97 mH (typ.)
Series Resistance: at 12.7 MHz at 38.00053 MHz	150 Ω (max.) 70 Ω (max.)
Load Capacitance	18 ± 0.2 pF
Drive Level	1.0 mW (max.)
Aging Per Year	0.005% (max.)
Oscillation Mode	Fundamental
Maximum Frequency Variation (16.5 pF or 19.5 pF load Capacitance	± 0.0035%

Table 11. KS16114 Third Overtone Crystal Specifications

Parameter	Value
Normal Frequency (25 ° C)	38.000530 MHz
Frequency Tolerance (25 ° C)	± 0.0015%
Operating Temperature	0 ° C to 60 ° C
Storage Temperature	-55 ° C to 85 ° C
Temperature Stability (0 ° C to 60 ° C)	± 0.003%
Calibration Mode	Parallel Resonant
Shunt Capacitance	7 pF (max)
Series Capacitance: at 12.7 MHz at 38.00053 MHz	 0.024 pF (typ.) 0.0022 pF (typ.)
Series Inductance: at 12.7 MHz at 38.00053 MHz	 6.58 mH (typ.) 7.97 mH (typ.)
Series Resistance: at 12.7 MHz at 38.00053 MHz	 150 Ω (max.) 70 Ω (max.)
Load Capacitance	18 ± 0.2 pF
Drive Level	1.0 mW (max.)
Aging Per Year	0.0005% (max.)
Oscillation Mode	Third Overtone
Maximum Frequency Variation (16.5 pF or 19.5 pF load Capacitance)	 ± 0.0035%

MODEM CIRCUIT INTERFACE

The modem is packaged in a 68 - pin PLCC to be designed into OEM circuit boards. An example of a hardware realization is shown in Figure 11. This figure also includes the circuitry needed to display the eye pattern.

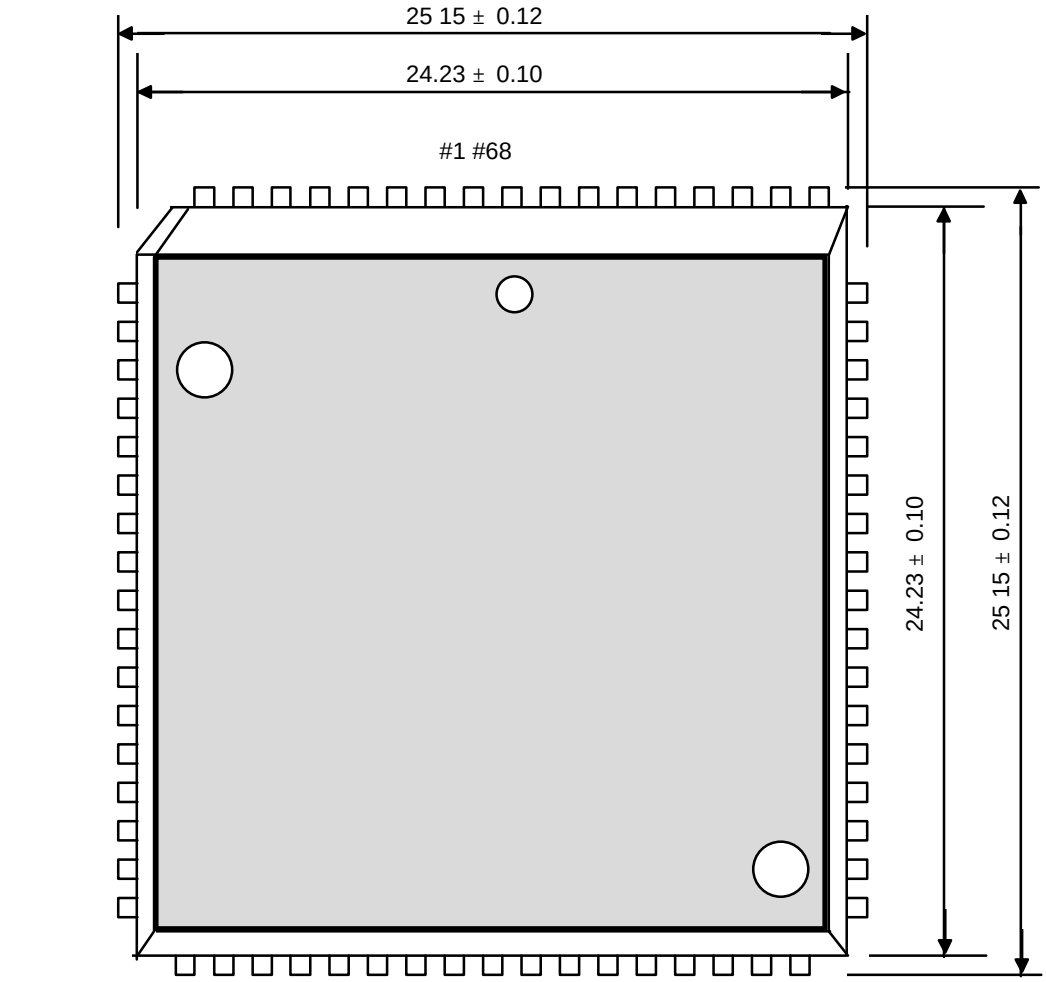


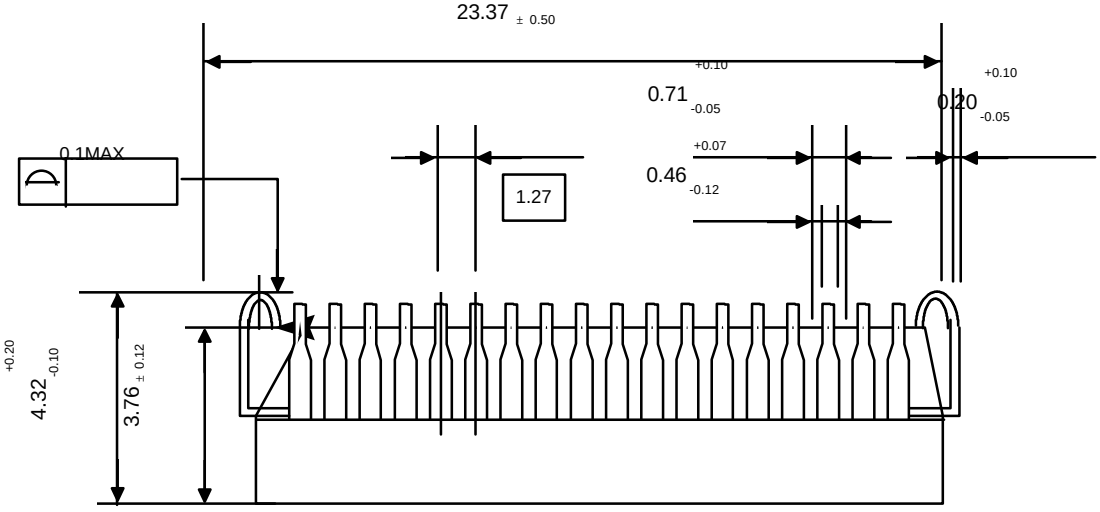
Note :

1. All Resistors ± 5%, ∗ 1/8W unless noted
2. All capacitors μ F± 20%, 50V unless noted

Figure 11. Complete Modem Circuit and Eye Pattern Generator

Package Dimension





Samsung Preliminary Fax Modem designer's guide

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