Ordering number : EN*5117

CMOS LSI

# LC6529N, LC6529F, LC6529L

## 4-Bit Microcomputer for Small-Scale Control Applications

**Preliminary**

## Overview

The LC6529N/F/L provides the basic architecture and instruction set of the Sanyo LC6500 Series of 4-bit single-chip microcomputers in a version specially for small-scale control applications involving circuits built with standard logic elements, applications using simple, comparator-based voltage or phase detectors, or other applications controlling a limited number of controls. The LC6529F is a replacement for the former LC6529H. (Certain functions differ, however.) The N (medium-speed) and L (power-saving) versions are new additions to the lineup.

## Features

- Power-saving CMOS design (Standby mode accessed with HALT instruction included.)
- Memory: 1 kilobyte of 8-bit ROM and 64 words of 4-bit RAM
- Instruction set: 51-member subset of LC6500 standard complement of 80 instructions
- (L version) Wide range of operating voltages: 2.2 to 6.0 V
- (F version) 0.92 µs/3.0 V instruction cycle time
- Flexible I/O ports
  Four ports with up to 16 lines
  - — Bidirectional I/O ports: 12
    Dedicated input ports: 4 (These double as comparator inputs.)
  - — I/O voltage limit: max. +15 V (open-drain configuration)
  - — Output current: max. 20 mA sink current (capable of directly driving an LED)

  Choice of options to match system specifications
  - — Choice of open-drain or pull-up resistor output configurations at the bit level for all ports
  - — Choice of reset output levels for Ports C and D in groups of 4 bits each
    Port E configurable as four comparator inputs
- Stack: Four levels
- Timers: 4-bit prescaler plus 8-bit programmable counter
- Comparators: 4 channels (2 reference levels)
  Separator reference level for each channel pair
  - — Feedback resistor option for choice of input with or without hysteresis
- Choice of clock oscillator options to match system specifications
  - — Oscillator circuit options: 2-pin RC oscillator circuit (N and L versions) or 2-pin ceramic oscillator circuit (N, F, and L versions)
  - — Frequency divider options: Built-in 1/3 and 1/4 frequency dividers that eliminate the need for external frequency dividers

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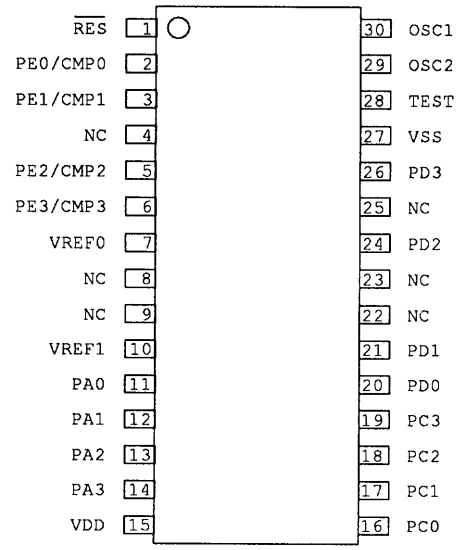
## Summary of Functions

| Item | LC6529N | LC6529F | LC6529L |
|---|---|---|---|
| [Memory] | | | |
| ROM | 1024 × 8 bits | 1024 × 8 bits | 1024 × 8 bits |
| RAM | 64 × 4 bits | 64 × 4 bits | 64 × 4 bits |
| Instruction set | 51 | 51 | 51 |
| [On-board functions] | | | |
| Timers | 4-bit prescaler plus 8-bit programmable counter | 4-bit prescaler plus 8-bit programmable counter | 4-bit prescaler plus 8-bit programmable counter |
| Stack levels | 4 | 4 | 4 |
| Standby mode | HALT instruction places chip on standby. | HALT instruction places chip on standby. | HALT instruction places chip on standby. |
| Comparators | 4 channels (2 reference levels) | 4 channels (2 reference levels) | 4 channels (2 reference levels) |
| [I/O ports] | | | |
| Number of ports | 12 bidirectional I/O pins, 4 input pins | 12 bidirectional I/O pins, 4 input pins | 12 bidirectional I/O pins, 4 input pins |
| I/O voltage limit | max. 15 V (ports A, C, and D) | max. 15 V (ports A, C, and D) | max. 15 V (ports A, C, and D) |
| Output current | 10 mA typ. 20 mA max. | 10 mA typ. 20 mA max. | 10 mA typ. 20 mA max. |
| I/O circuit configuration | Choice of open-drain output or pull-up resistors at the bit level for ports A, C, and D | | |
| Reset output level | Choice of high or low in groups of 4 bits each (ports C and D) | | |
| Port function | Port E configurable as four comparator inputs | | |
| [Characteristics] | | | |
| Minimum cycle time | 2.77 µs ($V_{DD}$ ≥ 3.0 V) | 0.92 µs ($V_{DD}$ ≥ 3.0 V) | 3.84 µs ($V_{DD}$ ≥ 2.2 V) |
| Operating temperature | –40 to +85°C | –40 to +85°C | –40 to +85°C |
| Power supply voltage | 3.0 to 6.0 V | 3.0 to 6.0 V | 2.2 to 6.0 V |
| Current drain | 1.1 mA typ. | 1.6 mA typ. | 1.0 mA typ. |
| [Clock] | | | |
| Oscillator | RC (850 kHz, 400 kHz typ.)<br>Ceramic oscillator (400 kHz, 800 kHz, 2 MHz, 4 MHz) | Ceramic oscillator (2 MHz, 4 MHz) | RC (400 kHz typ.)<br>Ceramic oscillator (400 kHz, 800 kHz, 2 MHz, 4 MHz) |
| Frequency divider options | 1/1, 1/3, 1/4 | 1/1 | 1/1, 1/3, 1/4 |
| [Miscellaneous] | | | |
| Package | DIP24S, SSOP24, MFP30S | DIP24S, SSOP24, MFP30S | DIP24S, SSOP24, MFP30S |
| OTP | Included | Included | Included |

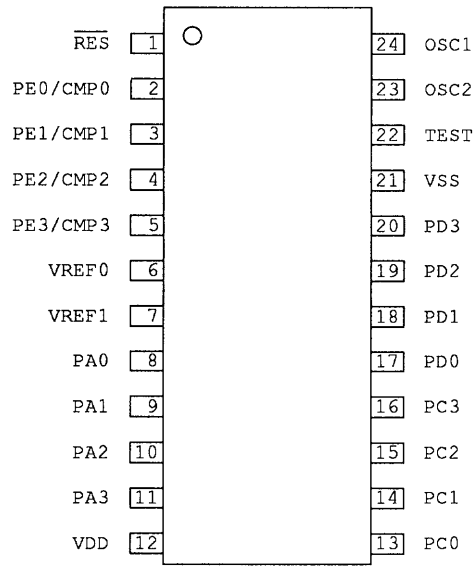
Note: The oscillator constants will be announced once the recommended circuit design has been decided.

### Pin Assignments

MFP30S




DIP24S/SSOP24



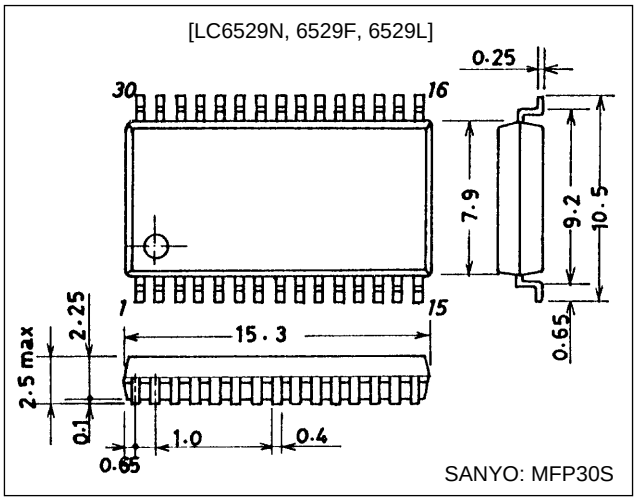

Top view

Note: Do not use dip-soldering when mounting the SSOP package on the circuit board.

## Package Dimensions

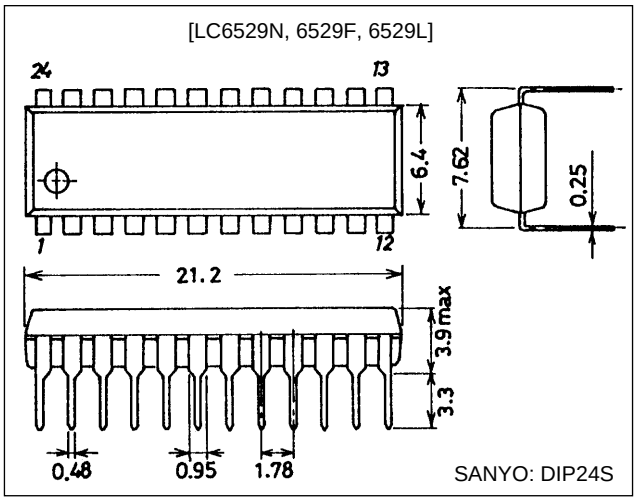
unit: mm

**3073A-MFP30S**



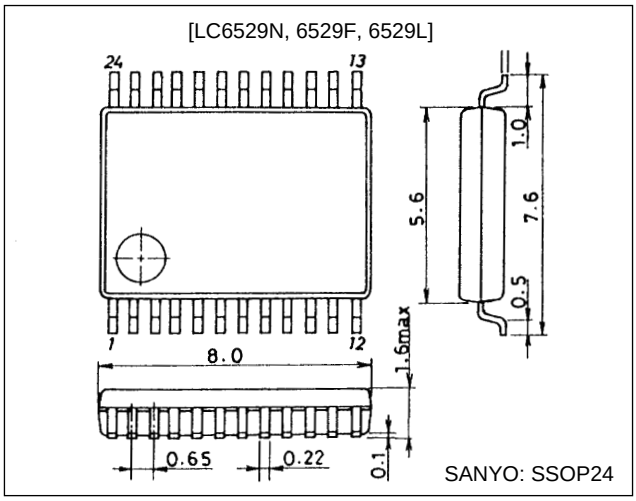

unit: mm

**3067-DIP24S**




unit: mm

**3175A-SSOP24**

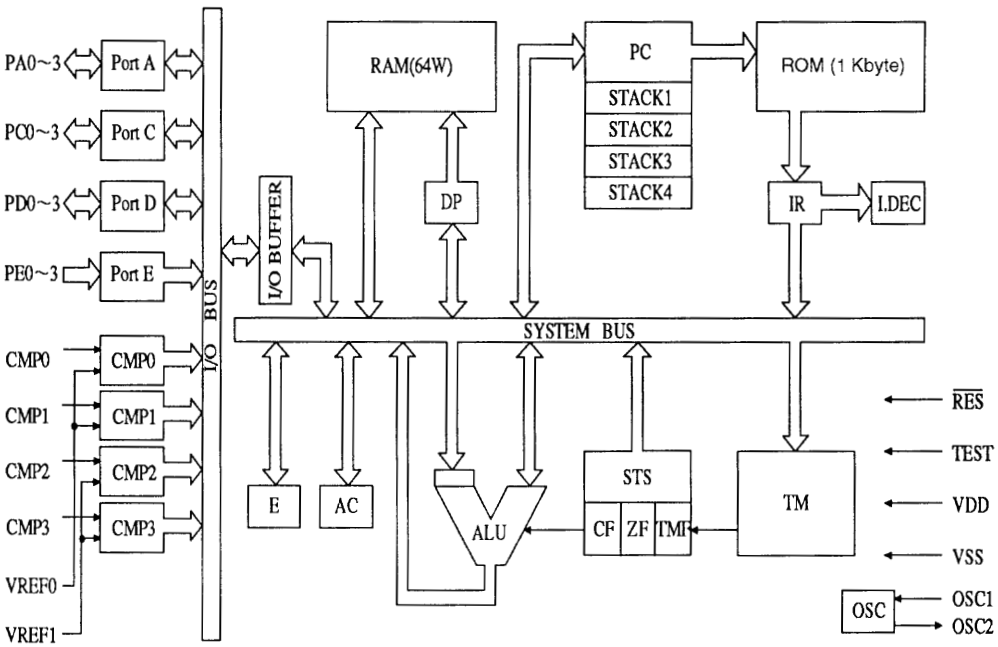



Note: The above diagrams give only the nominal dimensions. Contact Sanyo for drawings complete with tolerances.

## Pin Names

| | |
|---|---|
| OSC1, OSC2: | Pins for RC or ceramic oscillator circuit |
| TEST: | Test pin |
| RES: | Reset pin |
| PA0 to PA3: | Bidirectional I/O port A, bits 0 to 3 |
| PC0 to PC3: | Bidirectional I/O port C, bits 0 to 3 |
| PD0 to PD3: | Bidirectional I/O port D, bits 0 to 3 |
| PE0 to PE3: | Unidirectional input port E, bits 0 to 3 |
| CMP0 to CMP3: | Comparator input port, bits 0 to 3 |
| VREF0, VREF1: | Reference inputs |

## System Block Diagram

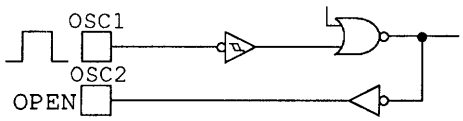
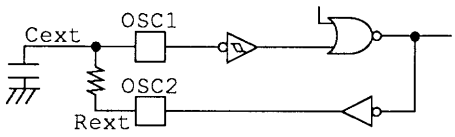
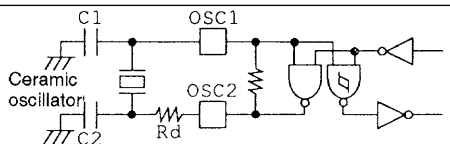



| | | | |
|---|---|---|---|
| RAM: | Data memory | ROM: | Program memory |
| AC: | Accumulator | PC: | Program Counter |
| ALU: | Arithmetic and Logic Unit | IR: | Instruction Register |
| DP: | Data pointer | I.DEC: | Instruction Decoder |
| E: | E register | CF: | Carry Flag |
| OSC: | Oscillator circuit | ZF: | Zero Flag |
| TM: | Timer | TMF: | Timer overflow Flag |
| STS: | Status register | | |

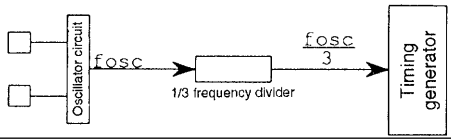
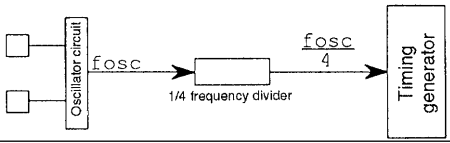
## Pin Functions

| Pin No. | Symbol | I/O | Function | Output driver type | Options | State after reset |
|---|---|---|---|---|---|---|
| 1 | $V_{DD}$ | — | Power supply. Normally +5 V. | | — | — |
| 1 | $V_{SS}$ | — | Power supply. 0 V. | | — | — |
| 1<br>1 | OSC1<br>OSC2 | I<br>O | Pins for attaching external system clock oscillator circuit (RC or ceramic) | | 1. 2-pin RC oscillator circuit (1-pin external clock)<br>2. 2-pin ceramic oscillator circuit<br>3. Frequency divider options: 1/1, 1/3, 1/4 | |
| 4 | PA0<br>PA1<br>PA2<br>PA3 | I/O | • Bidirectional I/O port A0 to A3: 4-bit input (IP instruction), 4-bit output (OP instruction), 1-bit conditionals (BP and BNP instructions), 1-bit set and reset (SPB and RPB instructions)<br>• PA3 also doubles as standby operation control.<br>• Block chattering from entering PA3 during the HALT instruction execution cycle. | • N channel: sink current type<br>• I/O voltage limit for open-drain configuration: max. +15 V<br>• P channel: high-impedance pull-up type | 1. Open-drain output<br>2. Pull-up resistor<br>• Choice of configuration 1. or 2. at bit level | High output (output N channel transistor off) |
| 4 | PC0<br>PC1<br>PC2<br>PC3 | I/O | • Bidirectional I/O port C0 to C3. Functions the same as PA0 to PA3 except that there is no the standby operation control.<br>• Option controls whether output is high or low after reset. | • N channel: sink current type<br>• I/O voltage limit for open-drain configuration: max. +15 V<br>• P channel: low-impedance pull-up type | 1. Open-drain output<br>2. Pull-up resistor<br>3. High output after reset<br>4. Low output after reset<br>• Choice of configuration 1. or 2. at bit level<br>• Choice of configuration 3. or 4. at port (4-bit) level | High or low (option) |
| 4 | PD0<br>PD1<br>PD2<br>PD3 | I/O | Bidirectional I/O port D0 to D3. Functions and options the same as PC0 to PC3. | • N channel: sink current type<br>• I/O voltage limit for open-drain configuration: max. +15 V<br>• P channel: high-impedance pull-up type | 1. Open-drain output<br>2. Pull-up resistor<br>3. High output after reset<br>4. Low output after reset<br>• Choice of configuration 1. or 2. at bit level<br>• Choice of configuration 3. or 4. at port (4-bit) level | High or low (option) |
| 4<br><br><br><br>4 | PE0/CMP0<br>PE1/CMP1<br>PE2/CMP2<br>PE3/CMP3 | I<br><br><br><br>I | • When configured for comparator input: CMP0 and CMP1 use reference voltage $V_{REF}0$; CMP2 and CMP3 use reference voltage $V_{REF}1$.<br>• 4-bit (CMP0 to 3) input (IP instruction)<br>• 1-bit conditionals (BP and BNP instructions)<br>• When configured for port E input:<br>• 4-bit (E0-3) input (IP instruction)<br>• 1-bit conditionals (BP and BNP instructions) | | 1. Comparator input<br>2. Port E input<br>3. Without feedback resistor<br>4. With feedback resistor<br>• Choice of configuration 1. or 2. at port (4-bit) level<br>• Options 3. and 4. only available with 1. | |
| 2 | $V_{REF}0$<br>$V_{REF}1$ | I | • Comparator reference level inputs: CMP0 and CMP1 use reference voltage $V_{REF}0$; CMP2 and CMP3 use reference voltage $V_{REF}1$.<br>• Connect to $V_{SS}$ when PE0/CMP0 to PE3/CMP3 configured as port E. | | | |
| 1 | $\overline{RES}$ | I | • System reset input<br>• Connect external capacitor for power up reset.<br>• Low level input for a minimum of four clock cycles triggers a reset. | | | |
| 1 | TEST | I | Chip test pin. Normally connect to $V_{SS}$. | | | |

## Oscillator Circuit Options

| Name | Circuit diagram | Conditions, etc. |
|---|---|---|
| External clock |  | Leave OSC2 open. |
| 2-pin RC oscillator circuit |  | |
| 2-pin ceramic oscillator circuit |  | |

## Frequency Divider Options

| Name | Circuit diagram | Conditions, etc. |
|---|---|---|
| No frequency divider (1/1) |  | Available with all three oscillator circuit options (N, F, and L versions) |
| 1/3 frequency divider |  | Available only with external clock and ceramic oscillator circuit options (N and L versions) |
| 1/4 frequency divider |  | Available only with external clock and ceramic oscillator circuit options (N and L versions) |

## Frequency Divider Options
## LC6529N

| Oscillator circuit | Frequency | Frequency divider options (cycle time) | $V_{DD}$ range | Note |
|---|---|---|---|---|
| Ceramic oscillator | 400 kHz | 1/1 (10 µs) | 3 to 6 V | 1/3 and 1/4 frequency divider options not available |
| | 800 kHz | 1/1 (5 µs)<br>1/3 (15 µs)<br>1/4 (20 µs) | 3 to 6 V<br>3 to 6 V<br>3 to 6 V | |
| | 2 MHz | 1/3 (6 µs)<br>1/4 (8 µs) | 3 to 6 V<br>3 to 6 V | 1/1 frequency divider option not available |
| | 4 MHz | 1/3 (3 µs)<br>1/4 (4 µs) | 3 to 6 V<br>3 to 6 V | 1/1 frequency divider option not available |
| External clock based on RC oscillator circuit | 200 k to 1444 kHz<br>600 k to 4330 kHz<br>800 k to 4330 kHz | 1/1 (20 to 2.77 µs)<br>1/3 (20 to 2.77 µs)<br>1/4 (20 to 3.70 µs) | 3 to 6 V<br>3 to 6 V<br>3 to 6 V | |
| RC oscillator circuit | Use 1/1 frequency divider and recommended constants or, if this is not possible, one of the frequency, frequency divider option, and $V_{DD}$ range combinations listed for external clocks based on an RC oscillator circuit. | | 3 to 6 V | |
| External clock based on ceramic oscillator circuit | This configuration not allowed. Use an external clock based on an RC oscillator circuit instead. | | | |

### LC6529F

| Oscillator circuit | Frequency | Frequency divider options (cycle time) | $V_{DD}$ range | Note |
|---|---|---|---|---|
| Ceramic oscillator | 4 MHz | 1/1 (1 µs) | 3 to 6 V | |
| External clock based on RC oscillator circuit | 200 k to 4330 kHz | 1/1 (20 to 0.92 µs) | 3 to 6 V | |
| External clock based on ceramic oscillator circuit | This configuration not allowed. Use an external clock based on an RC oscillator circuit instead. | | | |

### LC6529L

| Oscillator circuit | Frequency | Frequency divider options (cycle time) | $V_{DD}$ range | Note |
|---|---|---|---|---|
| Ceramic oscillator | 400 kHz | 1/1 (10 µs) | 2.2 to 6 V | 1/3 and 1/4 frequency divider options not available |
| | 800 kHz | 1/1 (5 µs)<br>1/3 (15 µs)<br>1/4 (20 µs) | 2.2 to 6 V<br>2.2 to 6 V<br>2.2 to 6 V | |
| | 2 MHz | 1/3 (6 µs)<br>1/4 (8 µs) | 2.2 to 6 V<br>2.2 to 6 V | 1/1 frequency divider option not available |
| | 4 MHz | 1/4 (4 µs) | 2.2 to 6 V | 1/1 and 1/3 frequency divider options not available |
| External clock based on RC oscillator circuit | 200 k to 1040 kHz<br>600 k to 3120 kHz<br>800 k to 4160 kHz | 1/1 (20 to 3.84 µs)<br>1/3 (20 to 3.84 µs)<br>1/4 (20 to 3.84 µs) | 2.2 to 6 V<br>2.2 to 6 V<br>2.2 to 6 V | |
| RC oscillator circuit | Use 1/1 frequency divider and recommended constants or, if this is not possible, one of the frequency, frequency divider option, and $V_{DD}$ range combinations listed for external clocks based on an RC oscillator circuit. | | 2.2 to 6 V | |
| External clock based on ceramic oscillator circuit | This configuration not allowed. Use an external clock based on an RC oscillator circuit instead. | | | |

### Reset Level Options for Ports C and D

The following two options are available for controlling the output levels of ports C and D in groups of four bits each.

| Option | Conditions, etc. |
|---|---|
| High level output after reset | Selection affects all bits of port |
| Low level output after reset | Selection affects all bits of port |

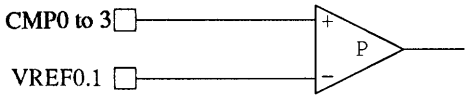
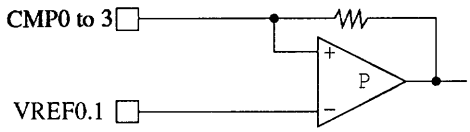
### Comparator vs. Port E Configuration Option

The four pins PE0/CMP0 to PE3/CMP3 may be configured for comparator input or as port E.

| Option | Conditions, etc. |
|---|---|
| Comparator input | Selection affects all bits of port |
| Port E input | Selection affects all bits of port |

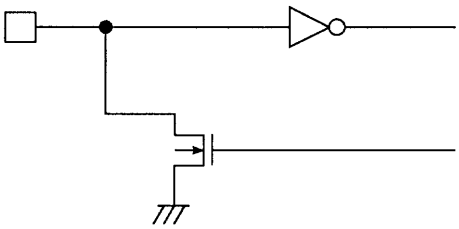
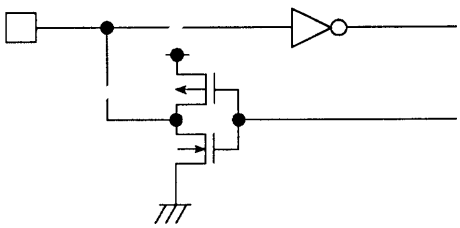
## Comparator Options

The comparators offer the following two configuration options.

| Name | Circuit diagram | Conditions, etc. |
|---|---|---|
| Without feedback resistor |  | The comparator does not use hysteresis. |
| With feedback resistor |  | The comparator, in combination with an external resistor, uses hysteresis. |

## Port Output Configurations

The bidirectional I/O ports A, C, and D offer a choice of two output configurations.

| Name | Circuit diagram | Conditions, etc. |
|---|---|---|
| Open drain (OD) |  | |
| With pull-up resistors (PU) |  | This option adds a high-impedance pull-up resistor for port A or D and a low-impedance one for port C. |

# Specifications

## LC6529N

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | –0.3 | | +7.0 | V |
| Input voltage | $V_I1$ | OSC1*1 | –0.3 | | $V_{DD}$ + 0.3 | V |
| | $V_I2$ | TEST, $\overline{RES}$ | –0.3 | | $V_{DD}$ + 0.3 | |
| | $V_I3$ | Port E (PE) configuration | –0.3 | | $V_{DD}$ + 0.3 | |
| Output voltage | $V_O$ | OSC2 | Voltages up to that generated allowed. | | | V |
| I/O voltages | $V_{IO}1$ | Open-drain (OD) configuration | –0.3 | | +15 | V |
| | $V_{IO}2$ | Pull-up (PU) resistor configuration | –0.3 | | $V_{DD}$ + 0.3 | |
| Peak output current | $I_{OP}$ | PA, PC, PD | –2 | | +20 | mA |
| Average output current | $I_{OA}$ | PA, PC, PD: Average for pin over 100-ms interval | –2 | | +20 | mA |
| | $\Sigma I_{OA}1$ | PA: Total current for pins PA0 to PA3*2 | –6 | | +40 | |
| | $\Sigma I_{OA}2$ | PC, PD: Total current for pins PC0 to PC3 and PD0 to PD3*2 | –14 | | +90 | |
| Allowable power dissipation | Pd max1 | Ta = –40 to +85°C (DIP24S) | | | 360 | mW |
| | Pd max2 | Ta = –40 to +85°C (SSOP24) | | | 165 | |
| | Pd max3 | Ta = –40 to +85°C (MFP30S) | | | 150 | |
| Operating temperature | Topr | | –40 | | +85 | °C |
| Storage temperature | Tstg | | –55 | | +125 | |

Note: 1. When the oscillator circuit in Figure 3 and the guaranteed constant are used, this is guaranteed over the full amplitude.
2. Averaged over 100-ms interval.

### Allowable Operating Ranges at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 3.0 | | 6.0 | V |
| Standby voltage | $V_{ST}$ | $V_{DD}$: Preserves contents of RAM and registers*. | 1.8 | | 6.0 | V |
| Input high level voltage | $V_{IH}1$ | Open-drain (OD) configuration: With output N-channel transistor off | 0.7 $V_{DD}$ | | 13.5 | V |
| | $V_{IH}2$ | Pull-up (PU) resistor configuration: With output N-channel transistor off | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}3$ | PE: Using port E configuration | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}4$ | $\overline{RES}$: $V_{DD}$ = 1.8 to 6 V | 0.8 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}5$ | OSC1: Using external clock option | 0.8 $V_{DD}$ | | $V_{DD}$ | |
| Input low level voltage | $V_{IL}1$ | PA, PC, PD: With output N-channel transistor off, $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.3 $V_{DD}$ | V |
| | $V_{IL}2$ | PA, PC, PD: With output N-channel transistor off | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}3$ | PE: Using port E configuration, $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.3 $V_{DD}$ | |
| | $V_{IL}4$ | PE: Using port E configuration | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}5$ | OSC1: Using external clock option, $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}6$ | OSC1: Using external clock option | $V_{SS}$ | | 0.2 $V_{DD}$ | |
| | $V_{IL}7$ | TEST: $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.3 $V_{DD}$ | |
| | $V_{IL}8$ | TEST | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}9$ | $\overline{RES}$: $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}10$ | $\overline{RES}$ | $V_{SS}$ | | 0.2 $V_{DD}$ | |
| Operating frequency (cycle time) | fop (Tcyc) | Using the built-in 1/3 or 1/4 frequency dividers extends the maximum to 4.33 MHz. | 200 (20) | | 1444 (2.77) | kHz (µs) |

Note: * Maintain the power supply voltage at $V_{DD}$ until the HALT instruction has completed execution, placing the chip in the standby mode. Block chattering from entering PA3 during the HALT instruction execution cycle.

Continued on next page.

Continued from preceding page.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| [External clock conditions] | | | | | | |
| Frequency | text | OSC1: If the clock frequency exceeds 1.444 MHz, use the built-in 1/3 or 1/4 frequency divider. Figure 1 | 200 | | 4330 | kHz |
| Pulse width | textH, textL | | 69 | | | ns |
| Rise/fall times | textR, textF | | | | 50 | |
| [Oscillator guaranteed constants] | | | | | | |
| 2-pin RC oscillator circuit | Cext | OSC1, OSC2: $V_{DD}$ = 4 to 6 V, Figure 2 | | 220 ± 5% | | pF |
| | Cext | OSC1, OSC2: Figure 2 | | 220 ± 5% | | |
| | Rext | OSC1, OSC2: $V_{DD}$ = 4 to 6 V, Figure 2 | | 4.7 ± 1% | | kΩ |
| | Rext | OSC1, OSC2: Figure 2 | | 12.0 ± 1% | | |
| Ceramic oscillator | | Figure 3 | | See Table 1. | | |

## Electrical Characteristics at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high level current | $I_{IH}1$ | Open-drain (OD) configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN}$ = 13.5 V | | | 5.0 | µA |
| | $I_{IH}2$ | PE: Using port E configuration, $V_{IN} = V_{DD}$ | | | 1.0 | |
| | $I_{IH}3$ | OSC1: Using external clock option, $V_{IN} = V_{DD}$ | | | 1.0 | |
| Input low level current | $I_{IL}1$ | Open-drain (OD) configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –1.0 | | | µA |
| | $I_{IL}2$ | Pull-up (PU) resistor configuration for port A or D: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –220 | –71.5 | | |
| | $I_{IL}3$ | Pull-up (PU) resistor configuration for port C: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –6.00 | –2.17 | | mA |
| | $I_{IL}4$ | PE: Using port E configuration, $V_{IN} = V_{SS}$ | –1.0 | | | µA |
| | $I_{IL}5$ | $\overline{RES}$: $V_{IN} = V_{SS}$ | –45 | –10 | | |
| | $I_{IL}6$ | OSC1: Using external clock option, $V_{IN} = V_{SS}$ | –1.0 | | | |
| Output high level voltage | $V_{OH}1$ | Pull-up (PU) resistor configuration for port C: $I_{OH}$ = –300 µA, $V_{DD}$ = 4 to 6 V | $V_{DD}$ – 1.2 | | | V |
| | $V_{OH}2$ | Pull-up (PU) resistor configuration for port C: $I_{OH}$ = –60 µA | $V_{DD}$ – 0.5 | | | |
| Output low level voltage | $V_{OL}1$ | PA, PC, PD: $I_{OL}$ = 10 mA, $V_{DD}$ = 4 to 6 V | | | 1.5 | V |
| | $V_{OL}2$ | PA, PC, PD: With $I_{OL}$ for each port less than or equal to 1 mA, $I_{OL}$ = 1.8 mA | | | 0.4 | |
| Hysteresis voltage | $V_{HIS}1$ | $\overline{RES}$ | | 0.1 $V_{DD}$ | | V |
| | $V_{HIS}2$ | OSC1*: Using RC oscillator or external clock option | | 0.1 $V_{DD}$ | | |

Note: * The RC oscillator and external clock options require a Schmidt trigger configuration for OSC1.

| Parameter | | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| [Current drain] | | | | | | | |
| | RC oscillator | $I_{DD\ OP}1$ | $V_{DD}$: Figure 2, 850 kHz (typ) | | 0.8 | 2.0 | mA |
| | | $I_{DD\ OP}2$ | $V_{DD}$: Figure 2, 400 kHz (typ) | | 0.4 | 1.0 | |
| | Ceramic oscillator | $I_{DD\ OP}3$ | $V_{DD}$: Figure 3, 4 MHz, 1/3 frequency divider | | 1.6 | 4.0 | mA |
| | | $I_{DD\ OP}4$ | $V_{DD}$: Figure 3, 4 MHz, 1/4 frequency divider | | 1.6 | 4.0 | |
| | | $I_{DD\ OP}5$ | $V_{DD}$: Figure 3, 2 MHz, 1/3 frequency divider | | 1.3 | 3.0 | |
| | | $I_{DD\ OP}6$ | $V_{DD}$: Figure 3, 2 MHz, 1/4 frequency divider | | 1.3 | 3.0 | |
| | | $I_{DD\ OP}7$ | $V_{DD}$: Figure 3, 800 kHz | | 1.1 | 2.6 | |
| | | $I_{DD\ OP}8$ | $V_{DD}$: Figure 3, 400 kHz | | 0.9 | 2.4 | |
| | External clock | $I_{DD\ OP}9$ | $V_{DD}$: 200 to 667 kHz, 1/1 frequency divider, 600 to 2000 kHz, 1/3 frequency divider, 800 to 2667 kHz, 1/4 frequency divider | | 1.0 | 2.5 | mA |
| | | $I_{DD\ OP}10$ | $V_{DD}$: 200 to 1444 kHz, 1/1 frequency divider, 600 to 4330 kHz, 1/3 frequency divider, 800 to 4330 kHz, 1/4 frequency divider | | 1.6 | 4.2 | |
| | Standby operation | $I_{DD}$ st1 | $V_{DD}$: With output N-channel transistor off and port level = $V_{DD}$, $V_{DD}$ = 6 V | | 0.05 | 10 | µA |
| | | $I_{DD}$ st2 | $V_{DD}$: With output N-channel transistor off and port level = $V_{DD}$, $V_{DD}$ = 3 V | | 0.025 | 5 | |
| [Oscillator characteristics] (RC oscillator) | | | | | | | |
| | Oscillator frequency | $f_{MOSC}$ | OSC1, OSC2: Figure 2, Cext = 220 pF ± 5%, Rext = 12.0 kΩ ± 1% | 309 | 400 | 577 | kHz |
| | | | OSC1, OSC2: Figure 2, Cext = 220 pF ± 5%, Rext = 4.7 kΩ ± 1%, $V_{DD}$ = 4 to 6 V | 660 | 850 | 1229 | |
| [Oscillator characteristics] (Ceramic oscillator) | | | | | | | |
| | Oscillator frequency | $f_{CFOSC}$* | OSC1, OSC2: Figure 3, $f_O$ = 400 kHz | 384 | 400 | 416 | kHz |
| | | | OSC1, OSC2: Figure 3, $f_O$ = 800 kHz | 768 | 800 | 832 | |
| | | | OSC1, OSC2: Figure 3, $f_O$ = 2 MHz | 1920 | 2000 | 2080 | |
| | | | OSC1, OSC2: Figure 3, $f_O$ = 4 MHz | 3840 | 4000 | 4160 | |
| | Oscillator stabilization interval | $t_{CFS}$ | Figure 4, $f_O$ = 400 kHz | | | 10 | ms |
| | | | Figure 4, $f_O$ = 800 kHz, $f_O$ = 2 MHz, $f_O$ = 4 MHz, 1/3, 1/4 frequency divider | | | 10 | |
| [Pull-up resistors] | | | | | | | |
| | I/O ports | RPP1 | Pull-up (PU) resistor configuration for port A or D: With output N-channel transistor off and $V_{IN}$ = $V_{SS}$, $V_{DD}$ = 5 V | 30 | 70 | 130 | kΩ |
| | | RPP2 | Pull-up (PU) resistor configuration for port C: With output N-channel transistor off and $V_{IN}$ = $V_{SS}$, $V_{DD}$ = 5 V | 1.0 | 2.3 | 3.9 | |
| | Reset port | Ru | $\overline{RES}$: $V_{IN}$ = $V_{SS}$, $V_{DD}$ = 5 V | 200 | 500 | 725 | |
| External reset characteristic: Reset time | | $t_{RST}$ | | | See Figure 6. | | |
| Pin capacitance | | $C_P$ | f = 1 MHz, $V_{IN}$ = $V_{SS}$ for pins other than one being measured | | | 10 | pF |

Note: * $f_{CFOSC}$ is the allowable oscillator frequency.

## Comparator Characteristics for Comparator Option at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Reference input voltage range | $V_{RFIN}$ | $V_{REF}0$ and $V_{REF}1$ | $V_{SS}$ + 0.3 | | $V_{DD}$ – 1.5 | V |
| Inphase input voltage range | $V_{CMIN}$ | CMP0 to CMP3 | $V_{SS}$ | | $V_{DD}$ – 1.5 | V |
| Offset voltage | $V_{OFF}$ | $V_{CMIN}$ = $V_{SS}$ to $V_{DD}$ – 1.5 V | | ±50 | ±300 | mV |
| Response speed | TRS1 | Figure 5: $V_{DD}$ = 4 to 6 V | | 1.0 | 5.0 | µs |
| | TRS2 | Figure 5 | | 1.0 | 200 | |
| Input high level current | $I_{IH}1$ | $V_{REF}0$ and $V_{REF}1$ | | | 1.0 | µA |
| | $I_{IH}2$ | CMP0 to CMP3: Without feedback resistor option | | | 1.0 | |
| Input low level current | $I_{IL}1$ | $V_{REF}0$ and $V_{REF}1$ | –1.0 | | | µA |
| | $I_{IL}2$ | CMP0 to CMP3: Without feedback resistor option | –1.0 | | | |
| Feedback resistor | RCMFB | CMP0 to CMP3: With feedback resistor option | | 460 | | kΩ |

## Table 1 Guaranteed Constants for Ceramic Oscillators

| Oscillator type | Standard type | | | | | Chip type | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Manufacturer | Oscillator | C1 | C2 | Rd | Manufacturer | Oscillator | C1 | C2 |
| [External capacitor] | | | | | | | | | |
| 4-MHz ceramic oscillator | Murata | CS A4.00MG | 33 pF ± 10% | 33 pF ± 10% | — | Murata | CS AC4.00MGC | 33 pF ± 10% | 33 pF ± 10% |
| | Kyocera | KBR-4.0MSA | 33 pF ± 10% | 33 pF ± 10% | — | — | — | — | — |
| 2-MHz ceramic oscillator | Murata | CS A2.00MG | 33 pF ± 10% | 33 pF ± 10% | — | Murata | CS AC2.00MGC | 33 pF ± 10% | 33 pF ± 10% |
| | Kyocera | KBR-2.0MSA | 33 pF ± 10% | 33 pF ± 10% | — | — | — | — | — |
| [Built-in capacitor] | | | | | | | | | |
| 4-MHz ceramic oscillator | Murata | CS A4.00MG | — | — | — | Kyocera | KBR-4.0MWS | — | — |
| | Kyocera | KBR-4.0MSA | — | — | — | — | — | — | — |
| 2-MHz ceramic oscillator | Murata | CS A2.00MG | — | — | — | Kyocera | KBR-2.0MWS | — | — |
| 800-kHz ceramic oscillator | Murata | CS B800J | 100 pF ± 10% | 100 pF ± 10% | 3.3 kΩ | — | — | — | — |
| | Kyocera | KBR-800F/Y | 150 pF ± 10% | 150 pF ± 10% | — | — | — | — | — |
| 400-kHz ceramic oscillator | Murata | CS B400P | 220 pF ± 10% | 220 pF ± 10% | 3.3 kΩ | — | — | — | — |
| | Kyocera | KBR-400BK/Y | 330 pF ± 10% | 330 pF ± 10% | — | — | — | — | — |

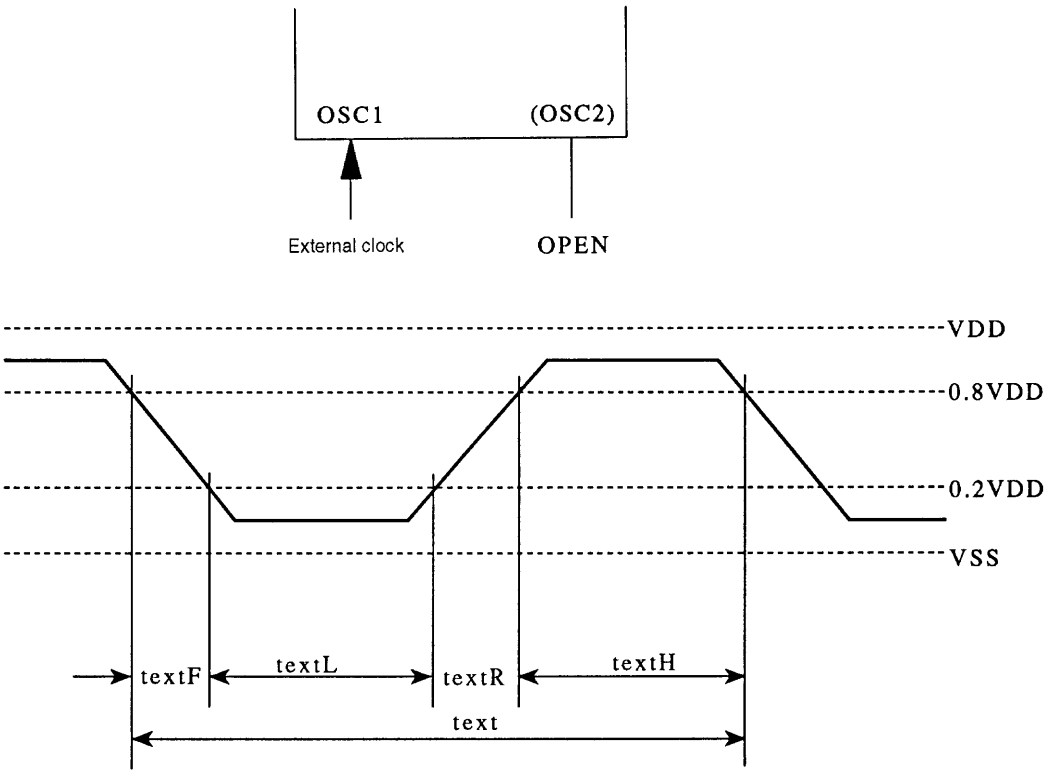



**Figure 1 External Clock Input Waveform**

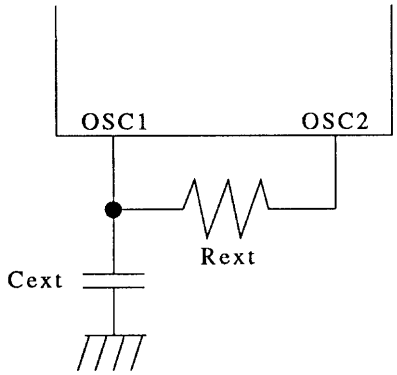



Figure 2 2-Pin RC Oscillator Circuit

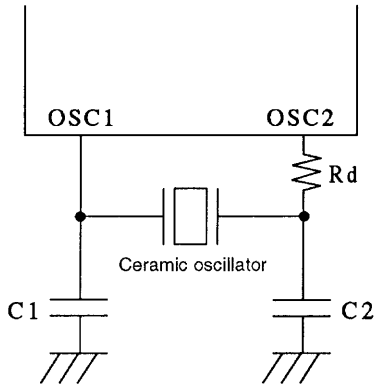



Figure 3 Ceramic Oscillator Circuit

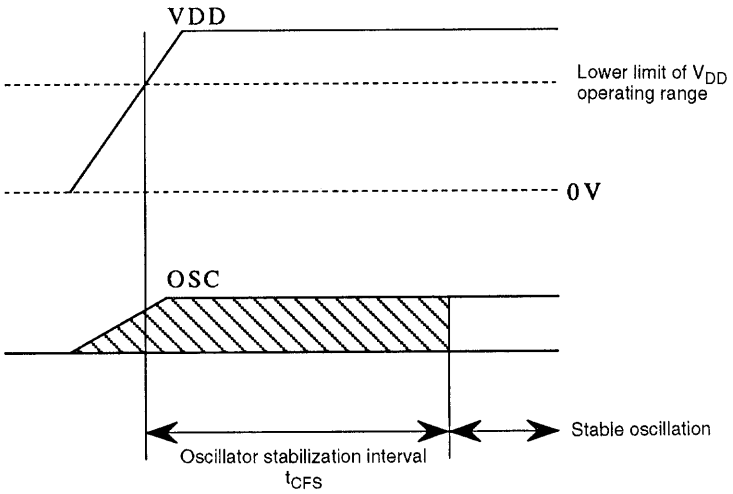



Figure 4 Oscillator Stabilization Interval

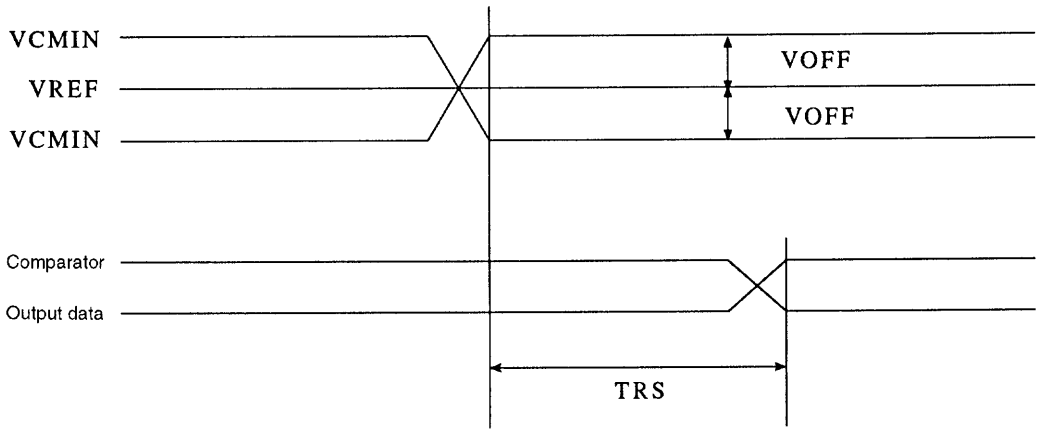
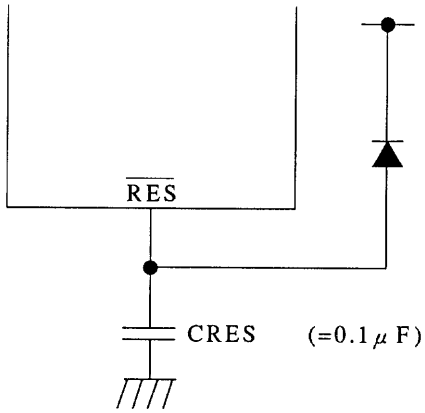



Figure 5 Comparator Response Speed (TRS) Timing




Note: When the power supply rising interval is zero, a value of 0.1 µF for CRES produces a reset interval of 10 to 100 ms. If the power supply rising interval is larger, adjust CRES to produce a minimum interval of 10 ms for the oscillation to stabilize.

**Figure 6 Reset Circuit**

### LC6529N RC Oscillator Characteristics

Figure 7 gives the RC oscillator characteristics for the LC6529N. The frequency fluctuation ranges are as follows:

1. For $V_{DD}$ = 3.0 to 6.0 V, Ta = –40 to +85°C, Cext = 220 pF, and Rext = 12.0 kΩ,

   309 kHz ≤ $f_{MOSC}$ ≤ 577 kHz

2. For $V_{DD}$ = 4.0 to 6.0 V, Ta = –40 to +85°C, Cext = 220 pF, and Rext = 4.7 kΩ,

   660 kHz ≤ $f_{MOSC}$ ≤ 1229 kHz

These results are only guaranteed for the above RC constants.
If the above values are not available, keep the RC constants within the following ranges. (See Figure 7.)

Rext = 3 to 20 kΩ, Cext = 150 to 390 pF

Note: 1. The oscillator frequency must be within the range between 350 and 750 kHz for $V_{DD}$ = 5.0 V and Ta = 25°C.
2. Make sure that the oscillator frequency remains well within the operating clock frequency range (See frequency divider option table.) for the two ranges $V_{DD}$ = 3.0 to 6.0 V, Ta = –40 to +85°C and $V_{DD}$ = 4.0 to 6.0 V, Ta = –40 to +85°C.

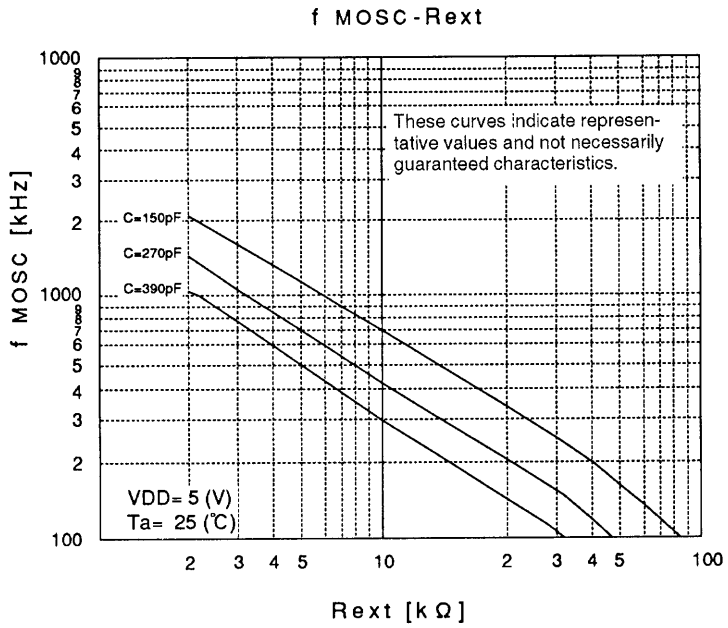



**Figure 7 RC Oscillator Frequency Data (Sample Values)**

## LC6529F

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | –0.3 | | +7.0 | V |
| Input voltage | $V_I1$ | OSC1*1 | –0.3 | | $V_{DD}$ + 0.3 | V |
| | $V_I2$ | TEST, $\overline{RES}$ | –0.3 | | $V_{DD}$ + 0.3 | |
| | $V_I3$ | Port E (PE) configuration | –0.3 | | $V_{DD}$ + 0.3 | |
| Output voltage | $V_O$ | OSC2 | Voltages up to that generated allowed. | | | V |
| I/O voltages | $V_{IO}1$ | Open-drain (OD) configuration | –0.3 | | +15 | V |
| | $V_{IO}2$ | Pull-up (PU) resistor configuration | –0.3 | | $V_{DD}$ + 0.3 | |
| Peak output current | $I_{OP}$ | PA, PC, PD | –2 | | +20 | mA |
| Average output current | $I_{OA}$ | PA, PC, PD: Average for pin over 100-ms interval | –2 | | +20 | mA |
| | $\Sigma I_{OA}1$ | PA: Total current for pins PA0 to PA3*2 | –6 | | +40 | |
| | $\Sigma I_{OA}2$ | PC, PD: Total current for pins PC0 to PC3 and PD0 to PD3*2 | –14 | | +90 | |
| Allowable power dissipation | Pd max1 | Ta = –40 to +85°C (DIP24S) | | | 360 | mW |
| | Pd max2 | Ta = –40 to +85°C (SSOP24) | | | 165 | |
| | Pd max3 | Ta = –40 to +85°C (MFP30S) | | | 150 | |
| Operating temperature | Topr | | –40 | | +85 | °C |
| Storage temperature | Tstg | | –55 | | +125 | |

Note: 1. When the oscillator circuit in Figure 3 and the guaranteed constant are used, this is guaranteed over the full amplitude.
2. Averaged over 100-ms interval.

### Allowable Operating Ranges at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 3.0 | | 6.0 | V |
| Standby voltage | $V_{ST}$ | $V_{DD}$: Preserves contents of RAM and registers*. | 1.8 | | 6.0 | V |
| Input high level voltage | $V_{IH}1$ | Open-drain (OD) configuration: With output N-channel transistor off | 0.7 $V_{DD}$ | | 13.5 | V |
| | $V_{IH}2$ | Pull-up (PU) resistor configuration: With output N-channel transistor off | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}3$ | PE: Using port E configuration | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}4$ | $\overline{RES}$: $V_{DD}$ = 1.8 to 6 V | 0.8 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}5$ | OSC1: Using external clock option | 0.8 $V_{DD}$ | | $V_{DD}$ | |
| Input low level voltage | $V_{IL}1$ | PA, PC, PD: With output N-channel transistor off, $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.3 $V_{DD}$ | V |
| | $V_{IL}2$ | PA, PC, PD: With output N-channel transistor off | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}3$ | PE: Using port E configuration, $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.3 $V_{DD}$ | |
| | $V_{IL}4$ | PE: Using port E configuration | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}5$ | OSC1: Using external clock option, $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}6$ | OSC1: Using external clock option | $V_{SS}$ | | 0.2 $V_{DD}$ | |
| | $V_{IL}7$ | TEST: $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.3 $V_{DD}$ | |
| | $V_{IL}8$ | TEST | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}9$ | $\overline{RES}$: $V_{DD}$ = 4 to 6 V | $V_{SS}$ | | 0.25 $V_{DD}$ | |
| | $V_{IL}10$ | $\overline{RES}$ | $V_{SS}$ | | 0.2 $V_{DD}$ | |
| Operating frequency (cycle time) | fop (Tcyc) | | 200 (20) | | 4330 (0.92) | kHz (µs) |
| [External clock conditions] | | | | | | |
| Frequency | text | OSC1: Figure 1 | 200 | | 4330 | kHz |
| Pulse width | textH, textL | | 69 | | | ns |
| Rise/fall times | textR, textF | | | | 50 | |
| Oscillator guaranteed constants Ceramic oscillator | | Figure 2 | See Table 1. | | | |

Note: * Maintain the power supply voltage at $V_{DD}$ until the HALT instruction has completed execution, placing the chip in the standby mode. Block chattering from entering PA3 during the HALT instruction execution cycle.

## Electrical Characteristics at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high level current | $I_{IH}1$ | Open-drain (OD) configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN}$ = 13.5 V | | | 5.0 | µA |
| | $I_{IH}2$ | PE: Using port E configuration, $V_{IN} = V_{DD}$ | | | 1.0 | |
| | $I_{IH}3$ | OSC1: Using external clock option, $V_{IN} = V_{DD}$ | | | 1.0 | |
| Input low level current | $I_{IL}1$ | Open-drain (OD) configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –1.0 | | | µA |
| | $I_{IL}2$ | Pull-up (PU) resistor configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –220 | –71.5 | | |
| | $I_{IL}3$ | Pull-up (PU) resistor configuration for port C: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –6.00 | –2.17 | | mA |
| | $I_{IL}4$ | PE: Using port E configuration, $V_{IN} = V_{SS}$ | –1.0 | | | µA |
| | $I_{IL}5$ | $\overline{RES}$: $V_{IN} = V_{SS}$ | –45 | –10 | | |
| | $I_{IL}6$ | OSC1: Using external clock option, $V_{IN} = V_{SS}$ | –1.0 | | | |
| Output high level voltage | $V_{OH}1$ | Pull-up (PU) resistor configuration for port C: $I_{OH}$ = –300 µA, $V_{DD}$ = 4 to 6 V | $V_{DD}$ – 1.2 | | | V |
| | $V_{OH}2$ | Pull-up (PU) resistor configuration for port C: $I_{OH}$ = –60 µA | $V_{DD}$ – 0.5 | | | |
| Output low level voltage | $V_{OL}1$ | PA, PC, PD: $I_{OL}$ = 10 mA, $V_{DD}$ = 4 to 6 V | | | 1.5 | V |
| | $V_{OL}2$ | PA, PC, PD: With $I_{OL}$ for each port less than or equal to 1 mA, $I_{OL}$ = 1.8 mA | | | 0.4 | |
| Hysteresis voltage | $V_{HIS}1$ | $\overline{RES}$ | | 0.1 $V_{DD}$ | | V |
| | $V_{HIS}2$ | OSC1*: Using RC oscillator or external clock option | | 0.1 $V_{DD}$ | | |

Note: * The RC oscillator and external clock options require a Schmidt trigger configuration for OSC1.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| [Current drain] | | | | | | |
| Ceramic oscillator | $I_{DD\ OP}1$ | $V_{DD}$: Figure 2, 4 MHz, 200 to 4330 kHz, 1/1 frequency divider Note: With output N-channel transistor off and port level = $V_{DD}$ | | 1.6 | 4.0 | mA |
| External clock | $I_{DD\ OP}2$ | | | 1.6 | 4.2 | |
| Standby operation | $I_{DD\ st}1$ | $V_{DD}$: With output N-channel transistor off and port level = $V_{DD}$, $V_{DD}$ = 6 V | | 0.05 | 10 | µA |
| | $I_{DD\ st}2$ | $V_{DD}$: With output N-channel transistor off and port level = $V_{DD}$, $V_{DD}$ = 3 V | | 0.025 | 5 | |
| [Oscillator characteristics] (Ceramic oscillator) | | | | | | |
| Oscillator frequency | $f_{CFOSC}$ | OSC1, OSC2: Figure 2, $f_O$ = 4 MHz* | 3840 | 4000 | 4160 | kHz |
| Oscillator stabilization interval | $t_{CFS}$ | Figure 3, $f_O$ = 4 MHz | | | 10 | ms |
| [Pull-up resistors] | | | | | | |
| I/O ports | RPP1 | Pull-up (PU) resistor configuration for port A or D: With output N-channel transistor off and $V_{IN} = V_{SS}$, $V_{DD}$ = 5 V | 30 | 70 | 130 | kΩ |
| | RPP2 | Pull-up (PU) resistor configuration for port C: With output N-channel transistor off and $V_{IN} = V_{SS}$, $V_{DD}$ = 5 V | 1.0 | 2.3 | 3.9 | |
| Reset port | Ru | $\overline{RES}$: $V_{IN} = V_{SS}$, $V_{DD}$ = 5 V | 200 | 500 | 725 | |
| External reset characteristic: Reset time | $t_{RST}$ | | | See Figure 5. | | |
| Pin capacitance | $C_P$ | f = 1 MHz, $V_{IN} = V_{SS}$ for pins other than one being measured | | 10 | | pF |

Note: * $f_{CFOSC}$ is the allowable oscillator frequency.

## Comparator Characteristics for Comparator Option at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Reference input voltage range | $V_{RFIN}$ | $V_{REF}0$, $V_{REF}1$ | $V_{SS}$ + 0.3 | | $V_{DD}$ – 1.5 | V |
| Inphase input voltage range | $V_{CMIN}$ | CMP0 to CMP3 | $V_{SS}$ | | $V_{DD}$ – 1.5 | V |
| Offset voltage | $V_{OFF}$ | $V_{CMIN}$ = $V_{SS}$ to $V_{DD}$ – 1.5 V | | ±50 | ±300 | mV |
| Response speed | TRS1 | Figure 4: $V_{DD}$ = 4 to 6 V | | 1.0 | 5.0 | µs |
| | TRS2 | Figure 4 | | 1.0 | 200 | |
| Input high level current | $I_{IH}1$ | $V_{REF}0$, $V_{REF}1$ | | | 1.0 | µA |
| | $I_{IH}2$ | CMP0 to CMP3: Without feedback resistor option | | | 1.0 | |
| Input low level current | $I_{IL}1$ | $V_{REF}0$, $V_{REF}1$ | –1.0 | | | µA |
| | $I_{IL}2$ | CMP0 to CMP3: Without feedback resistor option | –1.0 | | | |
| Feedback resistor | RCMFB | CMP0 to CMP3: With feedback resistor option | | 460 | | kΩ |

## Table 1. Guaranteed Constants for Ceramic Oscillators

| Oscillator type | Standard type | | | | | Chip type | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Manufacturer | Oscillator | C1 | C2 | Rd | Manufacturer | Oscillator | C1 | C2 |
| [External capacitor] | | | | | | | | | |
| 4-MHz ceramic oscillator | Murata | CS A4.00MG | 33 pF ± 10% | 33 pF ± 10% | — | Murata | CS AC4.00MGC | 33 pF ± 10% | 33 pF ± 10% |
| | Kyocera | KBR-4.0MSA | 33 pF ± 10% | 33 pF ± 10% | — | — | — | — | — |
| 2-MHz ceramic oscillator | Murata | CS A2.00MG | 33 pF ± 10% | 33 pF ± 10% | — | Murata | CS AC2.00MGC | 33 pF ± 10% | 33 pF ± 10% |
| | Kyocera | KBR-2.0MSA | 33 pF ± 10% | 33 pF ± 10% | — | — | — | — | — |
| [Built-in capacitor] | | | | | | | | | |
| 4-MHz ceramic oscillator | Murata | CS A4.00MG | — | — | — | Kyocera | KBR-4.0MWS | — | — |
| | Kyocera | KBR-4.0MSA | — | — | — | — | — | — | — |
| 2-MHz ceramic oscillator | Murata | CS A2.00MG | — | — | — | Kyocera | KBR-2.0MWS | — | — |

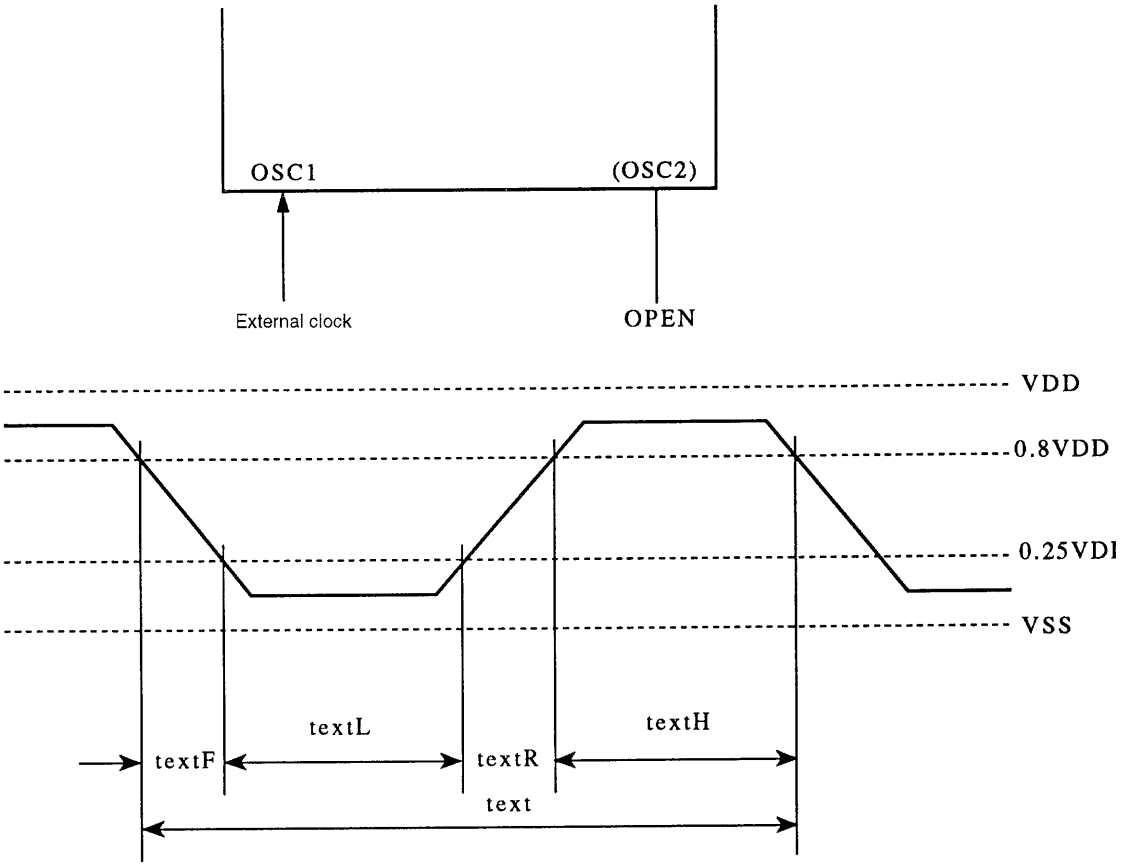



**Figure 1 External Clock Input Waveform**

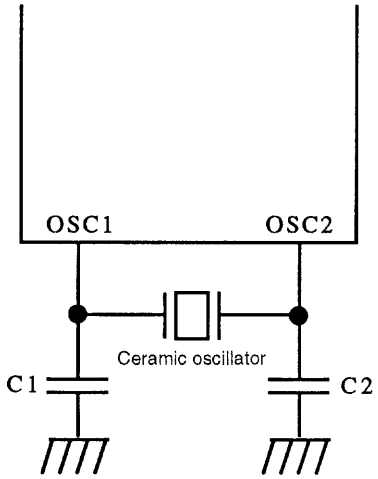



Figure 2 Ceramic Oscillator Circuit

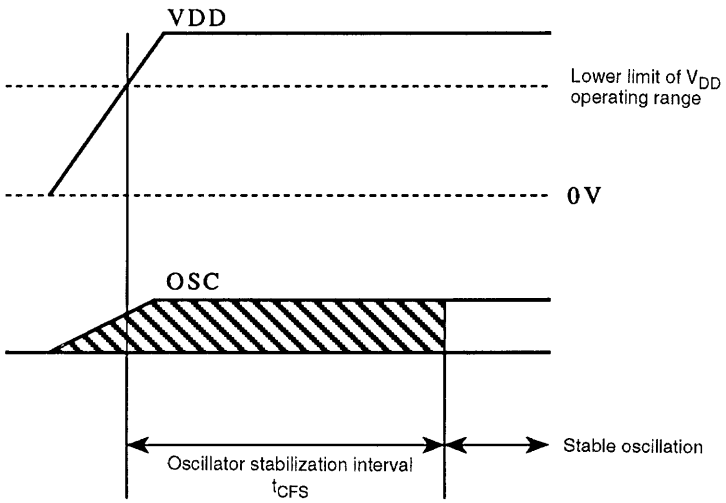



Figure 3 Oscillator Stabilization Interval

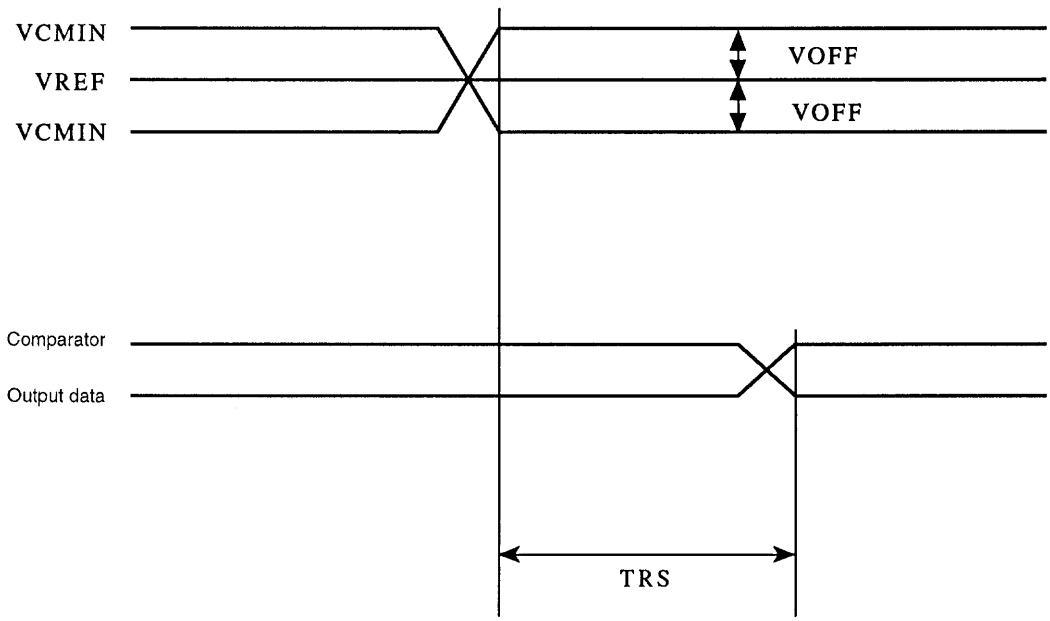
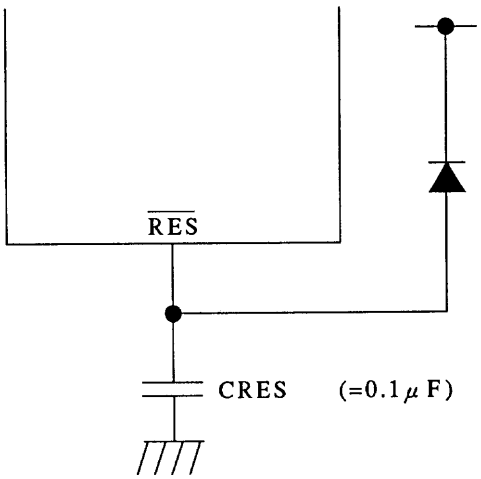



Figure 4 Comparator Response Speed (TRS) Timing




Note: When the power supply rising interval is zero, a value of 0.1 μF for CRES produces a reset interval of 10 to 100 ms. If the power supply rising interval is larger, adjust CRES to produce a minimum interval of 10 ms for the oscillation to stabilize.

**Figure 5 Reset Circuit**

## LC6529L

### Absolute Maximum Ratings at Ta = 25°C, $V_{SS}$ = 0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Maximum supply voltage | $V_{DD}$ max | $V_{DD}$ | –0.3 | | +7.0 | V |
| Input voltage | $V_I1$ | OSC1[*1] | –0.3 | | $V_{DD}$ + 0.3 | V |
| | $V_I2$ | TEST, $\overline{RES}$ | –0.3 | | $V_{DD}$ + 0.3 | |
| | $V_I3$ | Port E (PE) configuration | –0.3 | | $V_{DD}$ + 0.3 | |
| Output voltage | $V_O$ | OSC2 | Voltages up to that generated allowed. | | | V |
| I/O voltages | $V_{IO}1$ | Open-drain (OD) configuration | –0.3 | | +15 | V |
| | $V_{IO}2$ | Pull-up (PU) resistor configuration | –0.3 | | $V_{DD}$ + 0.3 | |
| Peak output current | $I_{OP}$ | PA, PC, PD | –2 | | +20 | mA |
| Average output current | $I_{OA}$ | PA, PC, PD: Average for pin over 100-ms interval | –2 | | +20 | mA |
| | $\Sigma I_{OA}1$ | PA: Total current for pins PA0 to 3[*2] | –6 | | +40 | |
| | $\Sigma I_{OA}2$ | PC, PD: Total current for pins PC0 to PC3 and PD0 to PD3[*2] | –14 | | +90 | |
| Allowable power dissipation | Pd max1 | Ta = –40 to +85°C (DIP24S) | | | 360 | mW |
| | Pd max2 | Ta = –40 to +85°C (SSOP24) | | | 165 | |
| | Pd max3 | Ta = –40 to +85°C (MFP30S) | | | 150 | |
| Operating temperature | Topr | | –40 | | +85 | °C |
| Storage temperature | Tstg | | –55 | | +125 | |

Note: 1. When the oscillator circuit in Figure 3 and the guaranteed constant are used, this is guaranteed over the full amplitude.
2. Averaged over 100-ms interval.

### Allowable Operating Ranges at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 2.2 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | $V_{DD}$ | 2.2 | | 6.0 | V |
| Standby voltage | $V_{ST}$ | $V_{DD}$: Preserves contents of RAM and registers*. | 1.8 | | 6.0 | V |
| Input high level voltage | $V_{IH}1$ | Open-drain (OD) configuration: With output N-channel transistor off | 0.7 $V_{DD}$ | | 13.5 | V |
| | $V_{IH}2$ | Pull-up (PU) resistor configuration: With output N-channel transistor off | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}3$ | PE: Using port E configuration | 0.7 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}4$ | $\overline{RES}$: $V_{DD}$ = 1.8 to 6 V | 0.8 $V_{DD}$ | | $V_{DD}$ | |
| | $V_{IH}5$ | OSC1: Using external clock option | 0.8 $V_{DD}$ | | $V_{DD}$ | |
| Input low level voltage | $V_{IL}1$ | PA, PC, PD: With output N-channel transistor off | $V_{SS}$ | | 0.2 $V_{DD}$ | V |
| | $V_{IL}2$ | PE: Using port E configuration | $V_{SS}$ | | 0.2 $V_{DD}$ | |
| | $V_{IL}3$ | OSC1: Using external clock option | $V_{SS}$ | | 0.15 $V_{DD}$ | |
| | $V_{IL}4$ | TEST | $V_{SS}$ | | 0.2 $V_{DD}$ | |
| | $V_{IL}5$ | $\overline{RES}$ | $V_{SS}$ | | 0.15 $V_{DD}$ | |
| Operating frequency (cycle time) | fop (Tcyc) | Using the built-in 1/3 or 1/4 frequency dividers extends the maximum to 4.16 MHz. | 200 (20) | | 1040 (3.84) | kHz (µs) |
| [External clock conditions] | | | | | | |
| Frequency | text | OSC1: If the clock frequency exceeds 1.040 MHz, use the built-in 1/3 or 1/4 frequency divider. Figure 1 | 200 | | 4160 | kHz |
| Pulse width | textH, textL | | 120 | | | ns |
| Rise/fall times | textR, textF | | | | 100 | |
| [Oscillator guaranteed constants] | | | | | | |
| 2-pin RC oscillator circuit | Cext | OSC1, OSC2: Figure 2 | 220 ± 5% | | | pF |
| | Rext | OSC1, OSC2: Figure 2 | 12.0 ± 1% | | | kΩ |
| Ceramic oscillator | | Figure 3 | See Table 1. | | | |

Note: * Maintain the power supply voltage at $V_{DD}$ until the HALT instruction has completed execution, placing the chip in the standby mode. Block chattering from entering PA3 during the HALT instruction execution cycle.

## Electrical Characteristics at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 2.2 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Input high level current | $I_{IH}1$ | Open-drain (OD) configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN}$ = 13.5 V | | | 5.0 | µA |
| | $I_{IH}2$ | PE: Using port E configuration, $V_{IN} = V_{DD}$ | | | 1.0 | |
| | $I_{IH}3$ | OSC1: Using external clock option, $V_{IN} = V_{DD}$ | | | 1.0 | |
| Input low level current | $I_{IL}1$ | Open-drain (OD) configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –1.0 | | | µA |
| | $I_{IL}2$ | Pull-up (PU) resistor configuration for port: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –220 | –71.5 | | |
| | $I_{IL}3$ | Pull-up (PU) resistor configuration for port C: With output N-channel transistor off. (Includes transistor's leak current.) $V_{IN} = V_{SS}$ | –6.00 | –2.17 | | mA |
| | $I_{IL}4$ | PE: Using port E configuration, $V_{IN} = V_{SS}$ | –1.0 | | | µA |
| | $I_{IL}5$ | $\overline{RES}$: $V_{IN} = V_{SS}$ | –45 | –10 | | |
| | $I_{IL}6$ | OSC1: Using external clock option, $V_{IN} = V_{SS}$ | –1.0 | | | |
| Output high level voltage | $V_{OH}$ | Pull-up (PU) resistor configuration for port C: $I_{OH}$ = –50 µA | $V_{DD}$ – 0.5 | | | V |
| Output low level voltage | $V_{OL}1$ | PA, PC, PD: $I_{OL}$ = 3 mA | | | 1.5 | V |
| | $V_{OL}2$ | PA, PC, PD: With $I_{OL}$ for each port less than or equal to 1 mA, $I_{OL}$ = 1 mA | | | 0.4 | |
| Hysteresis voltage | $V_{HIS}1$ | $\overline{RES}$ | | 0.1 $V_{DD}$ | | V |
| | $V_{HIS}2$ | OSC1*: Using RC oscillator or external clock option | | 0.1 $V_{DD}$ | | |

Note: * The RC oscillator and external clock options require a Schmidt trigger configuration for OSC1.

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| [Current drain] | | | | | | |
| RC oscillator | $I_{DD\ OP}1$ | $V_{DD}$: Figure 2, 400 kHz (typ) | | 0.4 | 1.0 | mA |
| Ceramic oscillator | $I_{DD\ OP}2$ | $V_{DD}$: Figure 3, 4 MHz, 1/4 frequency divider | | 1.6 | 4.0 | |
| | $I_{DD\ OP}3$ | $V_{DD}$: Figure 3, 4 MHz, 1/4 frequency divider, $V_{DD}$ = 2.2 V | | 0.4 | 0.8 | |
| | $I_{DD\ OP}4$ | $V_{DD}$: Figure 3, 2 MHz, 1/3 frequency divider | | 1.3 | 3.0 | |
| | $I_{DD\ OP}5$ | $V_{DD}$: Figure 3, 2 MHz, 1/4 frequency divider | | 1.3 | 3.0 | |
| | $I_{DD\ OP}6$ | $V_{DD}$: Figure 3, 2 MHz, 1/3, 1/4 frequency divider $V_{DD}$ = 2.2 V | | 0.3 | 0.6 | |
| | $I_{DD\ OP}7$ | $V_{DD}$: Figure 3, 800 kHz | | 1.1 | 2.6 | |
| | $I_{DD\ OP}8$ | $V_{DD}$: Figure 3, 400 kHz | | 0.9 | 2.4 | |
| External clock | $I_{DD\ OP}9$ | $V_{DD}$: 200 to 667 kHz, 1/1 frequency divider, 600 to 2000 kHz, 1/3 frequency divider, 800 to 2667 kHz, 1/4 frequency divider | | 1.0 | 2.5 | mA |
| Standby operation | $I_{DD}$ st1 | $V_{DD}$: With output N-channel transistor off and port level = $V_{DD}$, $V_{DD}$ = 6 V | | 0.05 | 10 | µA |
| | $I_{DD}$ st2 | $V_{DD}$: With output N-channel transistor off and port level = $V_{DD}$, $V_{DD}$ = 2.2 V | | 0.025 | 5 | |
| [Oscillator characteristics] | | | | | | |
| RC oscillator Oscillator frequency | $f_{MOSC}$ | OSC1, OSC2: Figure 2, Cext = 220 pF ± 5%, Rext = 12.0 kΩ ± 1% | 275 | 400 | 577 | kHz |
| [Oscillator characteristics] (Ceramic oscillator) | | | | | | |
| Oscillator frequency | $f_{CFOSC}$* | OSC1, OSC2: Figure 3, $f_O$ = 400 kHz | 384 | 400 | 416 | kHz |
| | | OSC1, OSC2: Figure 3, $f_O$ = 800 kHz | 768 | 800 | 832 | |
| | | OSC1, OSC2: Figure 3, $f_O$ = 2 MHz | 1920 | 2000 | 2080 | |
| | | OSC1, OSC2: Figure 3, $f_O$ = 4 MHz, 1/4 frequency divider | 3840 | 4000 | 4160 | |
| Oscillator stabilization interval | $t_{CFS}$ | Figure 4, $f_O$ = 400 kHz | | | 10 | ms |
| | | Figure 4, $f_O$ = 800 kHz, $f_O$ = 2 MHz, 1/3, 1/4 frequency divider, $f_O$ = 4 MHz, 1/4 frequency divider | | | 10 | |

Continued on next page.

Continued from preceding page.

| Parameter | | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|---|
| [Pull-up resistors] | | | | | | | |
| | I/O ports | RPP1 | Pull-up (PU) resistor configuration for port A or D: With output N-channel transistor off and $V_{IN} = V_{SS}$, $V_{DD}$ = 5 V | 30 | 70 | 130 | kΩ |
| | | RPP2 | Pull-up (PU) resistor configuration for port C: With output N-channel transistor off and $V_{IN} = V_{SS}$, $V_{DD}$ = 5 V | 1.0 | 2.3 | 3.9 | |
| | Reset port | Ru | $\overline{RES}$: $V_{IN} = V_{SS}$, $V_{DD}$ = 5 V | 200 | 500 | 725 | |
| External reset characteristic: Reset time | | $t_{RST}$ | | See Figure 6. | | | |
| Pin capacitance | | $C_P$ | f = 1 MHz, $V_{IN} = V_{SS}$ for pins other than one being measured | | 10 | | pF |

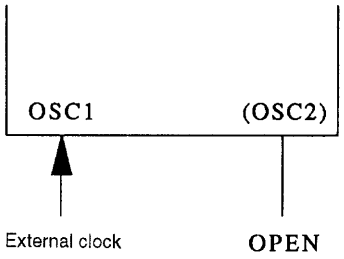
Note * $f_{CFOSC}$ is the allowable oscillator frequency.

## Comparator Characteristics for Comparator Option at Ta = –40 to +85°C, $V_{SS}$ = 0 V, $V_{DD}$ = 3.0 to 6.0 V

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|---|---|---|---|---|---|---|
| Reference input voltage range | $V_{RFIN}$ | $V_{REF}0$, $V_{REF}1$ | $V_{SS}$ + 0.3 | | $V_{DD}$ – 1.5 | V |
| Inphase input voltage range | $V_{CMIN}$ | CMP0 to CMP3 | $V_{SS}$ | | $V_{DD}$ – 1.5 | V |
| Offset voltage | $V_{OFF}$ | $V_{CMIN} = V_{SS}$ to $V_{DD}$ – 1.5 V | | ±50 | ±300 | mV |
| Response speed | TRS | Figure 5 | | 1.0 | 200 | µs |
| Input high level current | $I_{IH}1$ | $V_{REF}0$, $V_{REF}1$ | | | 1.0 | µA |
| | $I_{IH}2$ | CMP0 to CMP3: Without feedback resistor option | | | 1.0 | |
| Input low level current | $I_{IL}1$ | $V_{REF}0$, $V_{REF}1$ | –1.0 | | | µA |
| | $I_{IL}2$ | CMP0 to CMP3: Without feedback resistor option | –1.0 | | | |
| Feedback resistor | RCMFB | CMP0 to CMP3: With feedback resistor option | | 460 | | kΩ |

## Table 1 Guaranteed Constants for Ceramic Oscillators

| Oscillator type | Standard type | | | | | Chip type | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Manufacturer | Oscillator | C1 | C2 | Rd | Manufacturer | Oscillator | C1 | C2 |
| [External capacitor] | | | | | | | | | |
| 4-MHz ceramic oscillator | Murata | CS A4.00MG | 33 pF ± 10% | 33 pF ± 10% | — | Murata | CS AC4.00MGC | 33 pF ± 10% | 33 pF ± 10% |
| | Kyocera | KBR-4.0MSA | 33 pF ± 10% | 33 pF ± 10% | — | — | — | — | — |
| 2-MHz ceramic oscillator | Murata | CS A2.00MG | 33 pF ± 10% | 33 pF ± 10% | — | Murata | CS AC2.00MGC | 33 pF ± 10% | 33 pF ± 10% |
| | Kyocera | KBR-2.0MSA | 33 pF ± 10% | 33 pF ± 10% | — | — | — | — | — |
| [Built-in capacitor] | | | | | | | | | |
| 4-MHz ceramic oscillator | Murata | CS A4.00MG | — | — | — | Kyocera | KBR-4.0MWS | — | — |
| | Kyocera | KBR-4.0MSA | — | — | — | — | — | — | — |
| 2-MHz ceramic oscillator | Murata | CS A2.00MG | — | — | — | Kyocera | KBR-2.0MWS | — | — |
| 800-kHz ceramic oscillator | Murata | CS B800J | 100 pF ± 10% | 100 pF ± 10% | 3.3 kΩ | — | — | — | — |
| | Kyocera | KBR-800F/Y | 150 pF ± 10% | 150 pF ± 10% | — | — | — | — | — |
| 400-kHz ceramic oscillator | Murata | CS B400P | 220 pF ± 10% | 220 pF ± 10% | 3.3 kΩ | — | — | — | — |
| | Kyocera | KBR-400BK/Y | 330 pF ± 10% | 330 pF ± 10% | — | — | — | — | — |



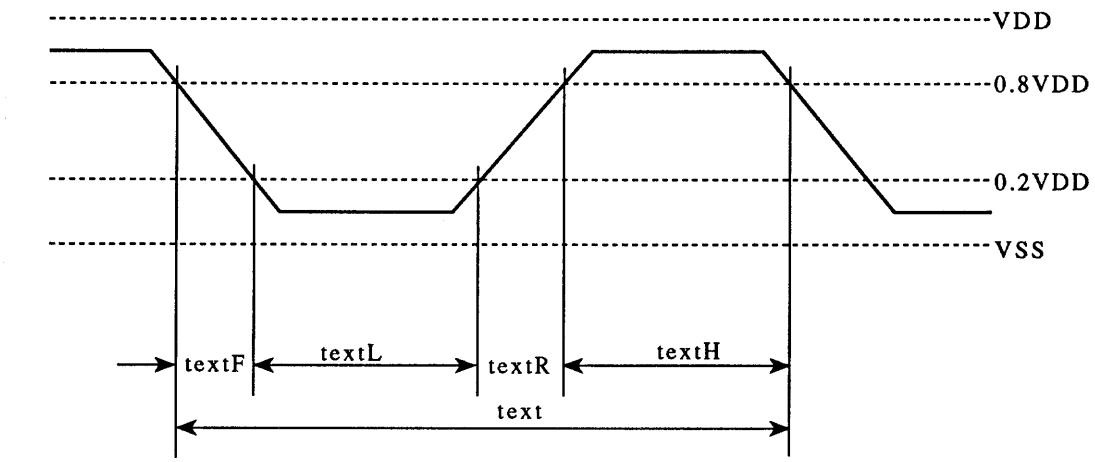




**Figure 1 External Clock Input Waveform**

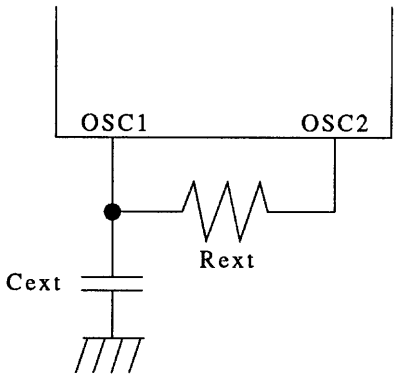



**Figure 2 2-Pin RC Oscillator Circuit**

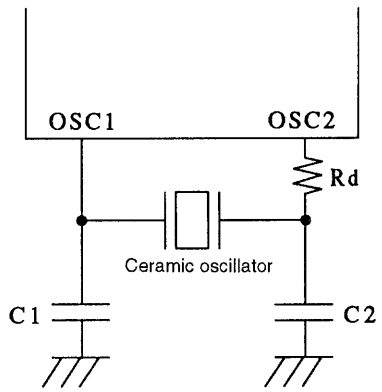



**Figure 3 Ceramic Oscillator Circuit**

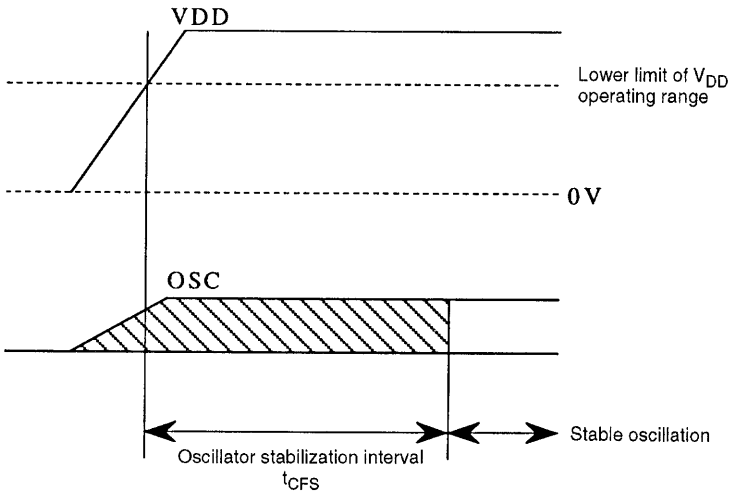



**Figure 4 Oscillator Stabilization Interval**

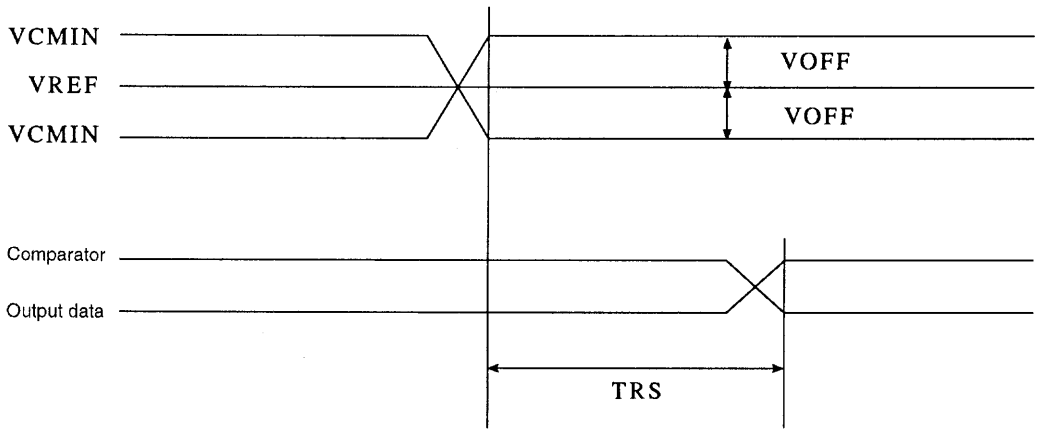
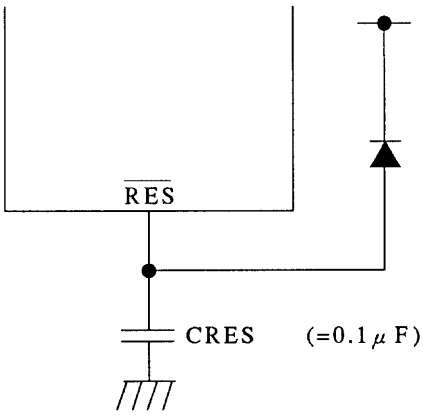



**Figure 5 Comparator Response Speed (TRS) Timing**




Note: When the power supply rising interval is zero, a value of 0.1 µF for CRES produces a reset interval of 10 to 100 ms. If the power supply rising interval is larger, adjust CRES to produce a minimum interval of 10 ms for the oscillation to stabilize.

**Figure 6 Reset Circuit**

### LC6529L RC Oscillator Characteristics

Figure 7 gives the RC oscillator characteristics for the LC6529L. The frequency fluctuation range is as follows:

For $V_{DD}$ = 2.2 to 6.0 V, Ta = –40 to +85°C, Cext = 220 pF, and Rext = 12.0 kΩ,

275 kHz ≤ = $f_{MOSC}$ ≤ = 577 kHz

These results are only guaranteed for the above RC constants.
If the above values are not available, keep the RC constants within the following ranges: (See Figure 7.)

Rext = 3 to 20 kΩ, Cext = 150 to 390 pF

Note: 1. The oscillator frequency must be within the range between 350 and 750 kHz for $V_{DD}$ = 5.0 V and Ta = 25°C.
2. Make sure that the oscillator frequency remains well within the operating clock frequency range (See frequency divider option table.) for the range $V_{DD}$ = 2.2 to 6.0 V, Ta = –40 to +85°C.

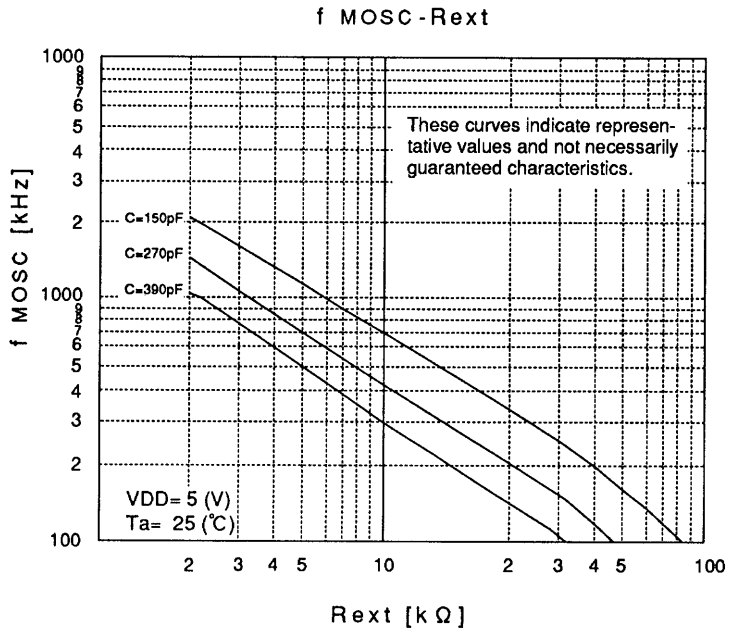



**Figure 7 RC Oscillator Frequency Data (Sample Values)**

## LC6529N/F/L Instruction Table (by Function)

Abbreviations:

| | | | |
|---|---|---|---|
| AC: | Accumulator | STACK | Stack register |
| ACt: | Accumulator bit t | TM: | Timer |
| CF: | Carry flag | TMF: | Timer overflow flag |
| DP: | Data pointer | ZF: | Zero flag |
| E: | E register | ( ), [ ]: | Indicates the contents of a location |
| M: | Memory | ←: | Transfer direction, result |
| M (DP): | Memory addressed by DP | +: | Addition |
| P ($DP_L$): | I/O port specified by $DP_L$ | –: | Subtraction |
| PC: | Program counter | ∀: | Exclusive or |

| Mnemonic | | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | $D_7$ $D_6$ $D_5$ $D_4$ | $D_3$ $D_2$ $D_1$ $D_0$ | | | | | | |
| [Accumulator manipulation instructions] | | | | | | | | | |
| CLA | Clear AC | 1 1 0 0 | 0 0 0 0 | 1 | 1 | AC ← 0 | Set AC to zero. | ZF | * |
| CLC | Clear CF | 1 1 1 0 | 0 0 0 1 | 1 | 1 | CF ← 0 | Clear CF to zero. | CF | |
| STC | Set CF | 1 1 1 1 | 0 0 0 1 | 1 | 1 | CF ← 1 | Set CF to one. | CF | |
| CMA | Complement AC | 1 1 1 0 | 1 0 1 1 | 1 | 1 | AC ← ($\overline{AC}$) | Take ones complement of AC. | ZF | |
| INC | Increment AC | 0 0 0 0 | 1 1 1 0 | 1 | 1 | AC ← (AC) + 1 | Add one to AC. | ZF, CF | |
| DEC | Decrement AC | 0 0 0 0 | 1 1 1 1 | 1 | 1 | AC ← (AC) – 1 | Subtract one from AC. | ZF, CF | |
| TAE | Transfer AC to E | 0 0 0 0 | 0 0 1 1 | 1 | 1 | E ← (AC) | Copy contents of AC to E. | | |
| XAE | Exchange AC with E | 0 0 0 0 | 1 1 0 1 | 1 | 1 | (AC) ↔ (E) | Exchange contents of AC and E. | | |
| [Memory manipulation instructions] | | | | | | | | | |
| INM | Increment M | 0 0 1 0 | 1 1 1 0 | 1 | 1 | M (DP) ← [M (DP)] + 1 | Add one to M (DP). | ZF, CF | |
| DEM | Decrement M | 0 0 1 0 | 1 1 1 1 | 1 | 1 | M (DP) ← [M (DP)] – 1 | Subtract one from M (DP). | ZF, CF | |
| SMB bit | Set M data bit | 0 0 0 0 | 1 0 $B_1$ $B_0$ | 1 | 1 | M (DP, $B_1$ $B_0$) ← 1 | Set bit specified by immediate data $B_1$ $B_0$ in M (DP) to one. | | |
| RMB bit | Reset M data bit | 0 0 1 0 | 1 0 $B_1$ $B_0$ | 1 | 1 | M (DP, $B_1$ $B_0$) ← 0 | Clear bit specified by immediate data $B_1$ $B_0$ in M (DP) to zero. | ZF | |
| [Arithmetic, logic and comparison instructions] | | | | | | | | | |
| AD | Add M to AC | 0 1 1 0 | 0 0 0 0 | 1 | 1 | AC ← (AC) + [M (DP)] | Add contents of M (DP) to contents of AC and store result in AC. | ZF, CF | |
| ADC | Add M to AC with CF | 0 0 1 0 | 0 0 0 0 | 1 | 1 | AC ← (AC) + [M (DP)] + (CF) | Add contents of M (DP) and CF to contents of AC and store result in AC. | ZF, CF | |
| DAA | Decimal adjust AC in addition | 1 1 1 0 | 0 1 1 0 | 1 | 1 | AC ← (AC) + 6 | Add 6 to contents of AC. | ZF | |
| DAS | Decimal adjust AC in subtraction | 1 1 1 0 | 1 0 1 0 | 1 | 1 | AC ← (AC) + 10 | Add 10 to contents of AC. | ZF | |
| EXL | Exclusive or M to AC | 1 1 1 1 | 0 1 0 1 | 1 | 1 | AC ← (AC) [M (DP)] | XOR contents of AC with contents of M (DP) and store result in AC. | ZF | |
| CM | Compare AC with M | 1 1 1 1 | 1 0 1 1 | 1 | 1 | $\overline{[M (DP)]}$ + (AC) + 1 | Compare contents of M (DP) with those of AC and set CF and ZF according to result. | ZF, CF | |

Note: * The second and subsequent repetitions of an LI or CLA instruction produce the same effects as an NOP instruction.

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| Mnemonic | | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | $D_7\ D_6\ D_5\ D_4$ | $D_3\ D_2\ D_1\ D_0$ | | | | | | |
| [Accumulator manipulation instructions] | | | | | | | | | |
| CI data | Compare AC with immediate data | 0 0 1 0<br>0 1 0 0 | 1 1 0 0<br>$I_3\ I_2\ I_1\ I_0$ | 2 | 2 | $\overline{I_3\ I_2\ I_1\ I_0}$ + (AC) + 1 | Compare contents of immediate data field ($I_3\ I_2\ I_1\ I_0$) with those of AC and set CF and ZF according to result.<br>Magnitude comparison / CF / ZF<br>$I_3\ I_2\ I_1\ I_0$ > AC: 0 0<br>$I_3\ I_2\ I_1\ I_0$ = AC: 1 1<br>$I_3\ I_2\ I_1\ I_0$ < AC: 1 0 | ZF, CF | |
| [Load and store instructions] | | | | | | | | | |
| LI data | Load AC with immediate data | 1 1 0 0 | $I_3\ I_2\ I_1\ I_0$ | 1 | 1 | AC ← $I_3\ I_2\ I_1\ I_0$ | Load AC with contents of immediate data field ($I_3\ I_2\ I_1\ I_0$). | ZF | * |
| S | Store AC to M | 0 0 0 0 | 0 0 1 0 | 1 | 1 | M (DP) ← (AC) | Copy contents of AC to M (DP). | | |
| L | Load AC from M | 0 0 1 0 | 0 0 0 1 | 1 | 1 | AC ← [M (DP)] | Copy contents of M (D) to AC. | ZF | |
| [Data pointer manipulation instructions] | | | | | | | | | |
| LDZ data | Load $DP_H$ with zero and $DP_L$ with immediate data respectively | 1 0 0 0 | $I_3\ I_2\ I_1\ I_0$ | 1 | 1 | $DP_H$ ← 0<br>$DP_L$ ← $I_3\ I_2\ I_1\ I_0$ | Clear $DP_H$ to zero and copy contents of immediate data field ($I_3\ I_2\ I_1\ I_0$) to $DP_L$. | | |
| LHI data | Load $DP_H$ with immediate data | 0 1 0 0 | 0 0 $I_1\ I_0$ | 1 | 1 | $DP_H$ ← $I_1\ I_0$ | Copy contents of immediate data field ($I_1\ I_0$) to $DP_H$. | | |
| IND | Increment $DP_L$ | 1 1 1 0 | 1 1 1 0 | 1 | 1 | $DP_L$ ← ($DP_L$) + 1 | Add one to $DP_L$. | ZF | |
| DED | Decrement $DP_L$ | 1 1 1 0 | 1 1 1 1 | 1 | 1 | $DP_L$ ← ($DP_L$) – 1 | Subtract one from $DP_L$. | ZF | |
| TAL | Transfer AC to $DP_L$ | 1 1 1 1 | 0 1 1 1 | 1 | 1 | $DP_L$ ← (AC) | Copy contents of AC to $DP_L$. | | |
| TLA | Transfer $DP_L$ to AC | 1 1 1 0 | 1 0 0 1 | 1 | 1 | AC ← ($DP_L$) | Copy contents of $DP_L$ to AC. | ZF | |
| [Jump and subroutine instructions] | | | | | | | | | |
| JMP addr | Jump | 0 1 1 0<br>$P_7\ P_6\ P_5\ P_4$ | 1 0 $P_9\ P_8$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | PC ← $P_9\ P_8\ P_7\ P_6$ $P_5\ P_4\ P_3\ P_2$ $P_1\ P_0$ | Jump to address in immediate data field ($P_9\ P_8\ P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$). | | |
| CZP addr | Call subroutine in the zero page | 1 0 1 1 | $P_3\ P_2\ P_1\ P_0$ | 1 | 1 | STACK ← (PC) + 1<br>$PC_9$ to $PC_6$, $PC_1$, $PC_0$ ← 0<br>$PC_5$ to $PC_2$ ← $P_3\ P_2\ P_1\ P_0$ | Call subroutine in zero page. | | |
| CAL addr | Call subroutine | 1 0 1 0<br>$P_7\ P_6\ P_5\ P_4$ | 1 0 $P_9\ P_8$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | STACK ← (PC) + 2<br>$P_9$ to $P_0$ ← 0<br>$P_9\ P_8\ P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$ | Call subroutine. | | |
| RT | Return from subroutine | 0 1 1 0 | 0 0 1 0 | 1 | 1 | PC ← (STACK) | Return from subroutine. | | |
| [Branch instructions] | | | | | | | | | |
| BAt addr | Branch on AC bit | 0 1 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 0 1 $t_1\ t_0$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0$ ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if ACt = 1 | Branch to specified address in same page ($P_7$ to $P_0$) if bit specified by immediate data $t_1\ t_0$ in AC is one. | | The mnemonic includes decimal equivalent t of immediate data i.e., BA0 to BA3. |
| BNAt addr | Branch on no AC bit | 0 0 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 0 0 $t_1\ t_0$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0$ ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if ACt = 0 | Branch to specified address in same page ($P_7$ to $P_0$) if bit specified by immediate data $t_1\ t_0$ in AC is zero. | | The mnemonic includes decimal equivalent t of immediate data i.e., BNA0 to BNA3. |
| BMt addr | Branch on M bit | 0 1 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 0 1 $t_1\ t_0$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0$ ← $P_7\ P_6\ P_5\ P_4$ $P_3\ P_2\ P_1\ P_0$ if [M (DP, $t_1\ t_0$)] = 1 | Branch to specified address in same page ($P_7$ to $P_0$) if bit specified by immediate data $t_1\ t_0$ in M (DP) is one. | | The mnemonic includes decimal equivalent t of immediate data i.e., BM0 to BM3. |

Note: * The second and subsequent repetitions of an LI or CLA instruction produce the same effects as an NOP instruction.

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| Mnemonic | | Instruction code | | Number of bytes | Number of cycles | Operation | Description | Affected status bits | Note |
|---|---|---|---|---|---|---|---|---|---|
| | | $D_7\ D_6\ D_5\ D_4$ | $D_3\ D_2\ D_1\ D_0$ | | | | | | |
| [Branch instructions] | | | | | | | | | |
| BNMt addr | Branch on no M bit | 0 0 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 0 1 $t_1$ $t_0$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if [M (DP, $t_1\ t_0$)]<br>= 0 | Branch to specified address in same page ($P_7$ to $P_0$) if bit specified by immediate data $t_1\ t_0$ in M (DP) is zero. | | The mnemonic includes decimal equivalent t of immediate data i.e., BNM0 to BNM3. |
| BPt addr | Branch on port bit | 0 1 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 0 $t_1$ $t_0$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if [P ($DP_L$, $t_1\ t_0$)]<br>= 1 | Branch to specified address in same page ($P_7$ to $P_0$) if bit specified by immediate data $t_1\ t_0$ in P ($DP_L$) is one. | | The mnemonic includes decimal equivalent t of immediate data i.e., BP0 to BP3. |
| BNPt addr | Branch on no port bit | 0 0 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 0 $t_1$ $t_0$<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if [P ($DP_L$, $t_1\ t_0$)]<br>= 0 | Branch to specified address in same page ($P_7$ to $P_0$) if bit specified by immediate data $t_1\ t_0$ in P ($DP_L$) is zero. | | The mnemonic includes decimal equivalent t of immediate data i.e., BNP0 to BNP3. |
| BTM addr | Branch on timer | 0 1 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 1 0 0<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if TMF = 1<br>then TMF ← 0 | Branch to specified address in same page ($P_7$ to $P_0$)<br>if TMF is one. Clear TMF to zero. | TMF | |
| BNTM addr | Branch on no timer | 0 0 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 1 0 0<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if TMF = 0<br>then TMF ← 0 | Branch to specified address in same page ($P_7$ to $P_0$)<br>if TMF is zero. Clear TMF to zero. | TMF | |
| BC addr | Branch on CF | 0 1 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 1 1 1<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if CF = 1 | Branch to specified address in same page ($P_7$ to $P_0$)<br>if CF is one. | | |
| BNC addr | Branch on no CF | 0 0 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 1 1 1<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if CF = 0 | Branch to specified address in same page ($P_7$ to $P_0$)<br>if CF is zero. | | |
| BZ addr | Branch on ZF | 0 1 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 1 1 0<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if ZF = 1 | Branch to specified address in same page ($P_7$ to $P_0$)<br>if ZF is one. | | |
| BNZ addr | Branch on no ZF | 0 0 1 1<br>$P_7\ P_6\ P_5\ P_4$ | 1 1 1 0<br>$P_3\ P_2\ P_1\ P_0$ | 2 | 2 | $PC_7$ to $PC_0 \leftarrow$<br>$P_7\ P_6\ P_5\ P_4$<br>$P_3\ P_2\ P_1\ P_0$<br>if ZF = 0 | Branch to specified address in same page ($P_7$ to $P_0$)<br>if ZF is zero. | | |
| [I/O instructions] | | | | | | | | | |
| IP | Input port to AC | 0 0 0 0 | 1 1 0 0 | 1 | 1 | AC ← [P ($DP_L$)] | Copy contents of port specified by P ($PD_L$) to AC. | ZF | |
| OP | Output AC to port | 0 1 1 0 | 0 0 0 1 | 1 | 1 | P ($DP_L$) ← (AC) | Copy contents of AC to port specified by P ($DP_L$). | | |
| SPB bit | Set port bit | 0 0 0 0 | 0 1 $B_1\ B_0$ | 1 | 2 | P ($DP_L$, $B_1\ B_0$) ← 1 | Set bit specified by immediate data $B_1\ B_0$ in port specified by P ($DP_L$) to one. | | Execution of this instruction invalidates contents of E. |
| RPB bit | Reset port bit | 0 0 1 0 | 0 1 $B_1\ B_0$ | 1 | 2 | P ($DP_L$, $B_1\ B_0$) ← 0 | Clear bit specified by immediate data $B_1\ B_0$ in port specified by P ($DP_L$) to zero. | ZF | Execution of this instruction invalidates contents of E. |
| [Other instructions] | | | | | | | | | |
| WTTM | Write timer | 1 1 1 1 | 1 0 0 1 | 1 | 1 | TM ← (E), (AC)<br>TMF ← 0 | Copy contents of E and AC to timer. Clear TMF to zero. | TMF | |
| HALT | Halt | 1 1 1 1 | 0 1 1 0 | 1 | 1 | Halt | Suspend all operations. | | Execution requires that pin PA3 be high. |
| NOP | No operation | 0 0 0 0 | 0 0 0 0 | 1 | 1 | No operation | Do nothing but consume one machine cycle. | | |

### The above subset excludes the following instructions from the LC6523, 6526 set

AND, BFn, BI, BNFn, BNI, CLI, JPEA, OR, RAL, RCTL, RFB, TRI, RTBL, SCTL, SFB, X, XAH, XA0, XA1, XA3, XD, XH0, XH1, XI, XL0, XL1, and XM.

### Specifying LC6529N/F/L User Options

Specifying (Ordering) LC6529N/F/L User Options

When developing the software or ordering the chip, the user must prepare an EPROM containing the user program, user option data, and fixed data. There are two ways of preparing these last two: with software provided by Sanyo and manually. This Section discusses both methods.

Using Sanyo's Option Specification Software

SU60K, the software for specifying LC6529 options, interactively asks the user to specify the options and writes the results to a mask option file, file.OPT.

The M60K macro assembler assembles the user program into an object file, file.OBJ.

The L60K linker merges the mask option and object files to create an EVA file, file.EVA.

The EVA2HEX conversion tool converts the user program and mask options inside the EVA file to an object file in hexadecimal (HEX) format.

The user use a PROM writer to download this HEX file to the EPROM submitted when ordering the chip.

For further details, see Figure A below and refer to the LC65/66K Software Manual.

Alternate Method

1. Overview
   If not using the software for specifying LC6529 options, the user must list the mask options using the coding procedures described below and then write these with the program to the EPROM regions shown in Figure A.
   When ordering, the user must submit an option table list as well as the EPROM. Figure B gives an example of such a list.
   The procedures for coding the mask options appear on the pages following Figure B.

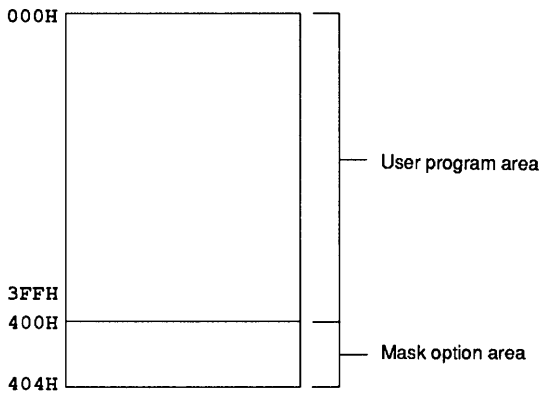


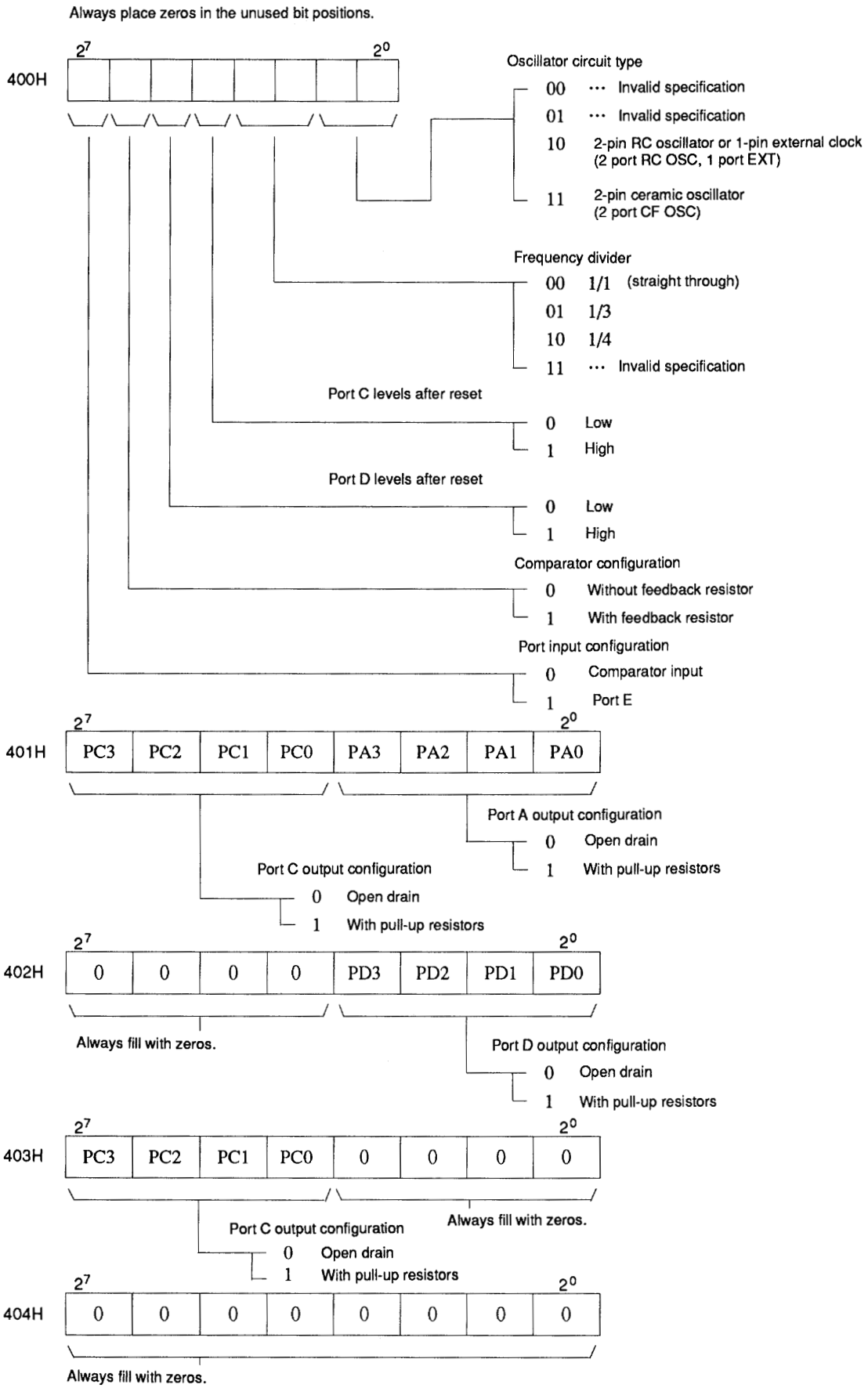

**Figure A LC6529 ROM Data**

2. Sample option table list

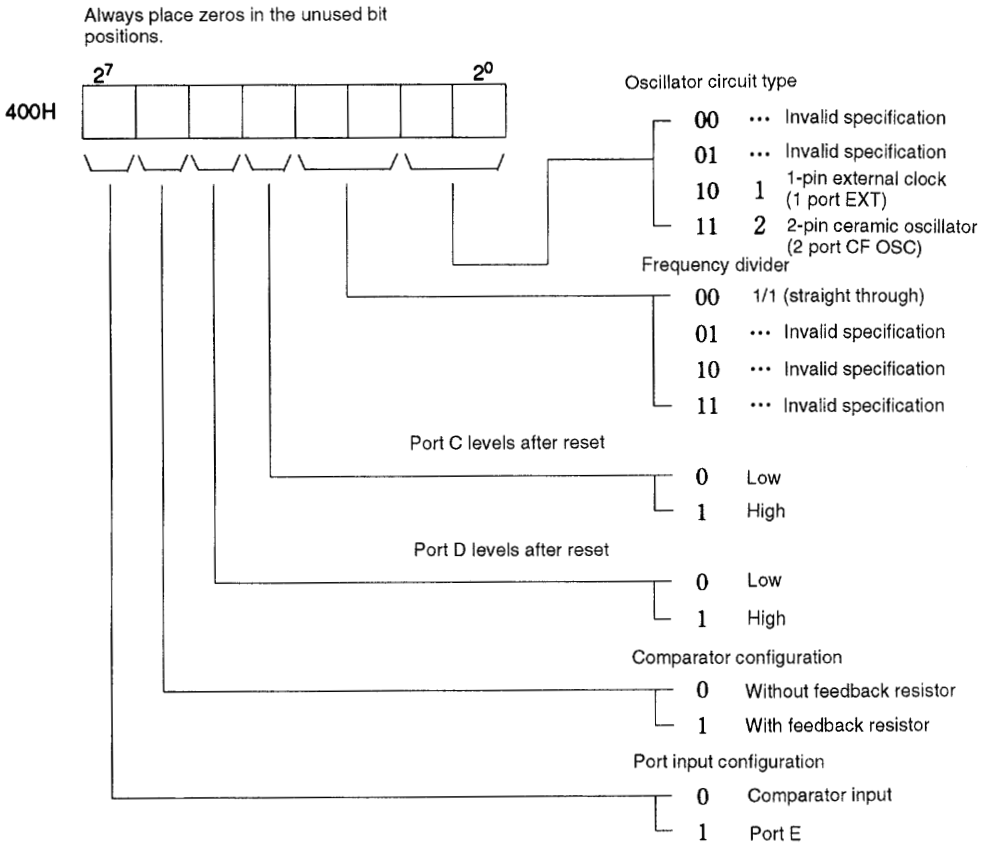
```
****************************** LC6529F MASK OPTION 1.XXX ******************************
                [FILE NAME]         L:SAMPLE.OPT          (94/11/11)          ver.1.xxx
                [COMMENTS]

OSC OPTION                                                  OSC DIVIDER
--------------------------                                  --------------------------
1 EXT       2 RC       2 CF                                  1/1        1/3        1/4
.....       ....       ****                                  ***        ...        ...

OUTPUT  LEVEL  AT RESET                     PORT  INPUT  OPTION
--------------------------                  ----------------------------------------
            HIGH        LOW                 COMP & FB           COMP           PORT E
PORT C      ****        ...                 .........           ****           ......
PORT D      ....        ***

PORT A MASK OPTION                          PORT C MASK OPTION
----------------------------------------    ----------------------------------------
            PULL UP           OPEN DRAIN                PULL UP           OPEN DRAIN
BIT0        *******           ..........    BIT0        .......           **********
BIT1        .......           **********    BIT1        *******           ..........
BIT2        *******           ..........    BIT2        .......           **********
BIT3        .......           **********    BIT3        *******           ..........

PORT D MASK OPTION
----------------------------------------
            PULL UP           OPEN DRAIN
BIT0        *******           ..........
BIT1        .......           **********
BIT2        *******           ..........
BIT3        .......           **********
```

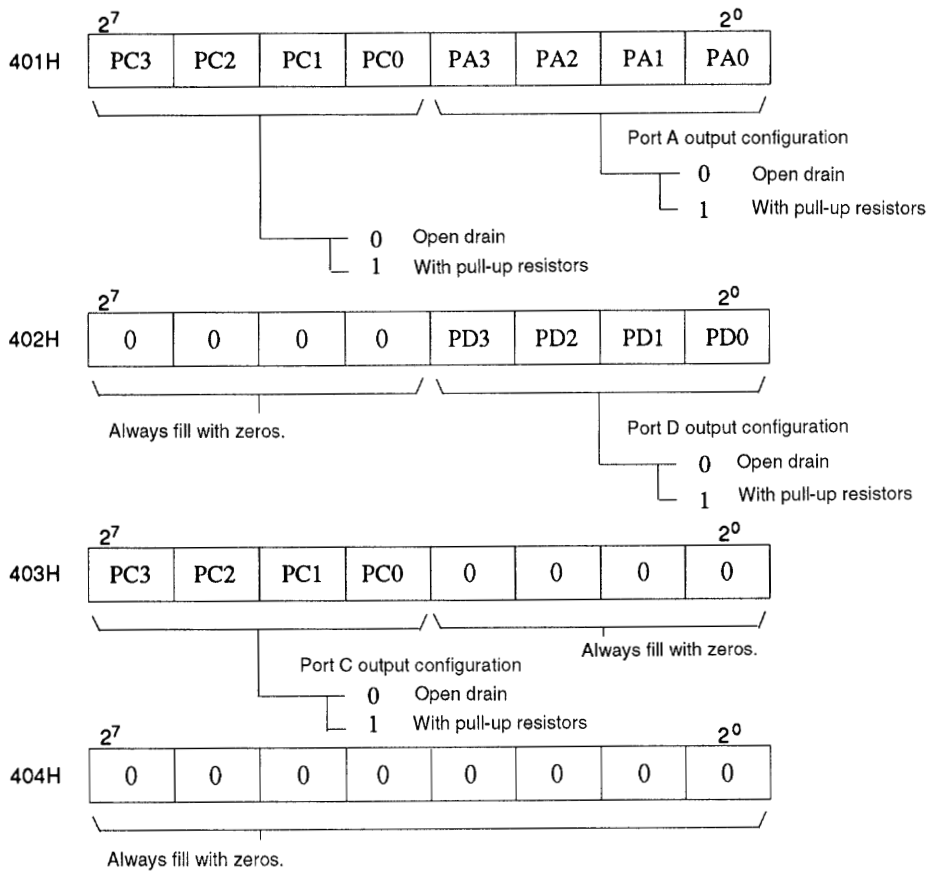
**Figure B  Sample Option Table List**

## Coding LC6529N/L Mask Options



## Coding LC6529F Mask Options



## Using Standby HALT Mode

The LC6529N/F/L features a convenient HALT mode that reduces current drain while the chip is on standby.
These standby functions involve the use of one instruction (HALT) and two control signal pins (PA3 and $\overline{\text{RES}}$). For the functions to work properly, the design of external circuits and chip software must pay due attention to these three. Depending on how extensively the standby functions are used, the designer must consider and provide countermeasures that protect the design from the effects of power supply fluctuations, power interruptions, external noise, and other adverse conditions.
This document discusses the circuit and program design issues related to the most frequent application of the standby functions, the detection and recovery from power outages.
When using the standby functions, follow the sample circuits given in this document and carefully observe all warnings accompanying them.
Departures from the design guidelines herein will warrant thorough testing and evaluation of the effects of such sudden changes in the operating environment as momentary power outages on application operation.

1. Entering and leaving the HALT mode
   Table 1 gives the conditions for entering and leaving the HALT mode.

### Table 1 Entering and Leaving the HALT Mode

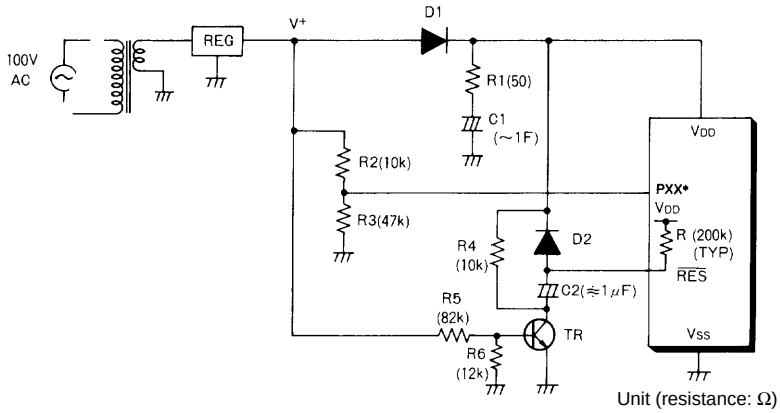
| Entering HALT mode | Leaving HALT mode |
|---|---|
| HALT instruction while PA3 is high. | 1. Reset signal ($\overline{\text{RES}}$ pin pulled low.)<br>2. PA3 pulled low. |

Note: The second method for leaving the HALT mode is only available when the design uses an RC oscillator circuit. It may not work properly with a ceramic oscillator circuit.

2. Important notes
   Using the standby functions requires close attention to the following issues in application circuit and software design.
   - The power supply voltage must not fall below the rating while the chip is on standby.
   - Carefully observe all timing restrictions for the control signals during transitions to and from the HALT mode.
   - Make sure that a signal for leaving the HALT mode does not overlap the execution of the HALT instruction.

   This document demonstrates how to observe these restrictions by discussing both application circuits for a power failure recovery function and programming considerations.
   Such a power failure recovery function detects failure of the main power supply and causes the chip to execute a HALT instruction to put itself on standby. Reducing the current drain this way allows the backup capacitor to maintain the register contents for a longer period than otherwise possible. When the power is restored, the chip is reset and automatically resumes execution with the program counter set to 000H. The following examples discuss how the software can then distinguish this type of reset from a power on reset sequence along with issues related to dealing with momentary AC power outages.

   - Example 1
     The first example does not distinguish a power-on reset sequence from a reset trigger by a power failure.
     — Circuit diagram
       Figure 2-1 gives the circuit diagram for this sample circuit.

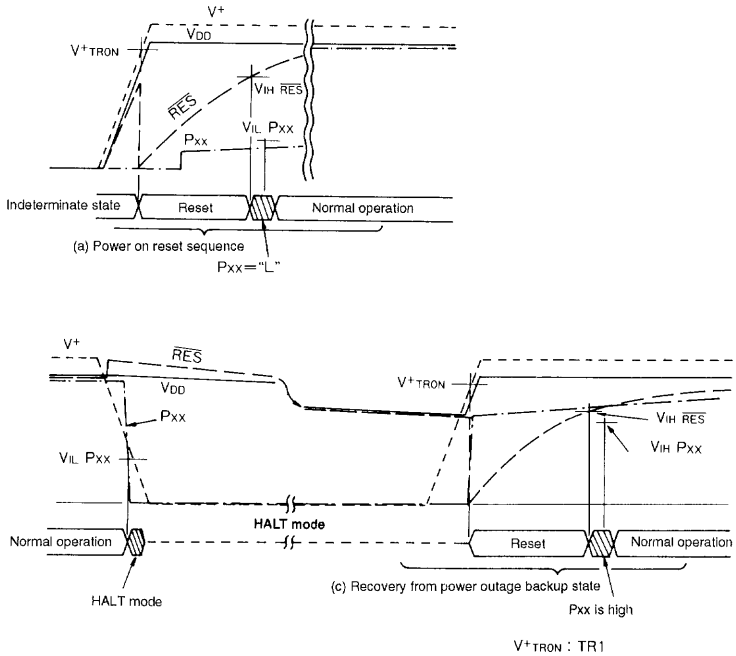



Note: All ports other than PA3 are configured as normal input ports.

**Figure 2-1 Power Outage Backup Example 1**

— Waveforms during operation

Figure 2-2 gives the waveforms relevant to the operation of the above circuit. There are three main states: (a) power-on reset sequence, (b) momentary break in main power supply, and (c) recovery from power outage backup state.




Note: $V^{+}_{TRON}$ = $V^{+}$ level at which transistor switches on and off

**Figure 2-2 Waveforms Relevant to Operation of Circuit Example 1**

— Main circuit states
  a: Power-on reset sequence
  Once the power supply voltage has reached the proper level, the chip automatically resets and begins execution with the program counter set to $000_H$.
  Caution: This circuit does not reset the chip until the power supply voltage is within the range specified for $V_{DD}$, so leaves the chip in an indeterminate state.
  b: Momentary break in main power supply
    i. If only the $\overline{RES}$ pin and none of the Pxx pins drops below the threshold level $V_{IL}$, the chip resets and repeats the power-on reset sequence.
    ii. If the $\overline{RES}$ pin and the Pxx pins remain above the threshold level $V_{IL}$, the chip continues normal execution.
    iii. If both the $\overline{RES}$ pin and the Pxx pins drop below the threshold level $V_{IL}$, the chip resets if two consecutive polls fail to detect a low at Pxx or, if a low is found, enters the HALT mode and then, because the power has been restored, leaves the HALT mode.
  c: Recovery from power outage backup state
  Since the power has been restored, the chip leaves the HALT mode.

— Design considerations
  a: $V^+$ rise time and C2
  The $V^+$ rise time must be approximately ten times the RC constant for the reset circuit, $C2 \times R$, where R is the internal resistance (typ. 200 kΩ). It must also be no longer than approximately 20 ms.
  b: R1 and C1 values
  R1 must be as small as possible; C1, as large as possible to provide the longest backup time. At the same time, however, R1 must be large enough such that the C1 charging current does not exceed the power supply capacity.
  c: R2 and R3 values
  Choose these to make the Pxx high levels equal to $V_{DD}$.
  d: R4 value
  Select R4 and thus the RC constant for C2 and R4 so that C2 discharges sometime in the interval between the point at which $V^+$ falls below $V^+_{TRON}$ (turning off the transistor) and the point at which Pxx falls below $V_{IL}$. (Otherwise, the chip will enter the HALT mode and then not respond to a reset.)
  e: R5 and R6 values
  Select R5 and R6 so that $V^+$ when the reset circuit operates, switching on the transistor (that is, when R5 and R6 produce a $V_{BE}$ of approximately 0.6 V) is at least the minimum operating voltage ($V_{DD}$) plus the $V_F$ for diode D1. To provide a rapid reset once the power is restored, however, keep this voltage as small as possible while still satisfying these conditions.
  f: Calculating backup time
  From the time that the chip detects the power outage at Pxx until it executes the HALT instruction, the chip operates normally so drains relatively large amounts of current. C1 must therefore be large enough to provide backup power not only for the set's backup period, but for this transitional period as well.

— Software considerations
  a: Assign signals so that PA3 is maintained high during standby operation.
  b: The software should double-check a standby request by polling twice.
  Example:

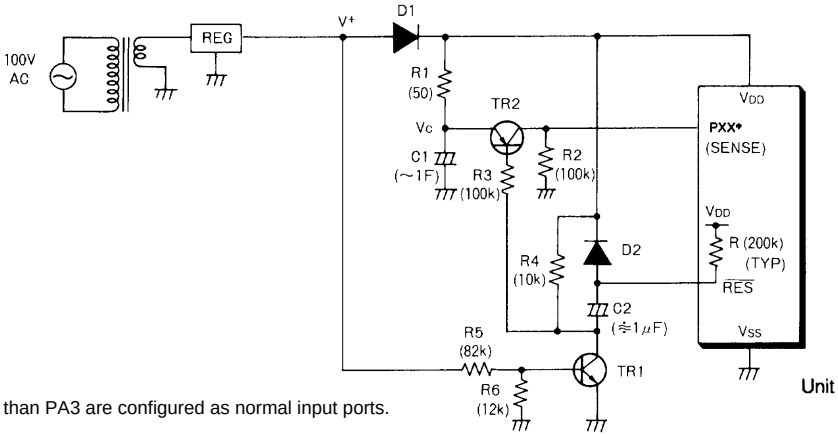
```
                ⋮
        BP1     AAA     : Poll once
        BP1     AAA     : Poll twice
        HALT            : Begin standby operation
AAA :   ⋮
```

- Example 2

  The second example distinguishes a power-on reset sequence from a reset trigger by a power failure.

  — Circuit diagram

  Figure 2-3 gives the circuit diagram for this sample circuit.

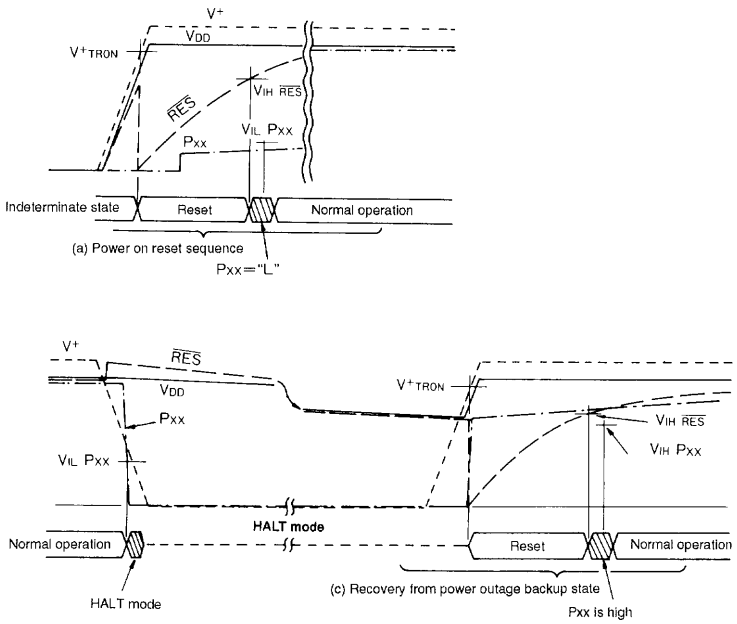



Note: All ports other than PA3 are configured as normal input ports.

**Figure 2-3 Power Outage Backup Example 2**

— Waveforms during operation

Figure 2-4 gives the waveforms relevant to the operation of the above circuit. There are two main states: (a) power-on reset sequence and (b) recovery from power outage backup state.




Note: $V^{+}_{TRON}$ = $V^{+}$ level at which transistor switches on and off

**Figure 2-4 Waveforms Relevant to Operation of Circuit Example 2**

— Main circuit states

a: Power-on reset sequence
The operation and points to watch are the same as for the first example. The only difference is that the software interprets a low at Pxx as indicating an initial reset.

b: Switch to standby operation
The chip polls Pxx and, if it is low, enters the HALT mode.

c: Recovery from power outage backup state
Since the power has been restored, the chip leaves the HALT mode. If the recovery routine then finds that Pxx is high, it switches to a separate routine for restarting after a power outage.
Caution: If the power supply voltage $V_{DD}$ drops below the $V_{IH}$ level for Pxx during the outage, this recovery routine will subsequently find that Pxx is low and execute the routine for an initial reset instead.

— Design considerations

a: R2 and R3 values
Make R2 much greater than R1 and choose R3 to limit TR2's $I_B$.

b: R4 value
Since there are no momentary outages, the value is not critical, but select R4 so that C2 quickly discharges.
In all other respects, the same considerations apply as in Example 1.

— Software considerations

a: Assign signals so that PA3 is maintained high during standby operation.

b: The software should check for a standby request by polling once.
Example:

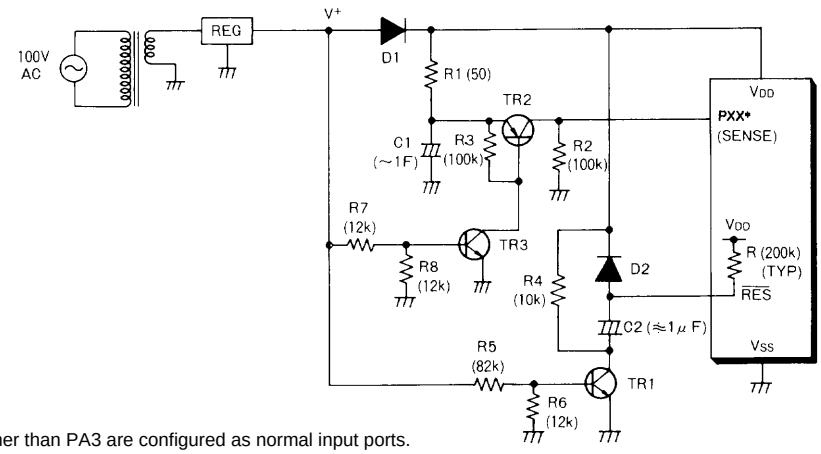
```
                ⋮
        BP1     AAA     : Poll port
        HALT            : Begin standby operation
AAA :   ⋮
```

• Example 3

The third example adds support for momentary power outages.

— Circuit diagram

Figure 2-5 gives the circuit diagram for this sample circuit.



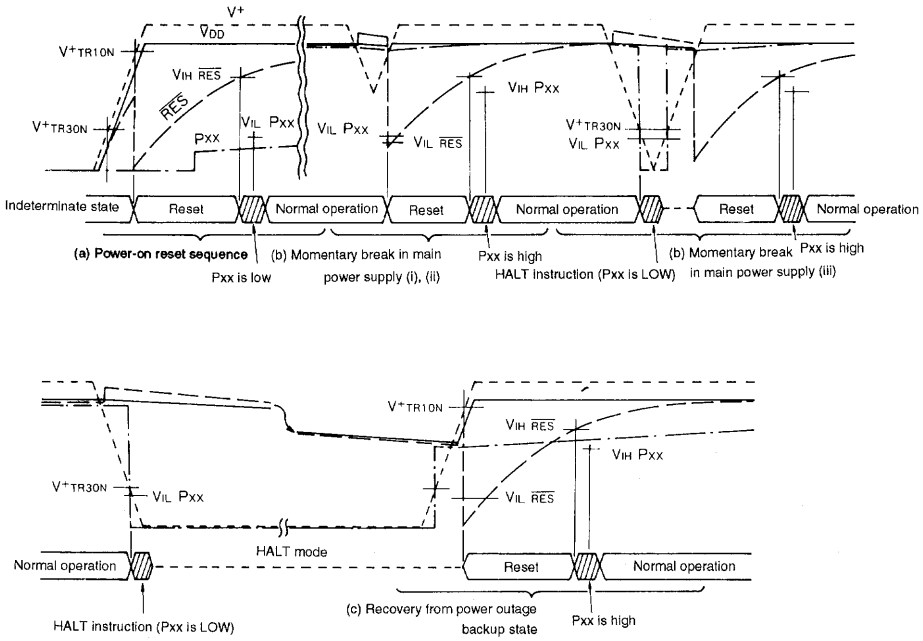

Note: All ports other than PA3 are configured as normal input ports.

Unit (resistance: Ω)

**Figure 2-5 Power Outage Backup Example 3**

— Waveforms during operation

Figure 2-5 gives the waveforms relevant to the operation of the above circuit. There are three main states: (a) power-on reset sequence, (b) momentary break in main power supply, and (c) recovery from power outage backup state.




Note: $V^+_{TR1ON}$ = $V^+$ level at which transistor TR1 switches on and off
$V^+_{TR3ON}$ = $V^+$ level at which transistor TR3 switches on and off

**Figure 2-5 Waveforms Relevant to Operation of Circuit Example 3**

— Main circuit states

a: Power-on reset sequence
The operation and points to watch are the same as for the second example.

b: Momentary break in main power supply

i. If only the $\overline{RES}$ pin and none of the Pxx pins drops below the threshold level $V_{IL}$, the chip resets. If the recovery routine then finds that Pxx is high, it switches to a separate routine for restarting after a power outage.

ii. If the $\overline{RES}$ pin and the Pxx pins remain above the threshold level $V_{IL}$, the chip continues normal execution.

iii. If both the $\overline{RES}$ pin and the Pxx pins drop below the threshold level $V_{IL}$, the chip resets if two consecutive polls fail to detect a low at Pxx or, if a low is found, enters the HALT mode and then, because the power has been restored, leaves the HALT mode. If the recovery routine then finds that Pxx is high, it switches to a separate routine for restarting after a power outage.

c: Recovery from power outage backup state
The operation and points to watch are the same as for the second example.

— Design considerations

a: R3 value
This serves as the bias resistor for transistor TR2.

b: R7 and R8 values
Select these so that transistor TR3 switches on and off at approximately 1.5 V.
In all other respects, the same considerations apply as in Example 1.

— Software considerations

The same considerations apply as in Example 1.