



LC72314W, 72315W, 72316W

Ultralow-Voltage ETR Controller with On-Chip LCD Driver

Preliminary

Overview

The LC72314W, LC72315W and LC72316W are ultralow-voltage (0.9 to 1.8 V) electronic tuning microcontrollers that include a PLL that operates up to 250 MHz and a 1/4 duty 1/2 bias LCD driver on chip. This IC includes an on-chip DC-DC converter that can easily create the power supply voltages needed for electronic tuning and contribute to reducing end product costs. This IC is optimal for portable audio equipment that must operate from a single battery.

Function

- Program memory (ROM):
 - 4096 × 16 bits (8K bytes) : LC72314W
 - 6144 × 16 bits (12K bytes): LC72315W
 - 8192 × 16 bits (16K bytes): LC72316W
- Data memory (RAM):
 - 256 × 4 bits: LC72314W
 - 512 × 4 bits: LC72315W/72316W
- Cycle time: 40 μs (all 1-word instructions)
- Stack: 8 levels
- LCD driver:
 - 48 to 112 segments (1/4 duty, 1/2 bias drive)
- Interrupts: Two external interrupts
 - Timer interrupts (1, 5, 10, and 50 ms)
- A/D converter: Four input channels
 - (6-bit successive approximation conversion)
- Input ports: 11 ports (of which three can be switched for use as A/D converter inputs)
- Output ports: 8 ports (of which 1 can be switched for use as the beep tone output and 4 are open-drain ports)
- I/O ports: 29 ports (of which 16 can be switched for use as LCD ports and as mask options, of which 3 can be switched for use as serial I/O ports)

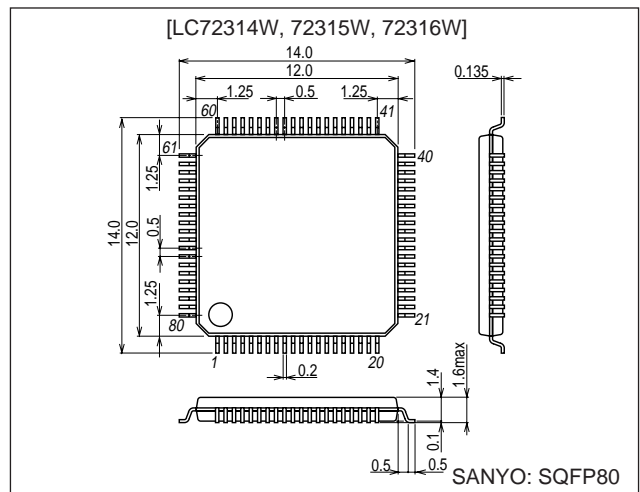
- Serial I/O: One system (LC72315W/72316W)
- PLL: Reference frequencies:
 - 1, 3, 3.125, 5, 6.25, 12.5, and 25 kHz
- Input frequencies:
 - FM band: 10 to 250 MHz
 - AM band (high): 2 to 20 MHz
 - AM band (low): 0.5 to 10 MHz
- Input sensitivity: FM band:
 - 35 mVrms (130 MHz to 250 MHz: 50 mVrms)
 - AM band (high, low): 35 mVrms
- IF counter: HCTR input pin 0.4 to 15 MHz (35 mVrms)
- External reset input: During CPU and PLL operations, instruction execution is started from location 0.

Continued on next page.

Package Dimensions

unit: mm

3220-SQFP80



■ Any and all SANYO products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your SANYO representative nearest you before using any SANYO products described or contained herein in such applications.

■ SANYO assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO products described or contained herein.

SANYO Electric Co., Ltd. Semiconductor Company

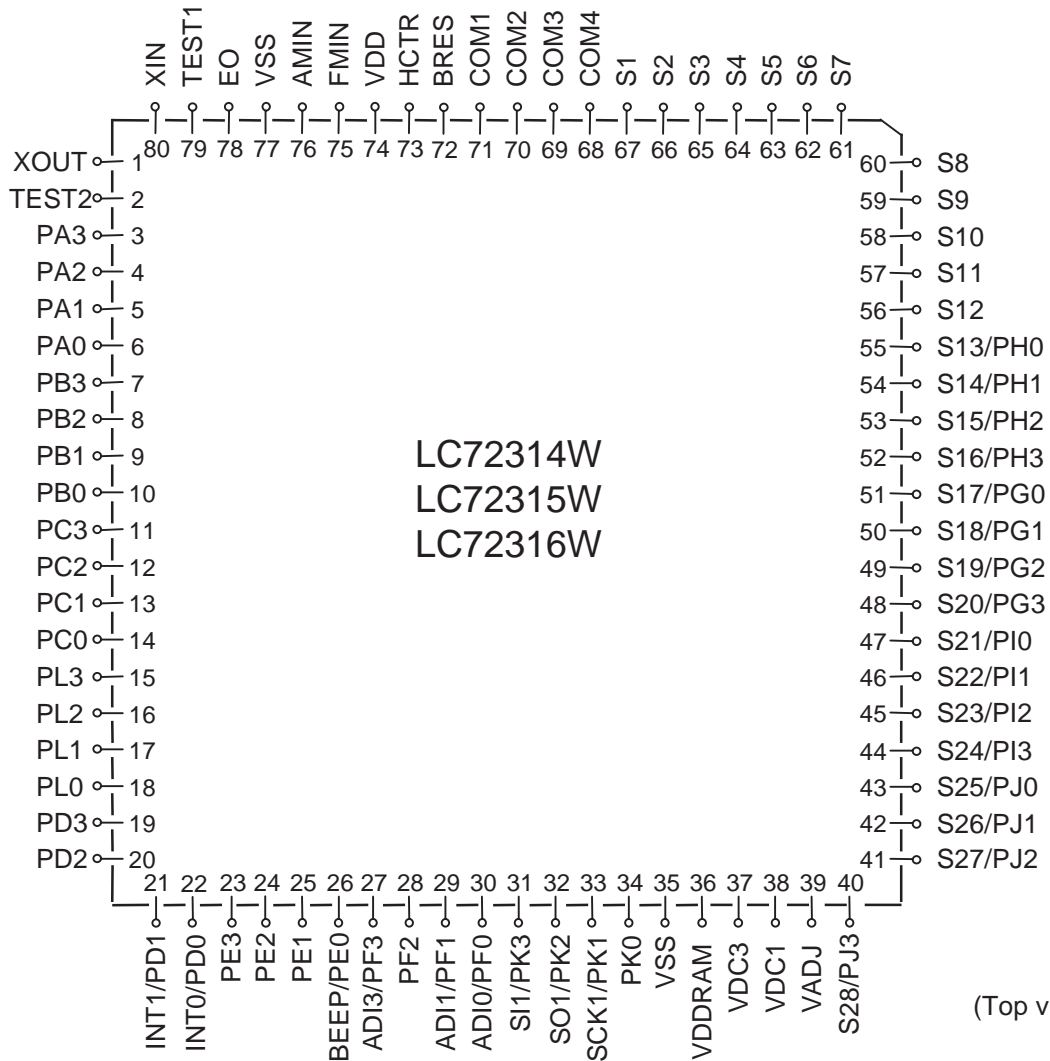
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

LC72314W, 72315W, 72316W

Continued from preceding page.

- Built-in power-on reset circuit:
The CPU starts execution from location 0 when power is first applied.
- Halt mode: The controller-operating clock is stopped.
- Backup mode: The crystal oscillator is stopped.
- Static power-on function:
Backup state is cleared with the PF port
- Beep tone: 1.5 and 3.1 kHz
- Built-in DC-DC converter:
For LCD and A/D converter use (3 V)
Can also be used for TU + B creation by using a secondary coil.
- Built-in remaining battery life verification function:
Converts the V_{DD} pin level to digital.
- Memory retention voltage: 0.8 V or higher
- Dedicated memory power supply: The RAM retention time has been increased by the provision of a dedicated memory power supply.
- Package: SQFP-80 (0.5-mm pitch)
- V_{DD} power supply: 0.9 to 1.8 V
- Operating frequency: 75 kHz

Pin Assignment



LC72314W, 72315W, 72316W

Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$, $V_{SS} = 0\text{ V}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{DD1\text{ max}}$	V_{DD}	-0.3 to +3.0	V
	$V_{DD3\text{ max}}$	$V_{DD\text{RAM}}$	-0.3 to +4.0	V
	$V_{DD4\text{ max}}$	VDC3	-0.3 to +4.0	V
Input voltage	V_{IN1}	FMIN, AMIN, HCTR	-0.3 to $V_{DD1} + 0.3$	V
	V_{IN2}	PA, PC, PD, PF, PG, PH, PI, PJ, PL, BRES	-0.3 to $V_{DD1} + 0.3$	V
Output voltage	V_{OUT1}	PE	-0.3 to +7	V
	V_{OUT2}	PB, PC, PD, PG, PH, PI, PJ, PK, PL	-0.3 to $V_{DD1} + 0.3$	V
	V_{OUT3}	VDC1, EO	-0.3 to $V_{DD4} + 0.3$	V
	V_{OUT4}	COM1 to COM4, S1 to S28	-0.3 to $V_{DD4} + 0.3$	V
Output current	I_{OUT1}	PC, PD, PG, PH, PI, PJ, PK, PL, EO	0 to 3	mA
	I_{OUT2}	PB	0 to 1	mA
	I_{OUT3}	PE	0 to 2	mA
	I_{OUT4}	S1 to S28	300	μA
	I_{OUT5}	COM1 to COM4	3	mA
Allowable power dissipation	P_{dmax}	$T_a = -10$ to $+60^\circ\text{C}$	100	mW
Operating temperature	T_{opr}		-10 to +60	$^\circ\text{C}$
Storage temperature	T_{stg}		-45 to +125	$^\circ\text{C}$

Allowable Operating Ranges at $T_a = -10$ to $+60^\circ\text{C}$, $V_{DD} = 0.9$ to 1.8 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD1}	Voltage applied to the V_{DD} pin	0.9	1.3	1.8	V
	V_{DD3}	Voltage applied to the $V_{DD\text{RAM}}$ pin	2.7	3.0	3.3	
	V_{DD4}	Voltage applied to the VDC3 pin	2.7	3.0	3.3	
	V_{DD5}	Memory retention voltage	0.8			
Input high-level voltage	V_{IH1}	Ports PC, PD, PG, PH, PI, PJ, PK, and PL	$0.7 V_{DD1}$		V_{DD1}	V
	V_{IH2}	Port PA	$0.8 V_{DD1}$		V_{DD1}	V
	V_{IH3}	Port PF	$0.8 V_{DD1}$		V_{DD1}	V
	V_{IH4}	Port BRES	$0.6 V_{DD1}$		V_{DD1}	V
Input low-level voltage	V_{IL1}	Ports PC, PD, PG, PH, PI, PJ, PK, and PL	0		$0.3 V_{DD1}$	V
	V_{IL2}	Port PA	0		$0.2 V_{DD1}$	V
	V_{IL3}	Port PF	0		$0.2 V_{DD1}$	V
	V_{IL4}	Port BRES	0		$0.2 V_{DD1}$	V
Input amplitude	V_{IN1}	XIN	0.5		0.6	Vrms
	V_{IN2}	FMIN, AMIN, HCTR: $V_{DD1} = 0.9$ to 1.8 V	0.035		0.35	Vrms
	V_{IN3}	FMIN: $V_{DD1} = 0.9$ to 1.8 V	0.05		0.35	Vrms
Input voltage range	V_{IN4}	ADI0, ADI1, ADI3, V_{DD1}	0		V_{DD4}	V
Input frequency	F_{IN1}	XIN: $C_I \leq 35\text{ k}\Omega$	70	75	80	kHz
	F_{IN2}	FMIN: V_{IN2} , $V_{DD1} = 0.9$ to 1.8 V	10		130	MHz
	F_{IN3}	FMIN: V_{IN3} , $V_{DD1} = 0.9$ to 1.8 V	130		250	MHz
	F_{IN4}	AMIN(L): V_{IN2} , $V_{DD1} = 0.9$ to 1.8 V	0.5		10	MHz
	F_{IN5}	AMIN(H): V_{IN2} , $V_{DD1} = 0.9$ to 1.8 V	2.0		20	MHz
	F_{IN5}	HCTR: V_{IN2} , $V_{DD1} = 0.9$ to 1.8 V	0.4		15	MHz

LC72314W, 72315W, 72316W

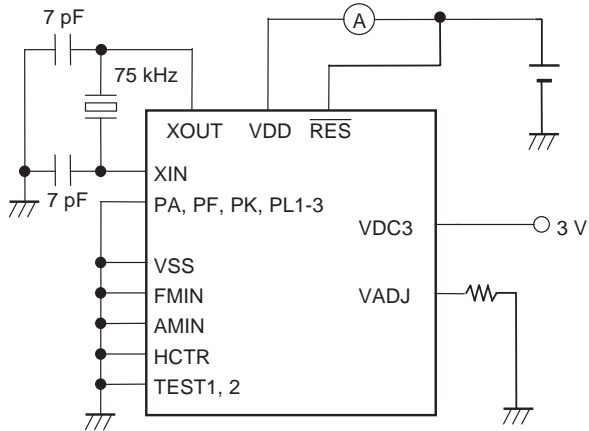
Electrical Characteristics under allowable operating conditions

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Input high-level current	I _{IH1}	XIN: V _{DD1} = 1.3 V			3	μA
	I _{IH2}	FMIN, AMIN, HCTR: V _{DD1} = 1.3 V	3	8	20	μA
	I _{IH3}	Port PF: V _{DD1} = 1.3 V			4	μA
	I _{IH4}	PA (without pull-down resistors), the PC, PD, PG, PH, PI, PJ, PK, and PL ports, and BRES: V _{DD1} = 1.3 V			3	μA
Input low-level current	I _{IL1}	XIN: V _{DD1} = V _{SS}			-3	μA
	I _{IL2}	FMIN, AMIN, HCTR: V _{DD1} = V _{SS}	-3	-8	-20	μA
	I _{IL3}	Port PF: V _{DD1} = V _{SS}			-4	μA
	I _{IL4}	PA (without pull-down resistors), the PC, PD, PG, PH, PI, PJ, PK, and PL ports, and BRES: V _{DD1} = V _{SS}			-3	μA
Input floating voltage	V _{IF}	PA (with pull-down resistors)			0.05 V _{DD1}	V
Pull-down resistor	R _{PD1}	PA/PF (with pull-down resistors), V _{DD1} = 1.3 V	75	100	200	kΩ
	R _{PD2}	TEST1, TEST2 (with pull-down resistors), V _{DD1} = 1.3 V		10		kΩ
Hysteresis	V _H	BRES	0.1 V _{DD1}	0.2 V _{DD1}		V
Output high-level voltage	V _{OH1}	PB: I _O = 1 mA	V _{DD1} – 0.3 V _{DD1}			V
	V _{OH2}	PC, PD, PG, PH, PI, PJ, PK, and PL: I _O = 1 mA	V _{DD1} – 0.3 V _{DD1}			V
	V _{OH3}	EO: I _O = 500 μA	V _{DD4} – 0.3 V _{DD4}			V
	V _{OH4}	XOUT: I _O = 1 μA	V _{DD1} – 0.3 V _{DD1}			V
	V _{OH5}	S1 to S28: I _O = 20 μA	V _{DD4} – 1			V
	V _{OH6}	COM1, COM2, COM3, COM4: I _O = 100 μA	V _{DD4} – 1			V
	V _{OH7}	VDC1: I _O = 1 mA	V _{DD4} – 1			V
Output low-level voltage	V _{OL1}	PB: I _O = -50 μA			0.3 V _{DD1}	V
	V _{OL2}	PC, PD, PE, PG, PH, PI, PJ, PK, and PL: I _O = -1 mA			0.3 V _{DD1}	V
	V _{OL3}	EO: I _O = -500 μA			0.3 V _{DD4}	V
	V _{OL4}	XOUT: I _O = -1 μA			0.3 V _{DD1}	V
	V _{OL5}	S1 to S28: I _O = -20 μA			V _{DD4} – 2	V
	V _{OL6}	COM1, COM2, COM3, COM4: I _O = -100 μA			V _{DD4} – 2	V
	V _{OL7}	PE: I _O = 2 mA			0.6 V _{DD1}	V
Output off leakage current	I _{OFF1}	Ports PB, PC, PD, PG, PH, PI, PJ, PK, PL, and EO	-3		+3	μA
	I _{OFF2}	Port PE	-100		+100	nA
A/D converter error		ADI0, ADI1, ADI3 V _{DD1}	-1/2		+1/2	LSB
Current drain	I _{DD1}	V _{DD1} = 1.3 V: F _{IN2} 130 MHz, T _a = 25°C		10	30	mA
	I _{DD2}	V _{DD1} = 1.3 V: In PLL stop mode, T _a = 25°C		0.15		mA
	I _{DD3}	V _{DD1} = 1.3 V: In HALT mode, T _a = 25°C *1		0.1		mA
	I _{DD4}	V _{DD1} = 1.8 V, with the oscillator stopped, T _a = 25°C *2		1		μA

Note*: The halt mode current drain is due to 20 instruction being executed every 125 ms.

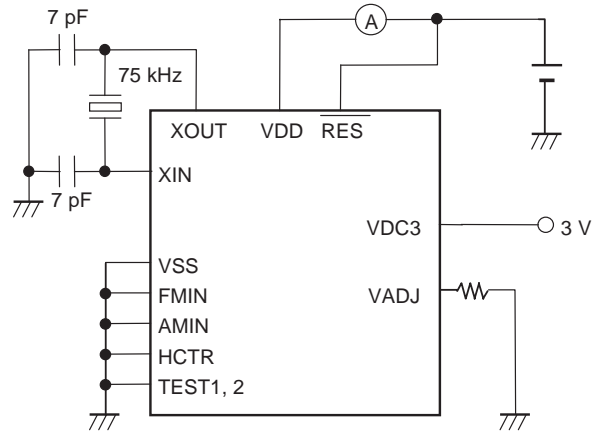
LC72314W, 72315W, 72316W

*1. Halt and PLL STOP mode current test circuit



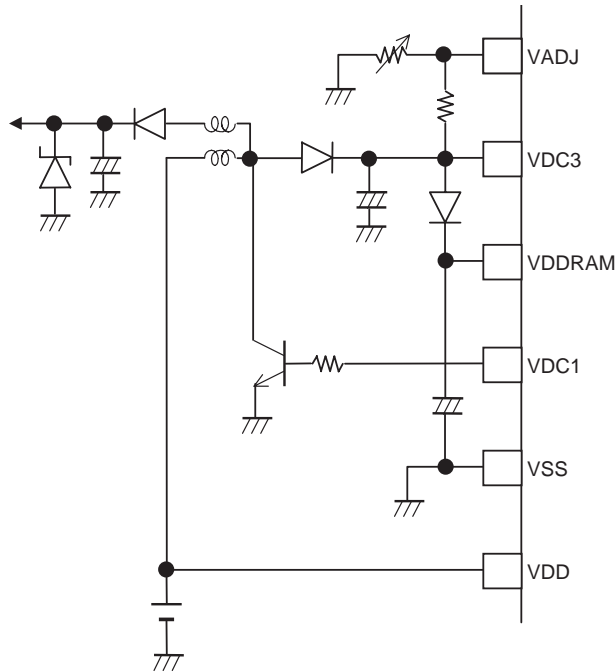
With all ports other than those specified above left open.
 With output mode selected for PC and PD.
 With segments S13 to S28 selected.

*2. Backup mode current test circuit



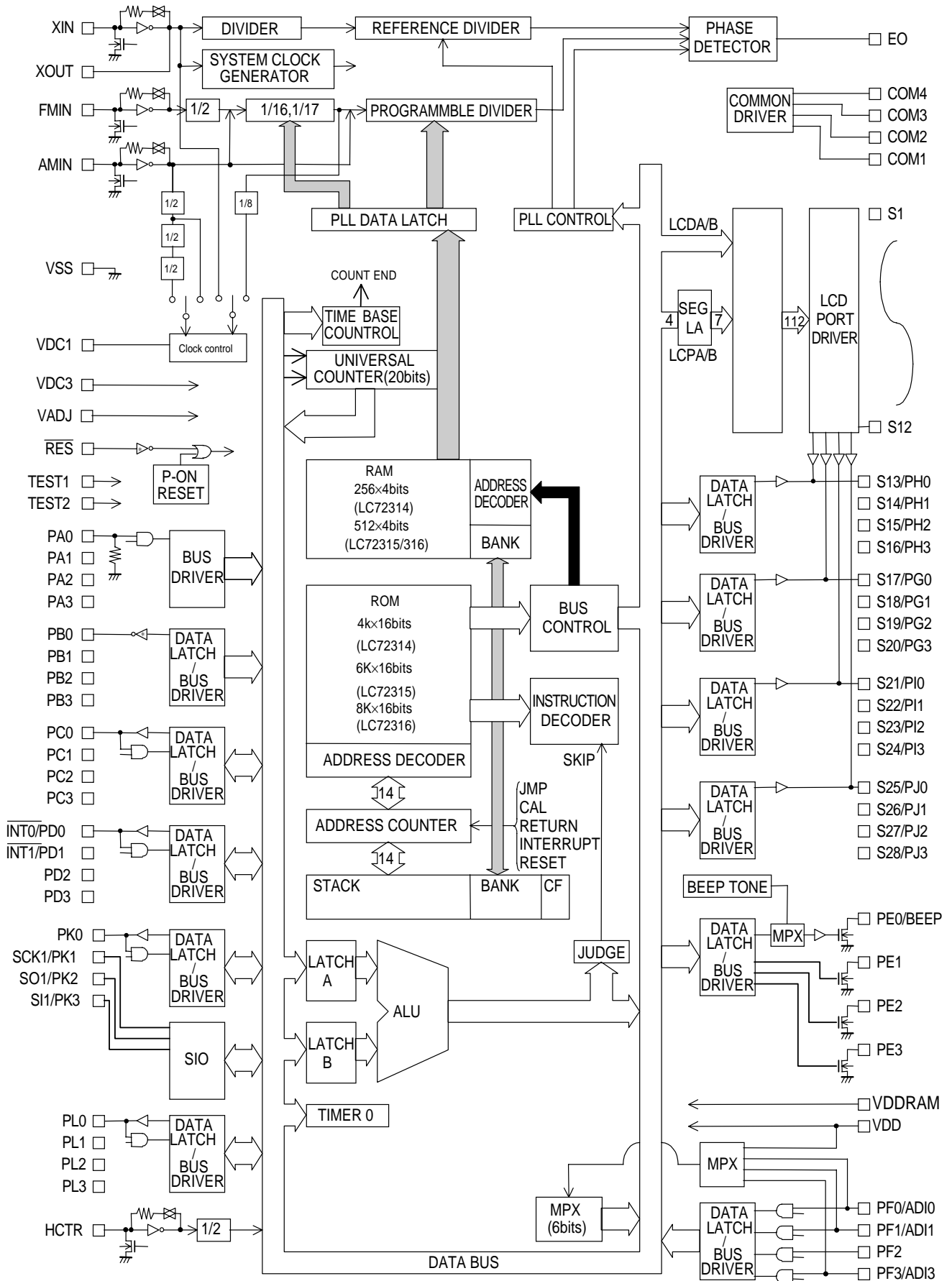
With all ports other than those specified above left open.
 With output mode selected for PC and PD.
 With segments S13 to S28 selected.

DC-DC Converter Application



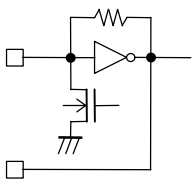
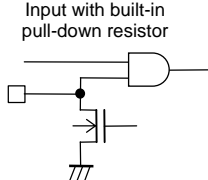
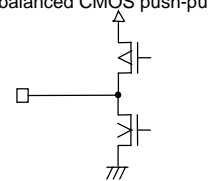
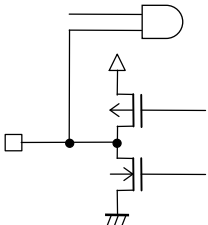
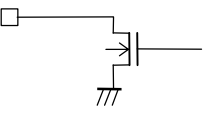
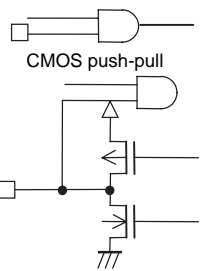
LC72314W, 72315W, 72316W

Block Diagram



LC72314W, 72315W, 72316W

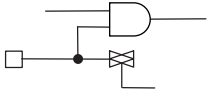
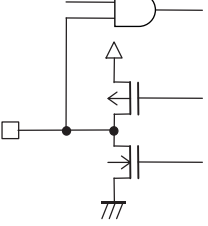
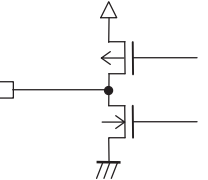
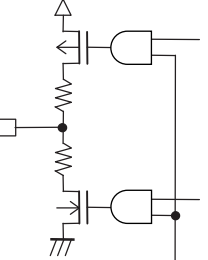
Pin Functions

Pin No.	Pin	I/O	Function	I/O circuit
80 1	XIN XOUT	I O	75 kHz oscillator connections	
79 2	TEST1 TEST2	I I	IC testing. These pins must be connected to ground during normal operation.	—
6 5 4 3	PA0 PA1 PA2 PA3	I	Special-purpose ports for key return signal input designed with a low threshold voltage. When a key matrix is formed in combination with port PB, simultaneous multiple key presses with up to 3 keys can be detected. The pull-down resistors are set up for all four pins at the same time with the IOS instruction (PWn = 2.b1). This setting cannot be specified for individual pins. In backup mode, these pins go to the input disabled state, and the pull-down resistors are disabled after a reset.	Input with built-in pull-down resistor 
10 9 8 7	PB0 PB1 PB2 PB3	O	Unbalanced CMOS outputs. These outputs are switched with the IOS 0 instruction. Since these outputs are unbalanced, no diodes are required to prevent short circuits due to simultaneous multiple key presses. These outputs go to the high-impedance output state in backup mode. After a reset, they go to the high-impedance output state and remain in that state until an output instruction (OUT, SPB, or RPB) is executed.	Unbalanced CMOS push-pull 
14 13 12 11 22 21 20 19	PC0 PC1 PC2 PC3 INT0/PD0 INT1/PD1 PD2 PD3 *2	I/O	General-purpose I/O ports. PD0, PD1 can be used as an external interrupt port. The IOS instruction (Pwn = 4, 5) is used for switching the general-purpose I/O port function, and these ports can be set to input or output in 1-bit units. (0: input, 1: output) In backup mode they go to the input disabled high-impedance state. After a reset, they switch to the general-purpose input port function.	CMOS push-pull 
26 25 24 23	BEEP/PE0 PE1 PE2 PE3	O	General-purpose output and beep tone output shared function ports (PE0 only). The BEEP instruction is used to switch PE0 between the general-purpose output port and beep tone output functions. To use PE0 as a general-purpose output port, execute a BEEP instruction with b2 set to 0. Set b2 to 1 to use PE0 as the beep tone output port. The b0 and b1 bits are used to select the beep tone frequency. There are two beep tone frequencies supported. *: When PE0 is set up as the beep tone output, executing an output instruction to PE0 only changes the state of the internal output latch, it does not affect the beep tone output in any way. Only the PE0 pin can be switched between the general-purpose output function and the beep tone output function; the PE1 to PE3 pin only functions as a general-purpose output. These pins go to the high-impedance state in backup mode and remain in that state until an output instruction or a BEEP instruction is executed. Since these ports are open-drain ports, resistors must be inserted between these pins and V _{DD} . These ports are set to general-purpose output port function after a reset.	N-channel open-drain 
18 17 16 15 34 33 32 31	PL0 PL1 PL2 PL3 PK0 SCK1/PK1 SO1/PK2 SI1/PK3	I/O I I I I/O I/O I/O I/O	Shared function pins used as either general-purpose I/O ports or a serial I/O port (only port PK). When used as general-purpose I/O ports, the I/O direction can be switched in single bit units with the IOS instruction (Pwn = 1, C). The IOS instruction (with Pwn = 1, b2) is used to switch the function between the general-purpose I/O port and the serial I/O port function. (0: general-purpose I/O port, 1: serial I/O) In backup mode (low power mode) these pins go to the input disabled high-impedance state. After a reset, the general-purpose input port function is selected. Pins PL1, PL2, and PL3 are used as input ports.	CMOS input CMOS push-pull 

Continued on next page.

LC72314W, 72315W, 72316W

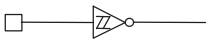
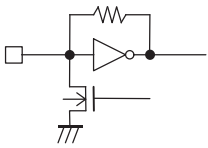
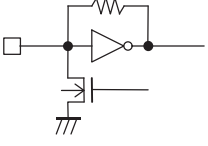
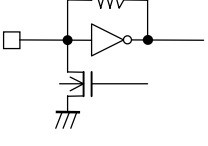
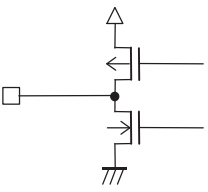
Continued from preceding page.

Pin No.	Pin	I/O	Function	I/O circuit													
30 29 28 27	PF0/ADI0 PF1/ADI1 PF2 PF3/ADI3	I	<p>General-purpose input and A/D converter input shared function ports. The IOS instruction (Pwn = FH) is used to switch between the general-purpose input and A/D converter port functions. The general-purpose input and A/D converter port functions can be switched in a units, with 0 specifying general-purpose input, and 1 specifying the A/D converter input function. To select the A/D converter function, set up the A/D converter pin with an IOS instruction with Pwn set to 1. The A/D converter is started with the UCC instruction (b3 = 1, b2 = 1). The ADCE flag is set when the conversion completes. The INR instruction is used to read in the data.</p> <p>*: If an input instruction is executed for one of these pins which is set up for analog input, the read in data will be at the low level since CMOS input is disabled. In backup mode these pins go to the input disabled high-impedance state. These ports are set to their general-purpose input port function after a reset. The A/D converter is a 6-bit successive approximation type converter, and features a conversion time of 1.28 ms. Note that the full-scale A/D converter voltage (3FH) is (63/96) V_{DD}.</p>	<p>CMOS input/analog input</p> 													
40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55	PJ3/S28 PJ2/S27 PJ1/S26 PJ0/S25 PI3/S24 PI2/S23 PI1/S22 PI0/S21 PG3/S20 PG2/S19 PG1/S18 PG0/S17 PH3/S16 PH2/S15 PH1/S14 PH0/S13 *2	I/O	<p>LCD driver segment output and general-purpose I/O shared function ports.</p> <p>The IOS instruction is used for switching between the segment output and general-purpose I/O functions and between input and output for the general-purpose I/O port function.</p> <ul style="list-style-type: none"> When used as segment output ports The general-purpose I/O port function is selected with the IOS instruction (Pwn = 8). b0 to b3 = S17 to 20/PG0 to 3 (0: segment output 1: general-purpose I/O) When used as general-purpose I/O ports The IOS instruction (Pwn = 9). b0 to b3 = S13 to 16/PH0 to 3 (0: segment output 1: general-purpose I/O) When used as general-purpose I/O ports The IOS instruction (Rwn = D) b0 to b3 = S21 to 24/PI0 to 3 (0: segment output 1: general-purpose I/O) When used as general-purpose I/O ports The IOS instruction (Rwn = E) b0 to b3 = S25 to 28/PJ0 to 3 (0: segment output 1: general-purpose I/O) When used as general-purpose I/O ports The IOS instruction (Pwn = 6, 7, A, B) is used to select input or output. Note that the mode can be set in a bit units. <table border="0" style="margin-left: auto; margin-right: auto;"> <tr> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b0 = PG0</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b0 = PH0</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b0 = PJ0</td> <td rowspan="4" style="padding: 0 10px;">0: Input 1: Output</td> </tr> <tr> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b1 = PG1</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b1 = PH0</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b1 = PJ1</td> </tr> <tr> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b2 = PG2</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b2 = PH0</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b2 = PJ2</td> </tr> <tr> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b3 = PG3</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b3 = PH0</td> <td style="border-left: 1px solid black; border-right: 1px solid black; padding: 0 5px;">b3 = PJ3</td> </tr> </table> <p>In backup mode, these pins go to the input disabled high-impedance state if set up as general-purpose outputs, and are fixed at the low level if set up as segment outputs. These ports are set up as segment outputs after a reset.</p> <p>Although the general-purpose port/LCD port setting is a mask option, the IOS instruction must be used as described above to set up the port function.</p>	b0 = PG0	b0 = PH0	b0 = PJ0	0: Input 1: Output	b1 = PG1	b1 = PH0	b1 = PJ1	b2 = PG2	b2 = PH0	b2 = PJ2	b3 = PG3	b3 = PH0	b3 = PJ3	<p>CMOS push-pull</p> 
b0 = PG0	b0 = PH0	b0 = PJ0	0: Input 1: Output														
b1 = PG1	b1 = PH0	b1 = PJ1															
b2 = PG2	b2 = PH0	b2 = PJ2															
b3 = PG3	b3 = PH0	b3 = PJ3															
56 to 67	S12 to S1	O	<p>LCD driver segment output pins.</p> <p>A 1/4-duty 1/2-bias drive technique is used.</p> <p>The frame frequency is 75 Hz.</p> <p>In backup mode, these outputs are fixed at the low level.</p> <p>After a reset, these outputs are fixed at the low level.</p>	<p>CMOS push-pull</p> 													
68 69 70 71	COM4 COM3 COM2 COM1	O	<p>LCD driver common output pins.</p> <p>A 1/4-duty 1/2-bias drive technique is used.</p> <p>The frame frequency is 75 Hz.</p> <p>In backup mode, these outputs are fixed at the low level.</p> <p>After a reset, these outputs are fixed at the low level.</p>														

Continued on next page.

LC72314W, 72315W, 72316W

Continued from preceding page.

Pin No.	Pin	I/O	Function	I/O circuit																														
72	$\overline{\text{RES}}$	I	System reset input. In CPU operating mode or halt mode, applications must apply a low level for at least one full machine cycle to reset the system and restart execution with the PC set to location 0. This pin is connected in parallel with the internal power on reset circuit.																															
38	VDC1	O	Output for the 3 V step-up circuit clock. Outputs 1/2 the AM local oscillator frequency in AM reception mode, and 1/256 the FM local oscillator or 75 kHz in FM reception mode.																															
37	VDC3	I	Voltage stepped up by the DC-DC converter (3 V) May also be used to input an equivalent voltage.																															
36	VDDRAM	I	RAM backup power supply. Connected to the VDC3 voltage through a diode.																															
39	VADJ	O	VDC3 voltage adjustment pin. Insert a 10 kΩ variable resistor between this pin and ground to adjust the VDC3 voltage.																															
75	FMIN	I	FM VCO (local oscillator) input. This pin is selected with the PLL instruction CW1. The input must be capacitor coupled. Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.	CMOS amplifier input 																														
76	AMIN	I	AM VCO (local oscillator) input. This pin and the bandwidth are selected with the PLL instruction CW1. <table border="1" data-bbox="566 1064 1125 1153"> <thead> <tr> <th>CW1</th> <th>b1, b0</th> <th>Input pins</th> <th>Bandwidth</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>AMIN (H)</td> <td>2 to 20 MHz (SW)</td> </tr> <tr> <td>1</td> <td>1</td> <td>FMIN (L)</td> <td>0.5 to 10 MHz (MW, LW)</td> </tr> </tbody> </table> The input must be capacitor coupled. Input is disabled in backup mode, in halt mode, after a reset, and in PLL stop mode.	CW1	b1, b0	Input pins	Bandwidth	1	0	AMIN (H)	2 to 20 MHz (SW)	1	1	FMIN (L)	0.5 to 10 MHz (MW, LW)	CMOS amplifier input 																		
CW1	b1, b0	Input pins	Bandwidth																															
1	0	AMIN (H)	2 to 20 MHz (SW)																															
1	1	FMIN (L)	0.5 to 10 MHz (MW, LW)																															
73	HCTR	I	Dedicated input port for the universal counter. • For frequency measurement, select the HCTR frequency measurement mode and measurement time with a UCS instruction (b3 = 0, b2 = 0) and start the counter with a UCC instruction. <table border="1" data-bbox="486 1355 1189 1512"> <thead> <tr> <th>UCS</th> <th>b3, b2</th> <th>Input pin measurement mode</th> <th>UCS</th> <th>b1, b0</th> <th>Measurement time</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>HCTR frequency measurement</td> <td>0</td> <td>0</td> <td>1 ms</td> </tr> <tr> <td>0</td> <td>1</td> <td>—</td> <td>0</td> <td>1</td> <td>4 ms</td> </tr> <tr> <td>1</td> <td>1</td> <td>—</td> <td>1</td> <td>0</td> <td>8 ms</td> </tr> <tr> <td></td> <td></td> <td></td> <td>1</td> <td>1</td> <td>32 ms</td> </tr> </tbody> </table> When the count operation completes, the CNTEND flag will be set. Since it operates as an AC amplifier in this mode, the input must be provided through a coupling capacitor. Input is disabled in backup mode, HALT mode, after a reset, and in PLL STOP mode.	UCS	b3, b2	Input pin measurement mode	UCS	b1, b0	Measurement time	0	0	HCTR frequency measurement	0	0	1 ms	0	1	—	0	1	4 ms	1	1	—	1	0	8 ms				1	1	32 ms	CMOS amplifier input 
UCS	b3, b2	Input pin measurement mode	UCS	b1, b0	Measurement time																													
0	0	HCTR frequency measurement	0	0	1 ms																													
0	1	—	0	1	4 ms																													
1	1	—	1	0	8 ms																													
			1	1	32 ms																													
78	EO	O	Main charge pump output. When the local oscillator frequency divided by N is higher than the reference frequency a high level is output, when lower, a low level is output, and the pin is set to the high-impedance state when the frequencies match. This output goes to the high-impedance state in backup mode, in halt mode, after a reset, and in PLL stop mode.	CMOS push-pull 																														
77 35 74	V _{SS} V _{SS} V _{DD}	—	Power supply pin. This pin must be connected to ground. This pin must be connected to ground. This pin must be connected to V _{DD} . Supports A/D converter.	—																														

Note*: When a pin in an I/O switching port is used as an output, applications must first set up the data with an OUT, SPB, or RPB instruction and then set up output mode with an IOS instruction.

LC72314 Series Instruction Set

Terminology

- ADDR : Program memory address
- b : Borrow
- C : Carry
- DH : Data memory address High (Row address) [2 bits]
- DL : Data memory address Low (Column address) [4 bits]
- I : Immediate data [4 bits]
- M : Data memory address
- N : Bit position [4 bits]
- Rn : Resister number [4 bits]
- Pn : Port number [4 bits]
- PW : Port control word number [4 bits]
- r : General register (One of the addresses from 00H to 0FH of BANK0)
- (), [] : Contents of register or memory
- M (DH, DL) : Data memory specified by DH, DL

Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format														
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1
Addition instructions	AD	r	M	Add M to r	$R \leftarrow (r) + (M)$	0	1	0	0	0	0	DH	DL	r						
	ADS	r	M	Add M to r, then skip if carry	$R \leftarrow (r) + (M)$, skip if carry	0	1	0	0	0	1	DH	DL	r						
	AC	r	M	Add M to r with carry	$R \leftarrow (r) + (M) + C$	0	1	0	0	1	0	DH	DL	r						
	ACS	r	M	Add M to r with carry, then skip if carry	$R \leftarrow (r) + (M) + C$ skip if carry	0	1	0	0	1	1	DH	DL	r						
	AI	M	I	Add I to M	$M \leftarrow (M) + I$	0	1	0	1	0	0	DH	DL	I						
	AIS	M	I	Add I to M, then skip if carry	$M \leftarrow (M) + I$, skip if carry	0	1	0	1	0	1	DH	DL	I						
	AIC	M	I	Add I to M with carry	$M \leftarrow (M) + I + C$	0	1	0	1	1	0	DH	DL	I						
Subtraction instructions	AICS	M	I	Add I to M with carry, then skip if carry	$M \leftarrow (M) + I + C$, skip if carry	0	1	0	1	1	1	DH	DL	I						
	SU	r	M	Subtract M from r	$R \leftarrow (r) - (M)$	0	1	1	0	0	0	DH	DL	r						
	SUS	r	M	Subtract M from r, then skip if borrow	$R \leftarrow (r) - (M)$, skip if borrow	0	1	1	0	0	1	DH	DL	r						
	SB	r	M	Subtract M from r with borrow	$R \leftarrow (r) - (M) - b$	0	1	1	0	1	0	DH	DL	r						
	SBS	r	M	Subtract M from r with borrow, then skip if borrow	$R \leftarrow (r) - (M) - b$, skip if borrow	0	1	1	0	1	1	DH	DL	r						
	SI	M	I	Subtract I from M	$M \leftarrow (M) - I$	0	1	1	1	0	0	DH	DL	I						
	SIS	M	I	Subtract I from M, then skip if borrow	$M \leftarrow (M) - I$, skip if borrow	0	1	1	1	0	1	DH	DL	I						
Comparison instructions	SIB	M	I	Subtract I from M with borrow	$M \leftarrow (M) - I - b$	0	1	1	1	1	0	DH	DL	I						
	SIBS	M	I	Subtract I from M with borrow, then skip if borrow	$M \leftarrow (M) - I - b$, skip if borrow	0	1	1	1	1	1	DH	DL	I						
	SEQ	r	M	Skip if r equal to M	$(r) - (M)$, skip if zero	0	0	0	1	0	0	DH	DL	r						
	SEQI	M	I	Skip if M equal to I	$(M) - I$, skip if zero	0	0	0	1	1	0	DH	DL	I						
	SNEI	M	I	Skip if M not equal to I	$(M) - I$, skip if not zero	0	0	0	0	0	1	DH	DL	I						
	SGE	r	M	Skip if r is greater than or equal to M	$(r) - (M)$, skip if not borrow	0	0	0	1	1	0	DH	DL	r						
Comparison instructions	SGEI	M	I	Skip if M is greater than equal to I	$(M) - I$, skip if not borrow	0	0	0	1	1	1	DH	DL	I						
	SLEI	M	I	Skip if M is less than I	$(M) - I$, skip if borrow	0	0	0	0	1	1	DH	DL	I						

Continued on next page.

LC72314W, 72315W, 72316W

Continued from preceding page.

Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format															
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
Logic operation instructions	AND	r	M	AND M with r	$R \leftarrow (r) \text{ AND } (M)$	0	0	1	0	0	0	DH	DL							r	
	ANDI	M	I	AND I with M	$M \leftarrow (M) \text{ AND } I$	0	0	1	0	0	1	DH	DL							I	
	OR	r	M	OR M with r	$R \leftarrow (r) \text{ OR } (M)$	0	0	1	0	1	0	DH	DL							r	
	ORI	M	I	OR I with M	$M \leftarrow (M) \text{ OR } I$	0	0	1	0	1	1	DH	DL							I	
	EXL	r	M	Exclusive OR M with r	$R \leftarrow (r) \text{ XOR } (M)$	0	0	1	1	0	0	DH	DL							r	
	EXLI	M	I	Exclusive OR M with M	$M \leftarrow (M) \text{ XOR } I$	0	0	1	1	1	0	DH	DL							I	
Transfer instructions	SHR	r		Shift r right with carry		0	0	0	0	0	0	0	0	1	1	1	0			r	
	LD	r	M	Load M to r	$R \leftarrow (M)$	1	1	0	1	0	0	DH	DL							r	
	ST	M	r	Store r to M	$M \leftarrow (r)$	1	1	0	1	0	1	DH	DL							r	
	MVRD	r	M	Move M to destination M referring to r in the same row	$[DH, Rn] \leftarrow (M)$	1	1	0	1	1	0	DH	DL							r	
	MVRS	M	r	Move source M referring to r to M in the same row	$M \leftarrow [DH, Rn]$	1	1	0	1	1	1	DH	DL							r	
	MVSR	M1	M2	Move M to M in the same row	$[DH, DL1] \leftarrow [DH, DL2]$	1	1	1	0	0	0	DH	DL1							DL2	
Bit test instructions	MVI	M	I	Move I to M	$M \leftarrow I$	1	1	1	0	0	1	DH	DL							I	
	TMT	M	N	Test M bits, then skip if all bits specified are true	if M (N) = all 1, then skip	1	1	1	1	0	0	DH	DL							N	
Jump and subroutine call instructions	TMF	M	N	Test M bits, then skip if all bits specified are false	if M (N) = all 0, then skip	1	1	1	1	0	1	DH	DL							N	
	JMP	ADDR		Jump to the address	$PC \leftarrow ADDR$	1	0	0	ADDR (13 bits)												
	CAL	ADDR		Call subroutine	$PC \leftarrow ADDR$ $Stack \leftarrow (PC) + 1$	1	0	1	ADDR (13 bits)												
	RT			Return from subroutine	$PC \leftarrow Stack$	0	0	0	0	0	0	0	0	0	1	0	0	0			
Status register instructions	RTI			Return from interrupt	$PC \leftarrow Stack$, $BANK \leftarrow Stack$, $CARRY \leftarrow Stack$	0	0	0	0	0	0	0	0	1	0	0	0	1			
	SS	SWR	N	Set status register	$(Status\ W-reg) N \leftarrow 1$	1	1	1	1	1	1	1	1	0	0	0	0	SWR	N		
	RS	SWR	N	Reset status register	$(Status\ W-reg) N \leftarrow 0$	1	1	1	1	1	1	1	1	0	0	1	SWR	N			
	TST	SRR	N	Test status register true	If (Status R-reg) N = all	1	1	1	1	1	1	1	1	0	1	SRR	N				
	TSF	SRR	N	Test status register false	If (Status R-reg) N = all	1	1	1	1	1	1	1	1	1	0	SRR	N				
Hardware control instructions	TUL	N		Test Unlock F/F	If Unlock F/F (N) = All 0s, then skip	0	0	0	0	0	0	0	0	1	1	0	1		N		
	PLL	M		Load M to PLL register	$PLL\ reg \leftarrow PLL\ data$	1	1	1	1	1	0	DH	DL					r			
	SIO	I1	I2	Serial I/O control	$SIO\ reg \leftarrow I1, I2$	0	0	0	0	0	0	0	1		I1			I2			
	UCS	I		Set I to UCCW1	$UCCW1 \leftarrow I$	0	0	0	0	0	0	0	0	0	0	1		I			
	UCC	I		Set I to UCCW2	$UCCW2 \leftarrow I$	0	0	0	0	0	0	0	0	0	1	0		I			
	BEEP	I		Beep control	$BEEP\ reg \leftarrow I$	0	0	0	0	0	0	0	0	1	1	0		I			
	DZC	I		Dead zone control	$DZC\ reg \leftarrow I$	0	0	0	0	0	0	0	1	0	1	1		I			
	TMS	I		Set timer register	$Timer\ reg \leftarrow I$	0	0	0	0	0	0	0	1	1	0	0		I			
I/O instructions	IOS	PWn	N	Set port control word	$IOS\ reg\ PWn \leftarrow N$	1	1	1	1	1	1	0	PWn						N		
	IN	M	Pn	Input register port data to M	$M \leftarrow (Pn)$	1	1	1	0	1	0	DH	DL					Pn			
	OUT	M	Pn	Output contents of M to port	$Pn \leftarrow M$	1	1	1	0	1	1	DH	DL					Pn			
	INR	M	Rn	Input port data to M	$M \leftarrow (Pn\ reg)$	0	0	1	1	1	0	DH	DL					Pn			
	OUTR	M	Rn	Output contents of M to register/port	$Rn\ reg \leftarrow (M)$	0	0	1	1	1	1	DH	DL					Rn			
	SPB	Pn	N	Set port bits	$(Pn)N \leftarrow 1$	0	0	0	0	0	0	1	0	Pn				N			
	RPB	Pn	N	Reset port bits	$(Pn)N \leftarrow 0$	0	0	0	0	0	0	1	1	Pn				N			
	TPT	Pn	N	Test port1 bits, then skip if all bits specified are true	If (Pn)N = all 1, then skip	1	1	1	1	1	1	0	0	Pn				N			
Bank switching instructions	TPF	Pn	N	Test port1 bits, then skip if all bits specified are false	If (Pn)N = all 0, then skip	1	1	1	1	1	1	0	1	Pn				N			
	BANK	I		Select Bank	$BANK \leftarrow I$	0	0	0	0	0	0	0	0	1	1	1		I			

Continued on next page.

LC72314W, 72315W, 72316W

Continued from preceding page.

Instruction group	Mnemonic	Operand		Function	Operations function	Instruction format															
		1st	2nd			f	e	d	c	b	a	9	8	7	6	5	4	3	2	1	0
LCD instructions	LCDA	M	I	Output segment pattern to LCD digit direct	LCD (DIGIT) ← M	1	1	0	0	0	0	DH		DL		DIGIT					
	LCDB	M	I			1	1	0	0	0	1	DH		DL		DIGIT					
	LCPA	M	I	Output segment pattern to LCD digit through LA	LCD (DIGIT) ← LA ← M	1	1	0	0	1	0	DH		DL		DIGIT					
	LCPB	M	I			1	1	0	0	1	1	DH		DL		DIGIT					
Other instructions	HALT	I		Halt mode control	HALT reg ← I, then CPU clock stop	0	0	0	0	0	0	0	0	0	0	0	1	0	0	I	
	CKSTP			Clock stop	Stop x'tal OSC	0	0	0	0	0	0	0	0	0	0	0	1	0	1		
	NOP			No operation	No operation	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

- Specifications of any and all SANYO products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- SANYO Electric Co., Ltd. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of SANYO Electric Co., Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of November, 2001. Specifications and information herein are subject to change without notice.