Ordering number: ENN*6585

CMOS IC

LC7958NC

64-Bit LED Driver for 300 dpi Printers

Preliminary

Overview

LC7958NC is a 64-bit constant current LED driver IC designed to directly drive LED head array.
The output terminals for LED drive are arranged in 2-row staggered position of 80-µm pitch at one side. It enables drive of LED Array of 300-dpi in one side disposition, 600dpi in both sides disposition

Features and Functions

- Logic voltage (VDD): +5 V ± 10 %
- LED drive current (IOH): 5.0 mA (TYP)
- Clock frequency (fc): 10 MHz
- Output current control circuit built in
- Mode switching function by the SEL pin
- Chip size: 1.43 mm × 5.39 mm
- Number of pads: 86
- 64-bit shift register circuit
- 64-bit latch circuit
- Output driver on/off switching function
- Constant current circuit
- 64-bit p-channel open drain LED driver

SANYO Electric Co.,Ltd. Semiconductor Company
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

The characteristics shown below are those of devices encapsulated in the SANYO standard ceramic package

Specifications

Absolute Maximum Ratings at Vss=0V

Parameter	Symbol	Conditions	Ratings	Unit
Power supply voltage	VDD1	Ta = 25 °C	-0.3 to 6.5	V
	VDD2		-0.3 to 6.5	
Input voltage	VI	Ta = 25 °C	-0.3 to VDD1+ 0.3	V
Output voltage	VO	Ta = 25 °C	-0.3 to VDD1+ 0.3	V
Driver output current	IOUT		0 to -10	mA
Operating Junction temperature	Tj		-10 to 125	°C
Storage temperature	Tstg		-35 to 125	°C

Allowable Operating Ranges at Vss = 0 V, VDD1 = VDD2 = 5 V ± 10%, Ta = 0 to 100°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Power supply voltage	VDD1,VDD2	VDD1(pad 2), VDD2(pad 6)	4.5		5.5	V
Potential difference*1	VDF	Between VDD1 and VDD2	-0.3	0	0.3	
High-level input voltage	VIH	All inputs	2.0		VDD1	V
Low-level input voltage	VIL		0		0.8	V
Clock frequency	fc	CLOCK 1			10	MHz
Clock duty	D CLK	CLOCK 1	35	50	65	%
Setup time from SI to CLOCK1	tsc	SI, CLOCK 1	30			ns
Hold time from CLOCK1 to SI	thold	SI, CLOCK 1	10			ns
Setup time from CLOCK1 to LOAD1	tSL	LOAD 1, CLOCK 1	50			ns
Hold time from LOAD1 to CLOCK1	tHL	LOAD 1, CLOCK 1	50			ns
LOAD1 pulse width	tWL	LOAD 1	40			ns
CLOCK1 rise/fall time	tCr tCf	CLOCK 1			35	ns
LOAD1 rise/fall time	tLr tLf	LOAD 1			35	ns

*1:In case potential difference occurred between VDD1 and VDD2, Driver current value changes. Therefore using it with VDD1=VDD2 is recommended.

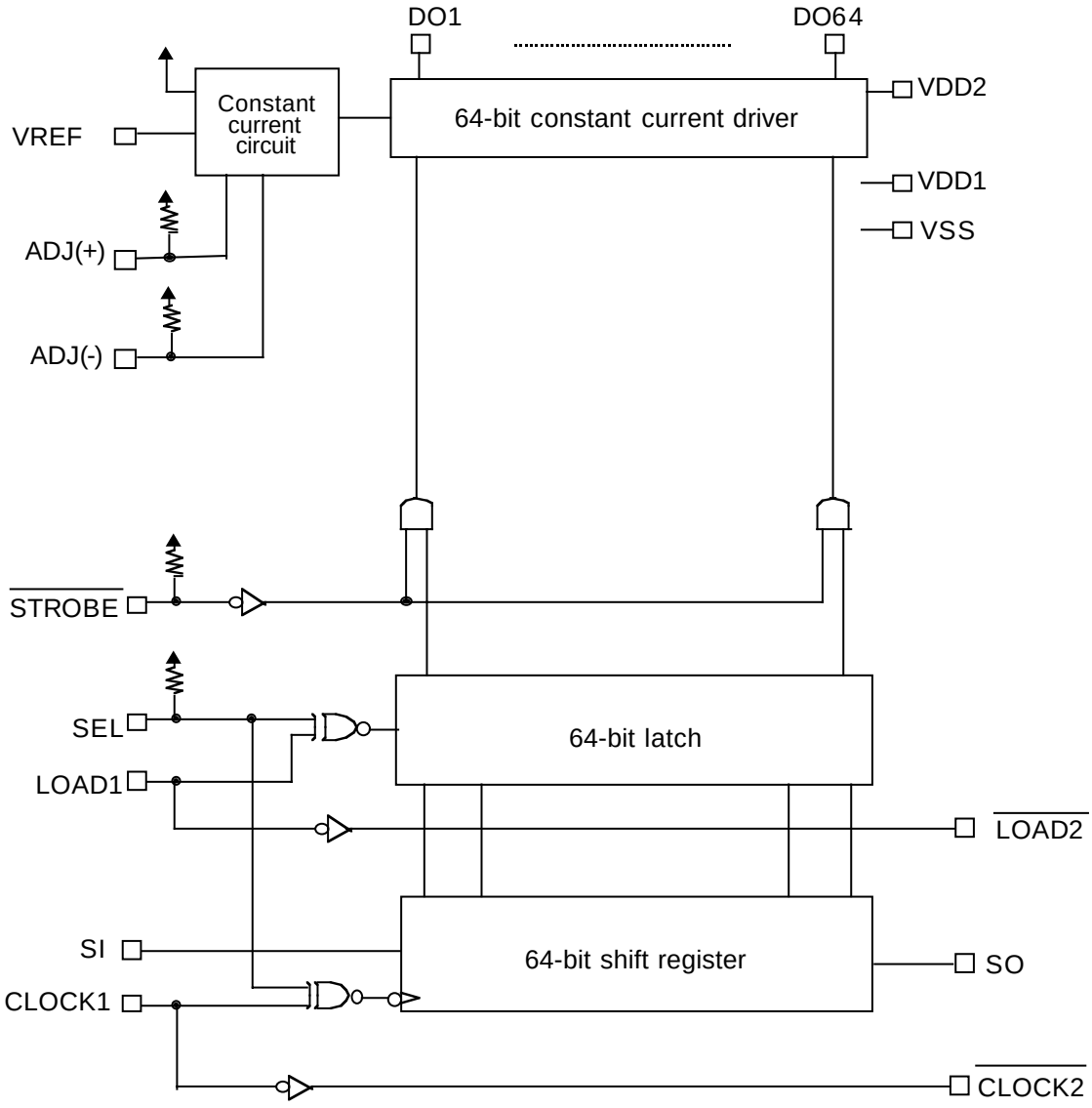
Electrical Characteristics at VSS = 0 V, VDD1 = VDD2 = 5 V ± 10%, Ta = 0 to 100°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
High-level output voltage	VOH	LOAD2, S0, CLOCK2: IO = -200µA	VDD - 0.5			V
Low-level output voltage	VOL	LOAD2, S0, CLOCK2: IO = 200µA			0.5	V
Clock frequency	fc		10			MHz
High-level input current	IIH	All input pads: VDD1 = 5.5 V, VI = 5.5 V			1.0	µA
Low-level input current	IIL1	LOAD1, SI, CLOCK1, STROBE, SEL, ADJ(-), ADJ(+): VDD1 = VDD2 = 5.5 V, VI = 0 V			-1.0	µA
	IIL2		-8	-25	-50	
	IIL3		-40	-100	-200	
High-level output current	IOH1	DO1 to DO64: operation mode 1, VDD1 = VDD2 = 5.0 V, VO = 1.6 V, VREF = 1.8 V	-3.7	-5.0	-6.7	mA
High-level output current minus correction	IOH2	DO1 to DO64: operation mode 2 VDD1 = VDD2 = 5.0 V, VO = 1.6 V, VREF = 1.8 V	-4.5	-6.0	-7.0	%
High-level output current plus correction	IOH3	DO1 to DO64: operation mode 3 VDD1 = VDD2 = 5.0 V, VO = 1.6 V, VREF = 1.8 V	+4.5	+6.0	+7.0	
High-level output current relative error between bits	ΔIOH	DO1 to DO64: with all bits on	-5.0		+5.0	%
Output off leakage current	IOL	DO1 to DO64: operation VDD1 = 5.5 V, VO = 0 V		0	-50	µA
Operating current drain (mode 1)	IDD	VDD1: VDD1 = VDD2 = 5.5 V, VREF = 1.8 V, fc = 10 MHz, with DO1 to DO64 off		9.0	13.0	mA
Standby current	IDDS	VDD1: VDD1 = VDD2 = 5.5 V, VREF = 1.8 V, with fc stopped, with DO1 to DO64 off		2.5	4.0	mA

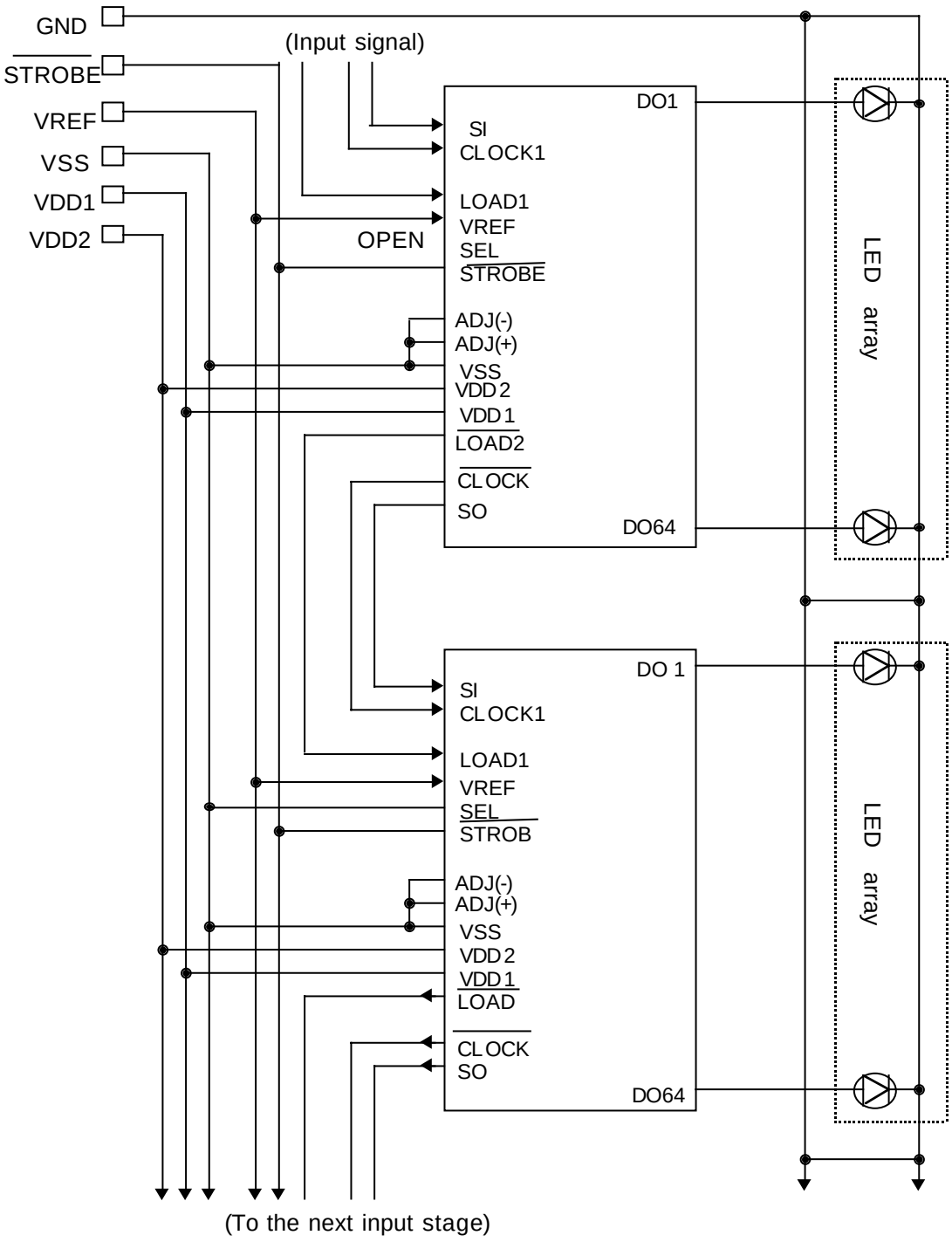
Switching Characteristics at VSS = 0 V, VDD1 = VDD2 = 5 V ± 10%, Ta = 0 to 100°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
SO output rise time	tor	SO: CL=10.8pF			50	ns
SO output fall time	tof					
Output transmission delay time from STROBE to DO	tpsr	STROBE, DO1 to DO64: CL = 10.8 pF, RF = 10 kΩ			250	ns
	tpsf					
Output transmission delay time from CLOCK2 to SO	tpcr	CLOCK2, SO	10		70	ns
	tpcf					
CLOCK1→CLOCK2 transmission delay time	tPH	CLOC1, CLOCK2, LOAD1, LOAD2: CL=10.8 pF			40	ns
	tPL					

Equivalent Circuit Block Diagram



Sample Application Circuit Diagram



Note 1: The electric potential of the IC substrate is at VDD1.

Note 2: The number of cascade connection stages should be within 60. (10MHz)

Note 3: All VDD2 terminals should be bonded.

Note 4: Leave the SEL Terminal of the odd-numbered IC open, and connect the SEL terminal of even-numbered IC with VSS.

Note 5: Apply the stable potential other than the VDD1 and VDD2 lines to the VREF terminal.

Function Table

1. Shift Register and Latch Blocks

SEL	CLOCK1	LOAD1	Shift register	Latch
High	Falling edge	-	DATA load and DATA shift	-
	Rising edge	-	DATA keep	-
	-	High	-	DATA load
	-	Low	-	DATA keep
Low	Falling edge	-	DATA load and DATA shift	-
	Rising edge	-	DATA keep	-
	-	Low	-	DATA load
	-	High	-	DATA keep

2. Output Block

$\overline{\text{STROBE}}$	SI	DO output
High	"×"	OFF
Low	Low	OFF
Low	High	ON

Note 1: "×": don't care

Establishment of Output Current

MODE	ADJ(+)	ADJ(-)	Current control resistance	IOH(typ)
1	Low	Low	Built in (RINT)	VREF/RINT × 10
2	Low	High	Built in (RINT)	VREF/RINT × 10 × 0.94
3	High	Low	Built in (RINT)	VREF/RINT× 10 × 1.06

Note 2: RINT(TYP) = 3.61 kΩ

*Complement explanation

Here shows the general usage of the modes 1 to 3 as follows.
MODE 1 is set by connecting the ADJ(+) and ADJ(-) terminals with VSS. In the MODE1 state, by cutting the bonding wire connected with ADJ(+) or ADJ(-), the IC enters the MODE2 or MODE3, respectively. The current in MODE1 can be corrected by about –6 % or +6 % in MODE2 or MODE3, respectively.

Ranking by Output Current

1. Test condition: VDD1 = VDD2 = 5.0 V, VREF = 1.8 V, VO = 1.6 V, Ta = 25 °C

2. Ranking determination: The rank is determined by the average ON current (Iave) of the terminals DO1 to DO64 when the all DO outputs are on.

3. Current width: (Imax - Imin)/(Imax + Imin) ≈ 2.0 %

Rank			Specification [mA]
A	B	C	
-	1	-	-3.700 to -3.853
-	2	-	-3.854 to -4.011
-	3	-	-4.012 to -4.177
1	4	-	-4.178 to -4.347
2	5	-	-4.348 to -4.524
3	6	-	-4.525 to -4.708
4	7	1	-4.709 to -4.900
5	8	2	-4.901 to -5.100
6	9	3	-5.101 to -5.308
7	-	4	-5.309 to -5.524
8	-	5	-5.525 to -5.749
9	-	6	-5.750 to -5.983
-	-	7	-5.984 to -6.227
-	-	8	-6.228 to -6.481
-	-	9	-6.482 to -6.700
*	*	*	Rejected article (for the manufacturing process control)

Note: The chips of Ranking No. "*" are marked with the ink

ON Current Deviation in a Chip

Test condition: VDD1 = VDD2 = 5.0 V, VO = 1.6 V, VREF = 1.8 V, Ta = 25 °C

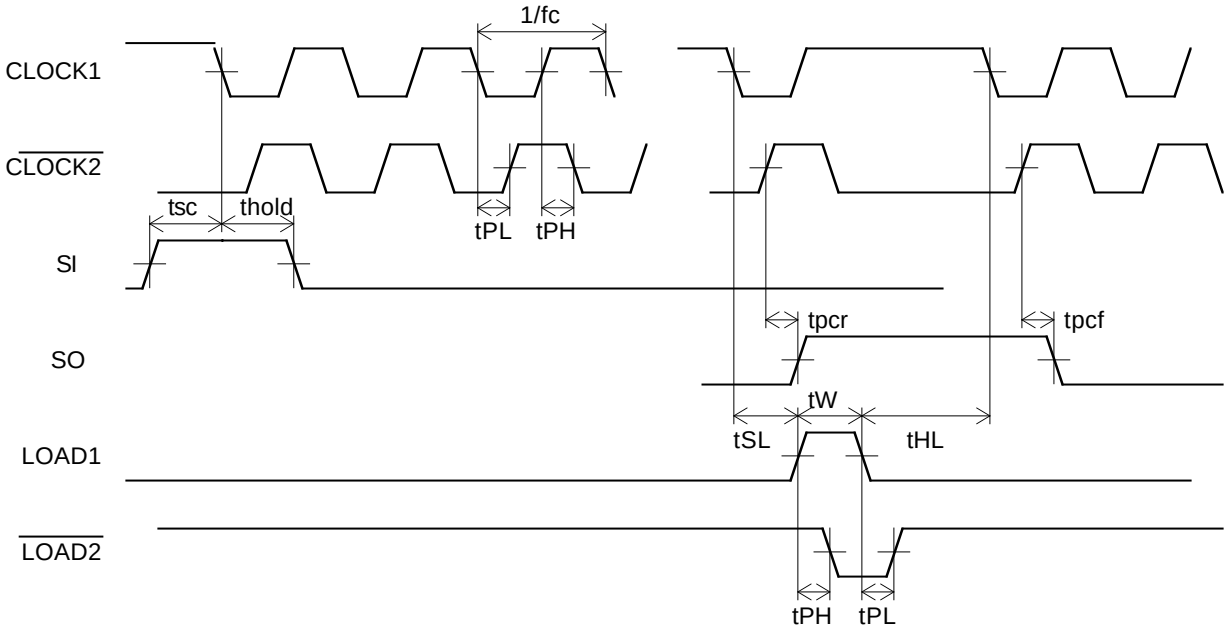
1. Let the average ON current of the terminals DO4, 12, 20, 28, 36, 44, 52, and 60 be Cave, the that of the terminals DO1, 12, 20, and 28 be Lave, and that of the terminals DO36, 44, 52, and 60 be Rave: then the relationship among the Cave, Lave, and Rave should be as follows.

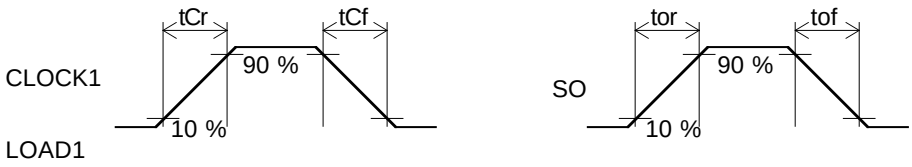
$|\text{Lave} - \text{Cave}| / \text{Cave} \leq 2.5\ \%$, $|\text{Rave} - \text{Cave}| / \text{Cave} \leq 2.5\ \%$

2. Let the average ON current of DO1 to DO8, DO29 to DO36, and DO57 to DO64 be I1, I2, and I3, respectively: the relationship among the I1, I2, and I3 should be as follows.

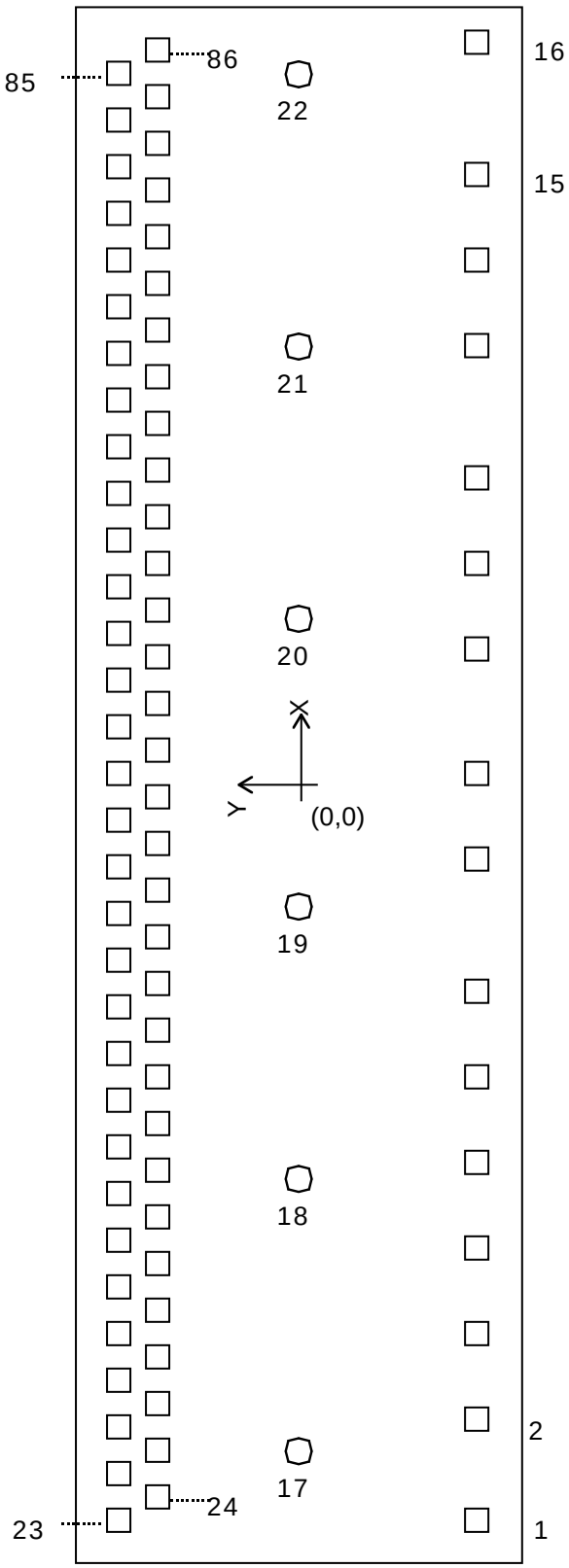
$|\text{In} - \text{Iave}| / \text{Iave} \leq 2.5\ \%$, Iave: Average ON current of the DO1 to DO64.
In: I2, and I3

Timing Chart (SEL = High)





Pad Assignment



Chip size: 5.39 mm × 1.43 mm

Pad size: (PV open)

110 µm × 110 µm (Others)

Φ 110 µm (VDD2)

100 µm × 100 µm (DOn)

Chip thickness: 330 µm ± 30 µm

Pad Coordinates

Unit: μm

No.	Pin	X	Y	No.	Pin	X	Y
1	SI	-2520	-484	44	DO22	-840	398
2	CLOCK1	-2040	-484	45	DO23	-760	539
3	LOAD1	-1800	-484	46	DO24	-680	398
4	VDD	-1560	-484	47	DO25	-600	539
5	VREF	-1080	-484	48	DO26	-520	398
6	SEL	-840	-484	49	DO27	-440	539
7	STROBE	-600	-484	50	DO28	-360	398
8	VSS	-120	-484	51	DO29	-280	539
9	NC	120	-484	52	DO30	-200	398
10	ADJ(-)	600	-484	53	DO31	-120	539
11	ADJ(+)	840	-484	54	DO32	-40	398
12	VSS	1080	-484	55	DO33	40	539
13	VDD	1560	-484	56	DO34	120	398
14	LOAD2	1800	-484	57	DO35	200	539
15	CLOCK2	2040	-484	58	DO36	280	398
16	S0	2520	-484	59	DO37	360	539
17	VDD2	-2280	18	60	DO38	440	398
18	VDD2	-1320	18	61	DO39	520	539
19	VDD2	-360	18	62	DO40	600	398
20	VDD2	360	18	63	DO41	680	539
21	VDD2	1320	18	64	DO42	760	398
22	VDD2	2280	18	65	DO43	840	539
23	DO1	-2520	539	66	DO44	920	398
24	D02	-2440	398	67	DO45	1000	539
25	DO3	-2360	539	68	DO46	1080	398
26	DO4	-2280	398	69	DO47	1160	539
27	DO5	-2200	539	70	DO48	1240	398
28	DO6	-2120	398	71	DO49	1320	539
29	DO7	-2040	539	72	DO50	1400	398
30	DO8	-1960	398	73	DO51	1480	539
31	DO9	-1880	539	74	DO52	1560	398
32	DO10	-1800	398	75	DO53	1640	539
33	DO11	-1720	539	76	DO54	1720	398
34	DO12	-1640	398	77	DO55	1800	539
35	DO13	-1560	539	78	DO56	1880	398
36	DO14	-1480	398	79	DO57	1960	539
37	DO15	-1400	539	80	DO58	2040	398
38	DO16	-1320	398	81	DO59	2120	539
39	DO17	-1240	539	82	DO60	2200	398
40	DO18	-1160	398	83	DO61	2280	539
41	DO19	-1080	539	84	DO62	2360	398
42	DO20	-1000	398	85	DO63	2440	539
43	DO21	-920	539	86	DO64	2520	398