

SANYO

No. ※ 4971

LC9947G**1/5 Inch Optical Size EIA Black-and-White
Solid-State Imaging Device****Preliminary****Overview**

The LC9947G is a 1/5 inch optical size frame transfer CCD (charge-coupled device) solid-state imaging device.

Features

- Effective number of pixels [total pixels]:
508 × 492 [532 × 500] (H × V)
- Number of optical blacks
Horizontal direction: Front: 2 pixels
Rear: 22 pixels
Vertical direction: Front: 5 pixels
Rear: 3 pixels
- Horizontal resolution: 380 TV lines
- Miniature size supports compact application designs.
- The LC9947G is provided in a 20-pin half-pitch completely transparent DIP package.
- Horizontal shift register, 5 V operation
- Can be used with a variable-speed electronic shutter

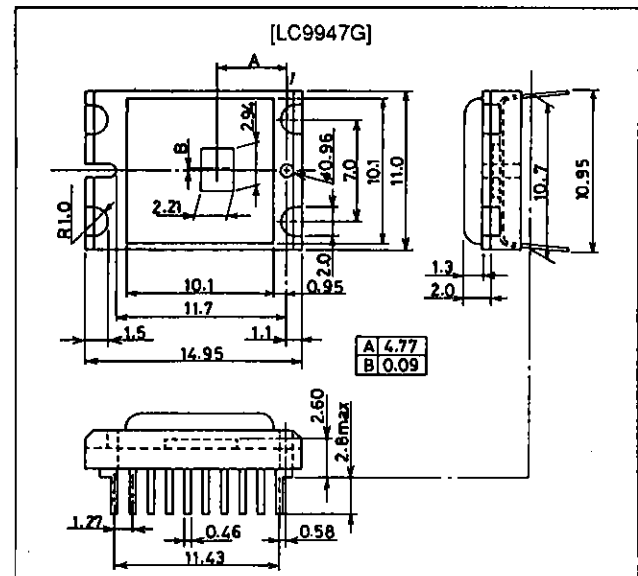
Device Structure

- 1/5 inch optical size frame transfer CCD image sensor
- Unit cell size: 5.8 μm (H) × 4.5 μm (V)
- Chip size: 4.180 mm (H) × 5.100 mm (V)
- Parallel gate CCD sensor
- Built-in high-sensitivity output amplifier

Note: Please contact your Sanyo sales representative in advance if you plan to design an optical system for this product.

Package Dimensions

unit: mm

3208A**SANYO Electric Co., Ltd. Semiconductor Business Headquarters**

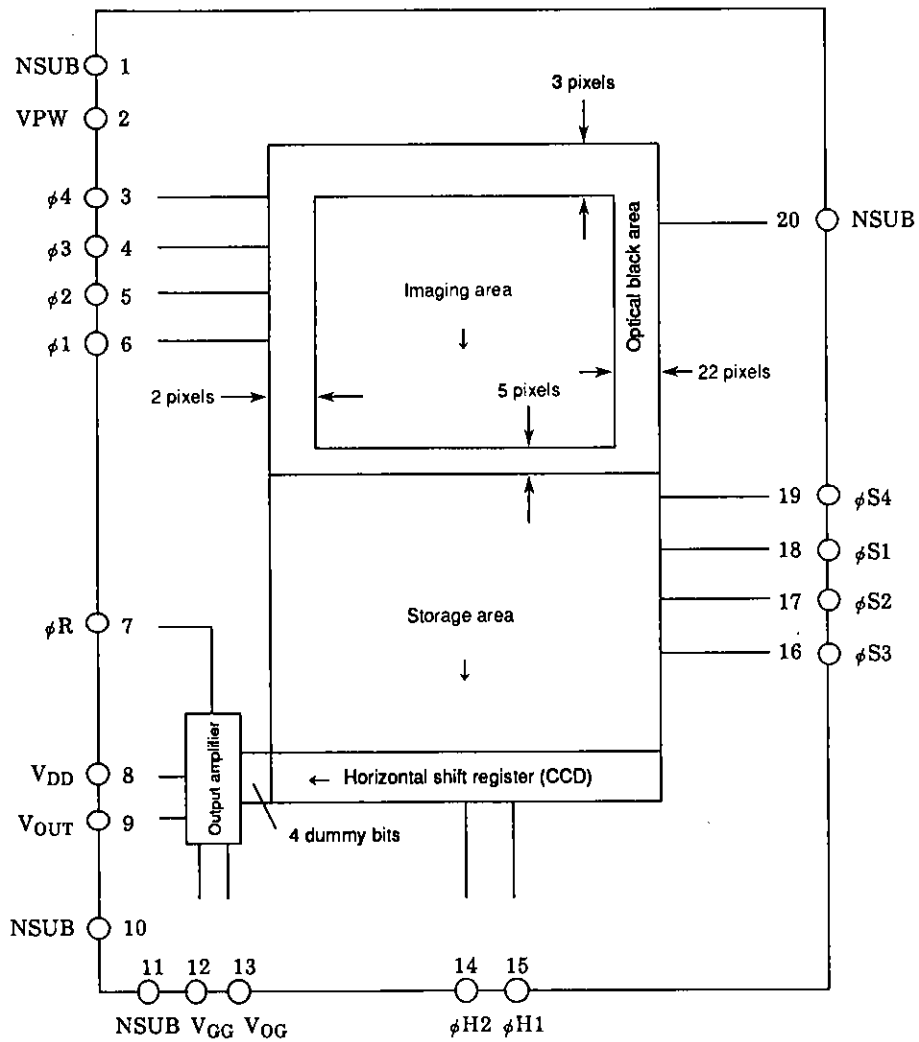
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Specifications

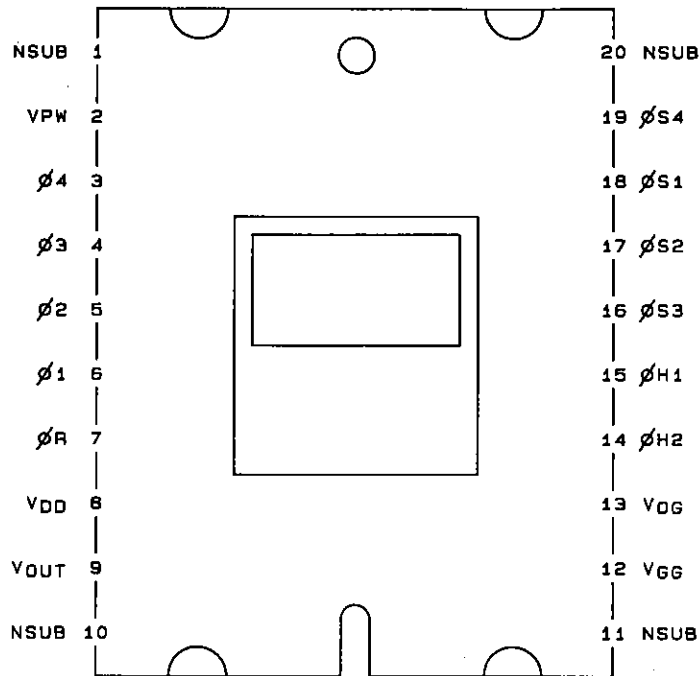
Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

| Parameter | Symbol | Conditions | Ratings | Unit |
|------------------------|----------------------|-------------------------------------|-------------|------------------|
| Maximum supply voltage | V_{DD} | $V_{PW} = 0\text{ V}$ | -0.3 to +18 | V |
| | NSUB | $V_{PW} = 0\text{ V}$ | -0.3 to +50 | V |
| | NSUB | $\phi 1$ to 4, $\phi S1$ to 4 = 0 V | -0.3 to +55 | V |
| | V_{GG} | $V_{PW} = 0\text{ V}$ | -0.3 to +5 | V |
| Horizontal clock pin | $\phi H1, 2, \phi R$ | $V_{PW} = 0\text{ V}$ | -0.3 to +18 | V |
| Other clock pins | — | $V_{PW} = 0\text{ V}$ | -15 to +18 | V |
| All other pins | — | $V_{PW} = 0\text{ V}$ | -0.3 to +10 | V |
| Operating temperature | T_{opr} | | -10 to +60 | $^\circ\text{C}$ |
| Storage temperature | T_{stg} | | -30 to +80 | $^\circ\text{C}$ |

Block Diagram



Pin Assignment



Top View

A02952

Pin Functions

| Pin No. | Symbol | Pin function | Pin No. | Symbol | Pin function |
|---------|------------------|--------------------|---------|-----------------|---------------------------------|
| 1 | NSUB | N-substrate | 20 | NSUB | N-substrate |
| 2 | VPW | P-well | 19 | øS4 | Storage area clock |
| 3 | ø4 | Imaging area clock | 18 | øS1 | Storage area clock |
| 4 | ø3 | Imaging area clock | 17 | øS2 | Storage area clock |
| 5 | ø2 | Imaging area clock | 16 | øS3 | Storage area clock |
| 6 | ø1 | Imaging area clock | 15 | øH1 | Horizontal shift register clock |
| 7 | øR | Reset gate | 14 | øH2 | Horizontal shift register clock |
| 8 | V _{DD} | Power supply | 13 | V _{OG} | CCD output gate |
| 9 | V _{OUT} | CCD output | 12 | V _{GG} | Load gate |
| 10 | NSUB | N-substrate | 11 | NSUB | N-substrate |

■ No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.

■ Anyone purchasing any products described or contained herein for an above-mentioned use shall:

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- ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.

■ Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

Clock Voltage/Frame Shift Frequency = 3.58 MHz

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|--|--------------|--------------|-------|------|------|------|
| Imaging block pulses: $\phi 1, \phi 2, \phi 3, \phi 4$ | | | | | | |
| Pulse amplitude | V_{PIF} | | 14.0 | 14.5 | 15.0 | V |
| Low level | V_{LIF} | | -10.0 | -9.5 | -9.0 | V |
| Storage block pulses: $\phi S1, \phi S2$ | | | | | | |
| Pulse amplitude | V_{PSL} | | 14.0 | 14.5 | 15.0 | V |
| Low level | V_{LSL} | | -7.0 | -6.5 | -6.0 | V |
| Storage block pulses: $\phi S3, \phi S4$ | | | | | | |
| Pulse amplitude | V_{PSL} | | 14.0 | 14.5 | 15.0 | V |
| Low level | V_{LSL} | | -7.5 | -7.0 | -6.5 | V |
| Horizontal transfer pulses: $\phi H1, \phi H2$ | | | | | | |
| Pulse amplitude | V_{PH} | | 4.5 | 5.0 | 5.5 | V |
| Low level | V_{LH} | | 0 | 0 | 0.5 | V |
| Reset gate: ϕR | | | | | | |
| Pulse amplitude | V_{PR} | | 4.5 | 5.0 | 5.5 | V |
| Low level | V_{LR} | | 4.2 | 4.5 | 4.8 | V |
| Substrate pulse: $\phi NSUB$ | | | | | | |
| High level | V_{HSUB}^* | See Figure 1 | 30.0 | | 40.0 | V |
| Low level | V_{LSUB} | See Figure 1 | 17.5 | 18.0 | 18.5 | V |

Note: Adjust the V_{HNS} saturation output to its maximum value without causing picture degradation.

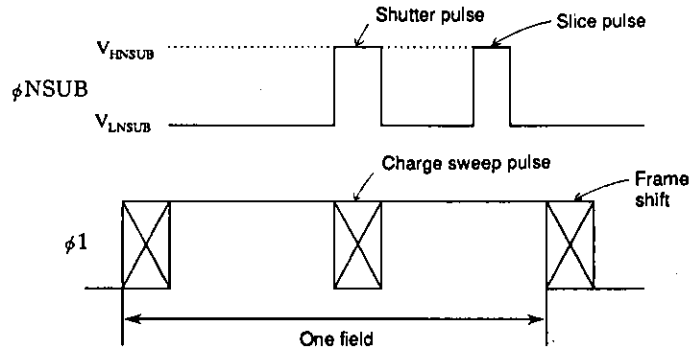


Fig. 1

Bias Conditions

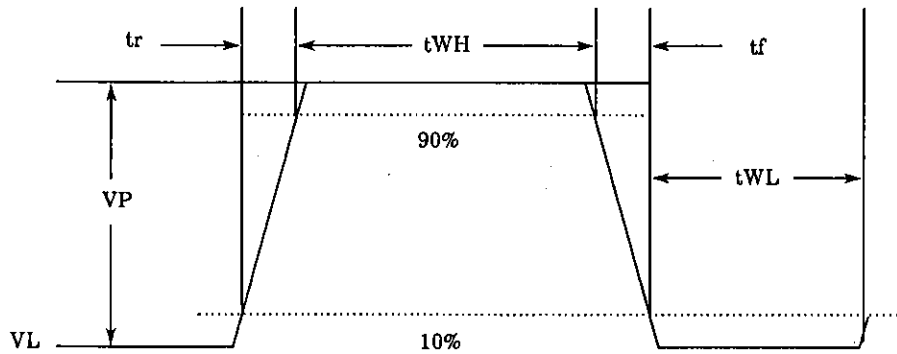
| Parameter | Symbol | Conditions | min | typ | max | Unit |
|------------------------|----------|------------|------|------|------|------|
| P-well | V_{PW} | | | 0 | | V |
| Output circuit voltage | V_{DD} | *1 | 14.5 | 15.0 | 15.5 | V |
| | V_{GG} | | 1.2 | 1.5 | 1.8 | V |
| OG bias | V_{OG} | | 4.5 | 5.0 | 5.5 | V |

Note: 1. This level must not become higher than the substrate pulse low level V_{LSUB} .

DC Characteristics

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|----------------------|----------|------------|-----|-----|------|------|
| DC operating current | I_{DD} | | 4.5 | 7.0 | 11.0 | mA |

Drive Pulse Waveform Standards



Note: VP: Pulse amplitude
VL: Low level

| Symbol | tWH | tWL | tr | tf | Unit | Notes |
|--------|------|-------|-----|------|------|---|
| | typ | typ | typ | typ | | |
| ø1 | 110 | 110 | 30 | 30 | ns | During frame transfer When the frame shift frequency is 3.58 MHz |
| ø2 | 110 | 110 | 30 | 30 | | |
| ø3 | 110 | 110 | 30 | 30 | | |
| ø4 | 110 | 110 | 30 | 30 | | |
| øS1 | 110 | 110 | 30 | 30 | ns | During frame transfer When the frame shift frequency is 3.58 MHz |
| øS2 | 110 | 110 | 30 | 30 | | |
| øS3 | 110 | 110 | 30 | 30 | | |
| øS4 | 110 | 110 | 30 | 30 | | |
| øS1 | 1.8 | 61.3 | 20 | 20 | ns | During 1H line vertical transfer The figures enclosed in dark lines are in µs units. |
| øS2 | 1.8 | 61.3 | 20 | 20 | | |
| øS3 | 61.3 | 1.8 | 20 | 20 | | |
| øS4 | 61.3 | 1.8 | 20 | 20 | | |
| øR | 17 | 80 | 4 | 4 | ns | Reset pulse |
| øH1 | 48 | 49 | 4 | 4 | | During horizontal transfer |
| øH2 | 48 | 49 | 4 | 4 | | |
| øNSUB | 7.6 | 16.6* | 2 | 0.4 | µs | Slice pulse * The units are ms |
| øNSUB | 1.0 | 16.6 | 3 | 0.05 | µs | Shutter pulse |

Imaging Characteristics at Ta = 25°C

| Parameter | Symbol | Conditions | min | typ | max | Unit |
|-----------------------------|--------|--------------------------|-----|------|-----|------|
| Sensitivity | S | Test method 1 | 110 | | | mV |
| Video signal non-uniformity | VF | Test method 2 | | | 15 | % |
| Saturated signal level | Vsat | Test method 3 | 500 | | | mV |
| Smear | SM | Test method 4* | | 0.04 | | % |
| Dark signal | Vdrk | Test method 5, Ta = 55°C | | | 7 | mV |
| γ characteristics | γ | | | 1 | | — |

Note: For a frame shift frequency of 3.58 MHz and a storage time of 1/60 s.

Test Methods

The following tests are performed with the CCD device to be measured mounted on the Sanyo evaluation board.

1. Sensitivity

Set up a CCV31F pattern box (Dai Nippon Printing Co., Ltd., intensity: 1320 NT, color temperature: 3100°K) with no pattern, and take an image with a 1 mm C-500 thickness infrared blocking filter mounted in front of a Fujinon HF16A lens. Set the lens aperture to f11, and set the separation between the lens and the pattern box to be 50 cm. Measure the CCD output signal from the center of the image in this state.

2. Video signal non-uniformity

Test this item under the following conditions.

- Standard drive state (See the specifications document.)
- Use a halogen lamp with a color temperature of 3200°K as the light source.
- Use an infrared blocking filter (C-500, 1 mm thickness).

Set the CCD surface illumination level to be 7 lux, and divide the screen into 45 blocks as shown in Figure 2.

Measure the average value in each block and determine the maximum, minimum, and mean of those values.

Determine the ratio of the difference between the maximum and minimum of the block averages to the mean of the block averages.

$$VF = \frac{(\text{block average maximum}) - (\text{block average minimum})}{(\text{block average mean})}$$

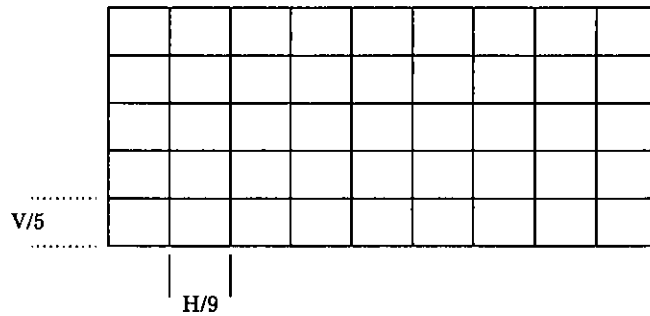


Fig. 2

3. Saturated signal level

In the test method 1 setup state, remove the lens to saturate the output signal. Measure the CCD output signal from the center of the image at this time.

4. Smear

- Place a 1/10 V chart in front of a halogen light source as described below and take the image.
- Adjust the image (input) light intensity using ND filters so that the output signal at point A, i.e., the CCD output, becomes 250 mV.
- Remove the ND filter and measure the output value for the first line (at point B) in the CCD output signal.

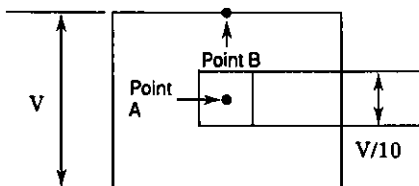


Fig. 3

$$SM = \frac{VB \times TND}{250} \times 100 (\%)$$

VB: The amount of smear (mV) at point B

TND: Transmittance of the ND filter

5. Dark signal

Block all light falling on the imaging element surface and measure the CCD output signal from the center of the image. At this time, do not take the difference between the signal level and the optical black segment level, but rather take the difference with the no signal level that has no pixel information. See Figure 4.

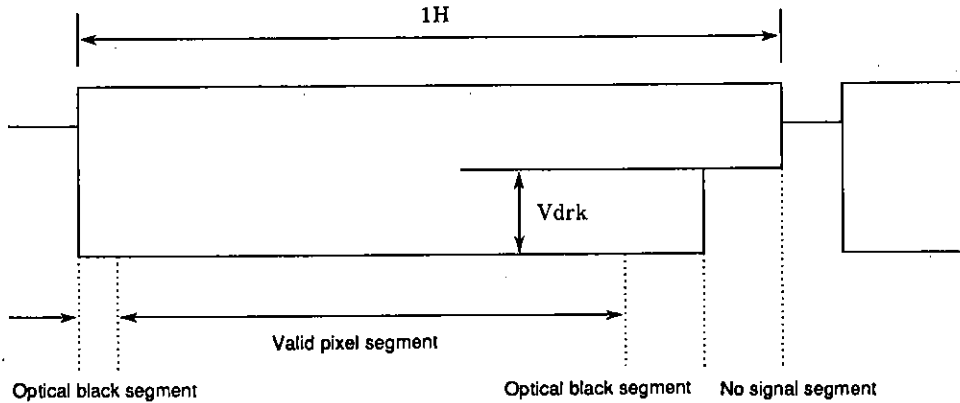


Fig. 4 Structure of the 1H Period

CCD B&W Camera Block Diagram

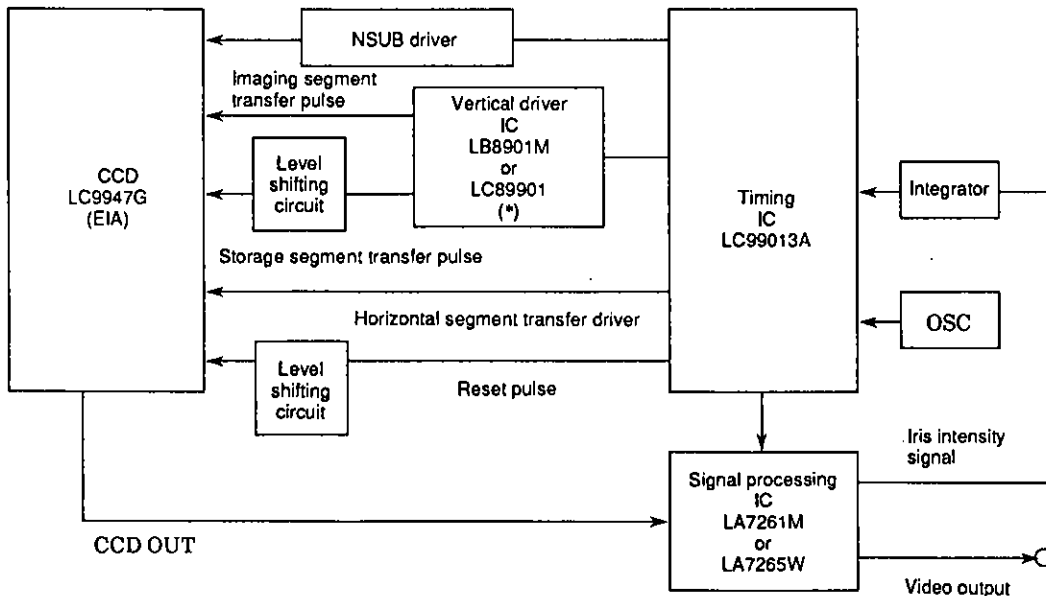


Fig. 5 CCD B&W Camera Block Diagram

Block Descriptions

| | |
|---------------------------|--|
| OSC | Generates the basic frequency (28.636 MHz) for synchronization signals and timing pulses |
| Timing pulse generator IC | Generates the pulses required for the video signal (SYNC, blanking, etc.) and the pulses required for driving the CCD. This IC includes a built-in CCD horizontal driver and provides an electronic iris function. |
| Driver IC | Amplifies the pulses described above to their prescribed levels and drives the CCD device. |
| Level shifting circuit | Drive pulse level shifter |
| Signal processing IC | Video signal processing, including sample and hold, clamping, AGC, gamma correction, white clipping, and pedestal addition. |

Notes on Handling and Mounting

1. Static discharge prevention

The following measure for static discharge prevention must be taken, since the sensor is easily destroyed by static discharges.

- Personnel and all equipment must be grounded when handling the sensor. For safety, personnel should be grounded through a resistor of about 1 M Ω . (The use of wrist straps is recommended.)
- Work should be performed either with bare hands or antistatic gloves. Antistatic work uniforms should be used. Also, conductive shoes should be worn.
- Spread conductive mats on the work place floors and on workbenches so that static charges do not arise.
- We recommend using an ionized air blower to remove static charges when handling CCD sensors.
- Use antistatic processed boxes to transport printed circuit boards with mounted CCD devices.

2. Soldering

- The package temperature must never exceed 80°C.
- In addition to static discharges, CCD sensors are also easily destroyed by thermal stress. The soldering iron tip temperature should be under 300°C when mounting on a printed circuit board, and 2 seconds per pin should be set as the target soldering time.
- Only use soldering irons that have a temperature controller that holds the soldering iron tip at a fixed temperature.
- Use extra care to avoid heating the element to over 80°C when re-soldering or removing a CCD element.

3. Dirt and contamination

- Work should be performed in a clean environment. (A class 1000 level is appropriate.)
- Do not touch the package surface or allow any objects to contact the surface. If dirt or other contamination gets on the package surface remove it with an air blower. (We recommend the use of an ionized air blower if possible.)
- Oily or greasy contamination can be removed with a cotton swab dipped in ethyl alcohol. Be extremely careful not to scratch the package surface.
- Store CCD devices in their special-purpose cases to avoid dirt and other contamination and to prevent condensation when transporting into a room with a radically differing temperature, warm or cool the device in advance.
- For devices supplied with protective tape, remove the tape immediately prior to use **only after thorough antistatic measures have been implemented**. Do not reuse the protective tape.

4. Storage methods

- Do not subject CCD products to intense light for extended periods.
- Since severe high temperature/high humidity conditions can adversely influence device characteristics, avoid storing CCD products in such environments.
- Since CCD sensors are high precision optical components, they must be protected from mechanical shocks.

5. Notes on mounting

- The use of a lens with an optical size of over 1/5 inch can result in flare. Consult your Sanyo sales representative before selecting a lens.
- This product is mounted in a fully clear plastic package, and is susceptible to light entering from the back of the printed circuit board that it is mounted on. Therefore end products must provide adequate protection from stray light.