LF2247
Image Filter with Coefficient RAM

LOGIC DEVICES INCORPORATED

FEATURES

- 66 MHz Data Input and Computation Rate
- Four 11 x 10-bit Multipliers with Individual Data and Coefficient Inputs and a 25-bit Accumulator
- Four 32 x 11-bit Serially Loadable Coefficient Registers
- Fractional or Integer Two's Complement Operands
- Package Styles Available:
  - 84-pin PLCC, J-Lead
  - 100-pin PQFP

DESCRIPTION

The **LF2247** consists of an array of four 11 x 10-bit registered multipliers followed by a summer and a 25-bit accumulator. The LF2247 provides a coefficient register file containing four 32 x 11-bit registers which are capable of storing 32 different sets of filter coefficients for the multiplier array. All multiplier data inputs are user accessible and can be updated every clock cycle with either fractional or integer two's complement data. The pipelined architecture has fully registered input and output ports and an asynchronous three-state output enable control to simplify the design of complex systems. The pipeline latency for all inputs is five clock cycles.

A 25-bit accumulator path allows cumulative word growth which may be internally rounded to 16 bits. Output data is updated every clock cycle and may be held under user control. The data inputs/outputs and control inputs are registered on the rising edge of CLK. The Serial Data In signal, SDIN, is registered on the

LF2247 BLOCK DIAGRAM

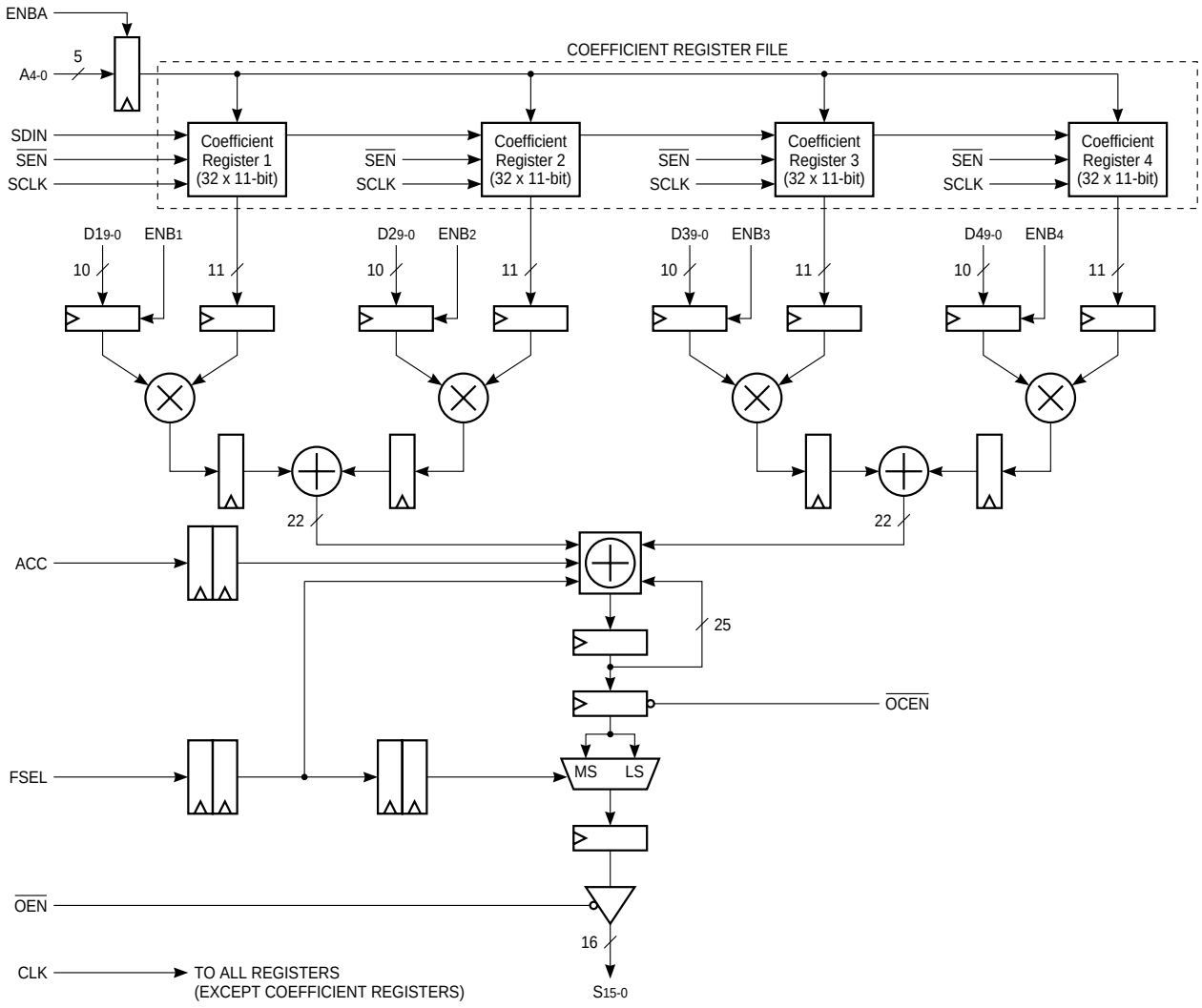


FIGURE 1A. INPUT FORMATS

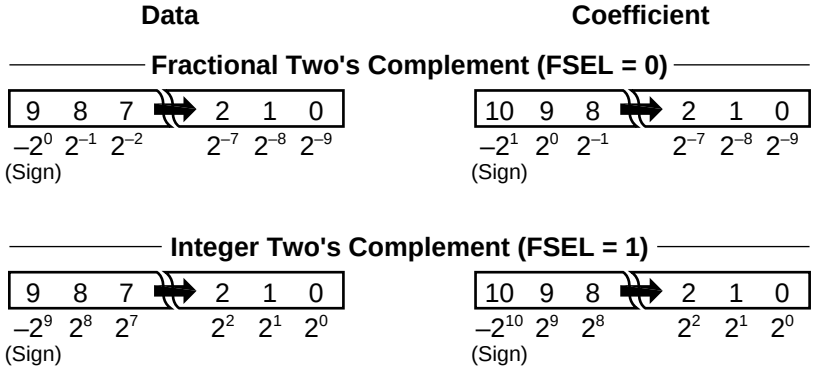
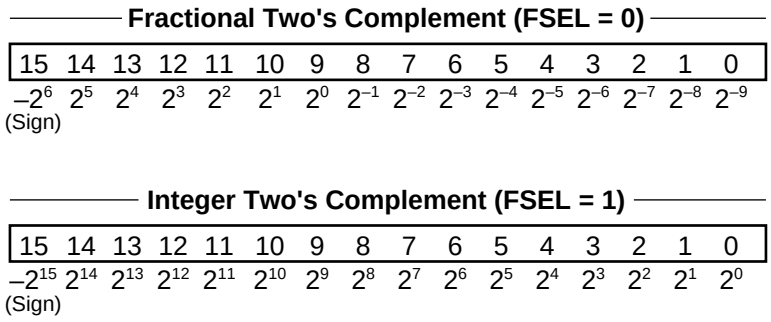


FIGURE 1B. OUTPUT FORMATS



rising edge of SCLK. The LF2247 operates at a clock rate of 66 MHz over the full temperature and supply voltage ranges.

The LF2247 is applicable for performing pixel interpolation in image manipulation and filtering applications. The LF2247 can perform a bilinear interpolation of an image (4-pixel kernels) at real-time video rates when used with an image resampling sequencer. Larger kernels or more complex functions can be realized by utilizing multiple devices.

Unrestricted access to all data ports and an addressable coefficient register file provides the LF2247 with considerable flexibility in applications such as digital filters, adaptive FIR filters, mixers, and other similar systems requiring high-speed processing.

SIGNAL DEFINITIONS

Power

V_{CC} and GND

+5 V power supply. All pins must be connected.

Clocks

CLK — Master Clock

The rising edge of CLK strobes all enabled registers except for the coefficient registers.

SCLK — Serial Clock

The rising edge of SCLK shifts data into and through the coefficient register file when it is enabled for serial data shifting.

Inputs

$D1_{9-0}$ – $D4_{9-0}$ — Data Input

D1–D4 are the 10-bit registered data input ports. Data is latched on the rising edge of CLK.

A_{4-0} — Row Address

A_{4-0} determines which row of data in the coefficient register file is used to feed data to the multiplier array. A_{4-0} is latched on the rising edge of CLK. When a new row address is loaded into the row address register, data from the register file will be latched into the multiplier input registers on the next rising edge of CLK.

SDIN — Serial Data Input

SDIN is used to serially load data into the coefficient registers. Data present on SDIN is shifted into the coefficient register file on the rising edge of SCLK when $\overline{SEN}$ is LOW. The 11-bit coefficients are loaded into the coefficient register file in 16-bit words as shown in Figure 2. The five most significant bits of the first 16-bit word determine which row the data is written to in the coefficient registers. Note that the five most significant bits of the remaining three 16-bit words are ignored. After all four 16-bit words are shifted into the register file, the lower eleven bits of each word (the coefficient data) are stored into the coefficient registers.

Outputs

S_{15-0} — Data Output

S_{15-0} is the 16-bit registered data output port.

Controls

ENB_1–ENB_4 — Data Input Enables

The ENB_N (N = 1, 2, 3, or 4) inputs allow the DN registers to be updated on each clock cycle. When ENB_N is LOW, data on DN_{9-0} is latched into

the DN register on the rising edge of CLK. When ENBN is HIGH, data on DN9-0 is not latched into the DN register and the register contents will not be changed.

ENBA — Row Address Input Enable

The ENBA input allows the row address register to be updated on each clock cycle. When ENBA is LOW, data on A4-0 is latched into the row address register on the rising edge of CLK. When ENBA is HIGH, data on A4-0 is not latched into the row address register and the register contents will not be changed.

$\overline{OEN}$ — Output Enable

When $\overline{OEN}$ is LOW, S15-0 is enabled for output. When $\overline{OEN}$ is HIGH, S15-0 is placed in a high-impedance state.

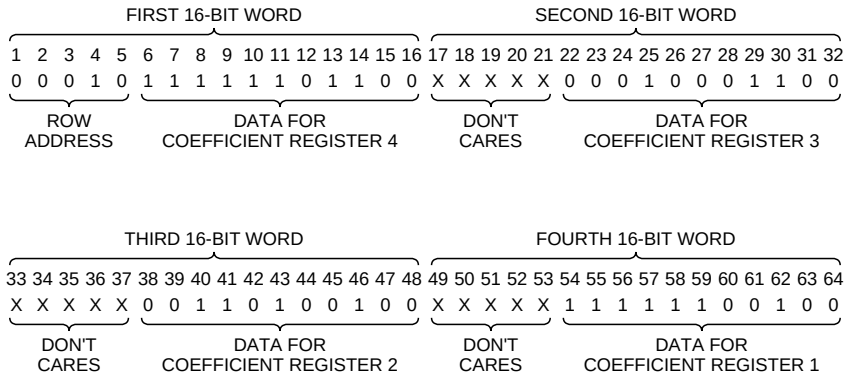
$\overline{OCEN}$ — Clock Enable

When $\overline{OCEN}$ is LOW, data in the pre-mux register (accumulator output) is loaded into the output register on the next rising edge of CLK. When $\overline{OCEN}$ is HIGH, data in the pre-mux register is held preventing the output register's contents from changing (if FSEL does not change). Accumulation continues internally as long as ACC is HIGH, despite the state of $\overline{OCEN}$.

FSEL — Format Select

When FSEL is LOW, the data input during the current clock cycle is assumed to be in fractional two's complement format, and the upper 16 bits of the accumulator are presented at the output. Rounding of the accumulator result to 16 bits is performed if the accumulator control input ACC is LOW. When FSEL is HIGH, the data input is assumed to be in integer two's complement format, and the lower 16 bits of the accumulator are presented at the output. No rounding is performed when FSEL is HIGH.

FIGURE 2. SERIAL DATA FORMAT



SHOWN IS SERIAL DATA STREAM TO LOAD ROW ADDRESS 2 WITH:
COEFFICIENT REGISTER 1 = 7E4
COEFFICIENT REGISTER 2 = 1A4
COEFFICIENT REGISTER 3 = 08C
COEFFICIENT REGISTER 4 = 7EC

ACC — Accumulator Control

The ACC input determines whether internal accumulation is performed on the data input during the current clock cycle. If ACC is LOW, no accumulation is performed, the prior accumulated sum is cleared, and the current sum of products is output. If FSEL is also LOW, one-half LSB rounding to 16 bits is performed on the result. When ACC is HIGH, the emerging product is added to the sum of the previous products, without additional rounding.

$\overline{SEN}$ — Serial Input Enable

The $\overline{SEN}$ input enables the shifting of serial data through the registers in the coefficient register file. When $\overline{SEN}$ is LOW, serial data on SDIN is shifted into the coefficient register file on the rising edge of SCLK. $\overline{SEN}$ must remain LOW until all four coefficients have been clocked in. $\overline{SEN}$ does not need to be pulsed between consecutive data sets. It can remain LOW while the entire register file is loaded by a constant bit stream. When $\overline{SEN}$ is HIGH, data can not be shifted into the register file and the register file's contents will not be changed. When enabling the coefficient register file for serial data input, the LF2247 requires a HIGH to LOW transition of $\overline{SEN}$ in order to function properly. Therefore, $\overline{SEN}$ needs to be set HIGH immediately after power up to ensure proper operation of the serial input circuitry.

MAXIMUM RATINGS *Above which useful life may be impaired (Notes 1, 2, 3, 8)*

Storage temperature ..... –65°C to +150°C
Operating ambient temperature ..... –55°C to +125°C
V_{CC} supply voltage with respect to ground ..... –0.5 V to +7.0 V
Input signal with respect to ground ..... –0.5 V to V_{CC} + 0.5 V
Signal applied to high impedance output ..... –0.5 V to V_{CC} + 0.5 V
Output current into low outputs ..... 25 mA
Latchup current ..... > 400 mA

OPERATING CONDITIONS *To meet specified electrical and switching characteristics*

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation, Commercial	0°C to +70°C	4.75 V ≤ V_{CC} ≤ 5.25 V
Active Operation, Military	–55°C to +125°C	4.50 V ≤ V_{CC} ≤ 5.50 V

ELECTRICAL CHARACTERISTICS *Over Operating Conditions (Note 4)*

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –2.0 mA	2.4			V
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 4.0 mA			0.4	V
V_{IH}	Input High Voltage		2.0		V_{CC}	V
V_{IL}	Input Low Voltage	(Note 3)	0.0		0.8	V
I_{IX}	Input Current	Ground ≤ V_{IN} ≤ V_{CC} (Note 12)			±10	µA
I_{OZ}	Output Leakage Current	Ground ≤ V_{OUT} ≤ V_{CC} (Note 12)			±40	µA
I_{CC1}	V_{CC} Current, Dynamic	(Notes 5, 6)			100	mA
I_{CC2}	V_{CC} Current, Quiescent	(Note 7)			6.0	mA
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz			10	pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1 MHz			10	pF

SWITCHING CHARACTERISTICS

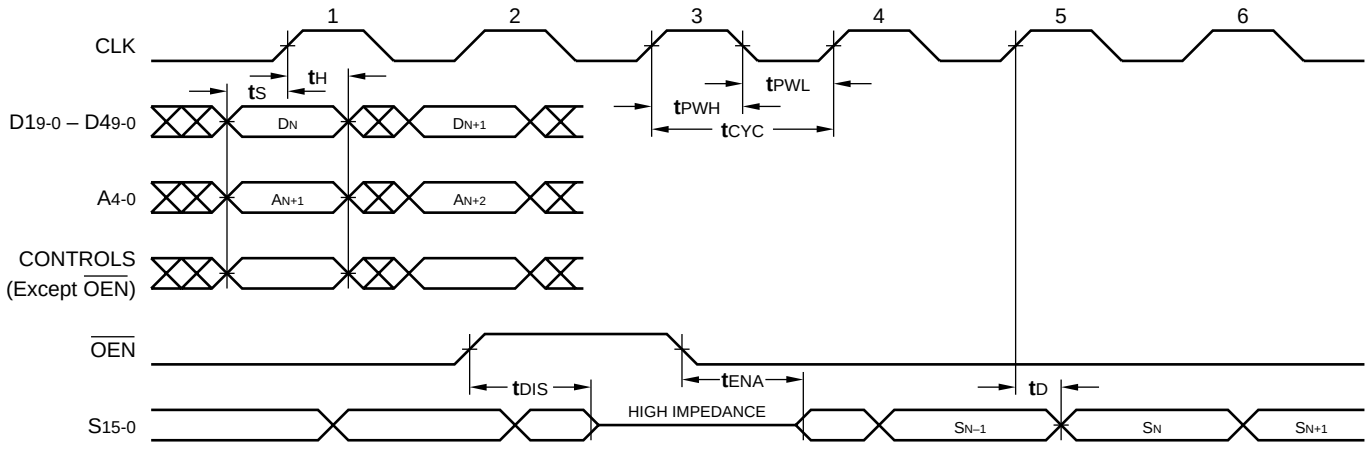
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2247–					
		33*		25		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25		15	
t_{PWL}	Clock Pulse Width Low	15		10		7	
t_{PWH}	Clock Pulse Width High	10		10		7	
t_S	Input Setup Time	10		8		5	
t_H	Input Hold Time	0		0		0	
t_D	Output Delay		15		13		11
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15		15

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2247–			
		33*		25*	
Symbol	Parameter	Min	Max	Min	Max
t_{CYC}	Cycle Time	33		25	
t_{PWL}	Clock Pulse Width Low	15		10	
t_{PWH}	Clock Pulse Width High	10		10	
t_S	Input Setup Time	10		8	
t_H	Input Hold Time	0		0	
t_D	Output Delay		15		13
t_{DIS}	Three-State Output Disable Delay (Note 11)		15		15
t_{ENA}	Three-State Output Enable Delay (Note 11)		15		15

SWITCHING WAVEFORMS: DATA I/O



*DISCONTINUED SPEED GRADE

SWITCHING CHARACTERISTICS

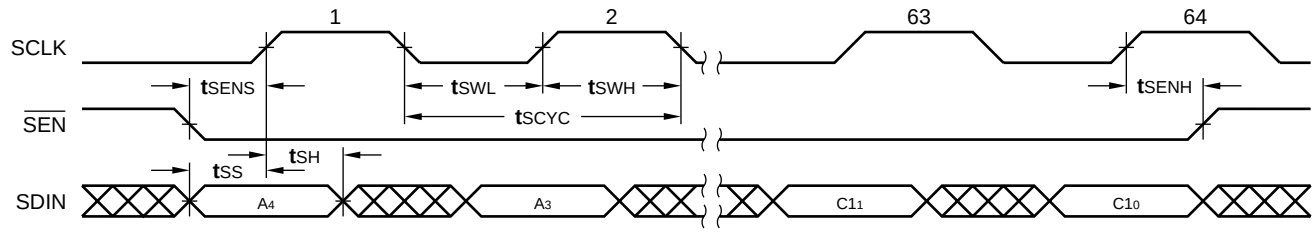
COMMERCIAL OPERATING RANGE (0°C to +70°C) *Notes 9, 10 (ns)*

		LF2247–					
		33*		25		15	
Symbol	Parameter	Min	Max	Min	Max	Min	Max
t_{SCYC}	Serial Interface Cycle Time	62		62		62	
t_{SWL}	Serial Clock Pulse Width Low	30		30		30	
t_{SWH}	Serial Clock Pulse Width High	30		30		30	
t_{SENS}	Serial Enable Setup Time	20		20		20	
t_{SENH}	Serial Enable Hold Time	0		0		0	
t_{SS}	Serial Data Input Setup Time	20		20		20	
t_{SH}	Serial Data Input Hold Time	0		0		0	

MILITARY OPERATING RANGE (–55°C to +125°C) *Notes 9, 10 (ns)*

		LF2247–			
		33*		25*	
Symbol	Parameter	Min	Max	Min	Max
t_{SCYC}	Serial Interface Cycle Time	62		62	
t_{SWL}	Serial Clock Pulse Width Low	30		30	
t_{SWH}	Serial Clock Pulse Width High	30		30	
t_{SENS}	Serial Enable Setup Time	20		20	
t_{SENH}	Serial Enable Hold Time	0		0	
t_{SS}	Serial Data Input Setup Time	20		20	
t_{SH}	Serial Data Input Hold Time	0		0	

SWITCHING WAVEFORMS: SERIAL DATA INPUT



*DISCONTINUED SPEED GRADE

NOTES

1. Maximum Ratings indicate stress specifications only. Functional operation of these products at values beyond those indicated in the Operating Conditions table is not implied. Exposure to maximum rating conditions for extended periods may affect reliability.

2. The products described by this specification include internal circuitry designed to protect the chip from damaging substrate injection currents and accumulations of static charge. Nevertheless, conventional precautions should be observed during storage, handling, and use of these circuits in order to avoid exposure to excessive electrical stress values.

3. This device provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at –0.6 V and V_{CC} + 0.6 V. The device can withstand indefinite operation with inputs in the range of –0.5 V to +7.0 V. Device operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

4. Actual test conditions may vary from those designated but operation is guaranteed as specified.

5. Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

6. Tested with all outputs changing every cycle and no load, at a 30 MHz clock rate.

7. Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

8. These parameters are guaranteed but not 100% tested.

9. AC specifications are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current sources of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed.

This device has high-speed outputs capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result, care must be exercised in the testing of this device. The following measures are recommended:

a. A 0.1 µF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Device Under Test (DUT) as possible. Similar capacitors should be installed between device V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or contactor fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain required DUT input levels relative to the DUT ground pin.

10. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

11. For the t_{ENA} test, the transition is measured to the 1.5 V crossing point with datasheet loads. For the t_{DIS} test, the transition is measured to the ±200mV level from the measured steady-state output voltage with ±10mA loads. The balancing voltage, V_{TH}, is set at 3.5 V for Z-to-0 and 0-to-Z tests, and set at 0 V for Z-to-1 and 1-to-Z tests.

12. These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

FIGURE A. OUTPUT LOADING CIRCUIT

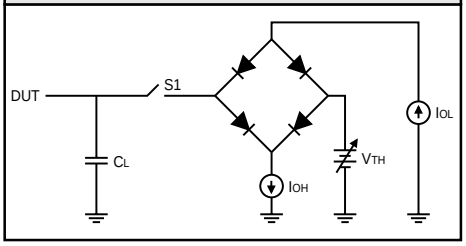
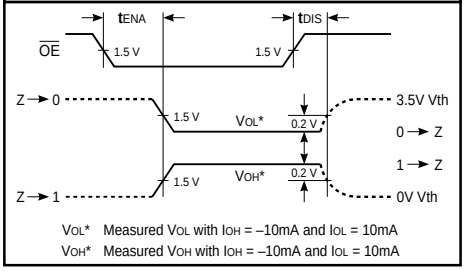
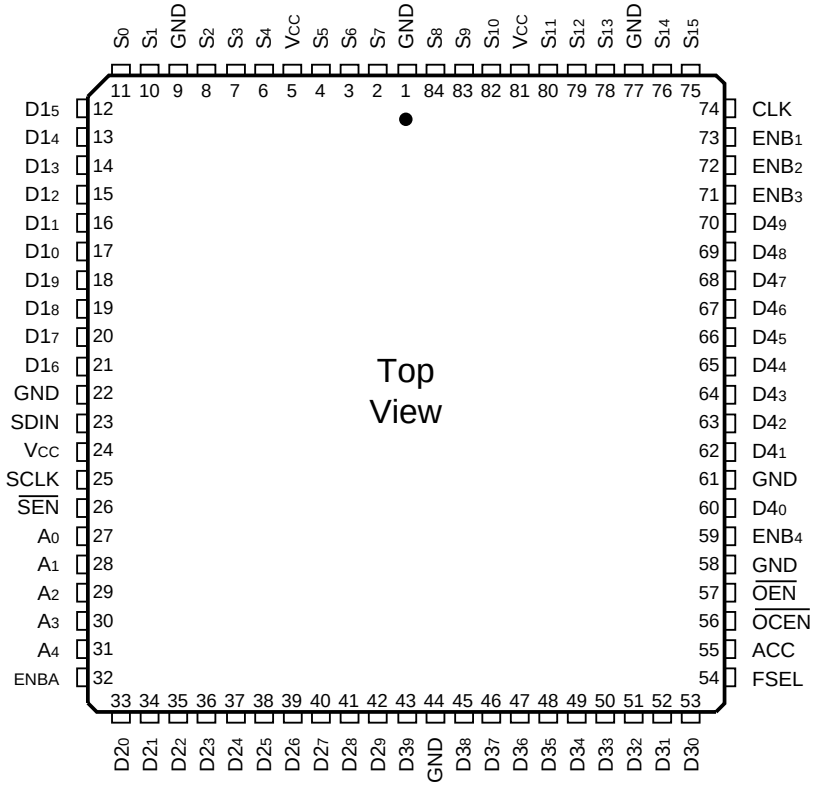


FIGURE B. THRESHOLD LEVELS



ORDERING INFORMATION

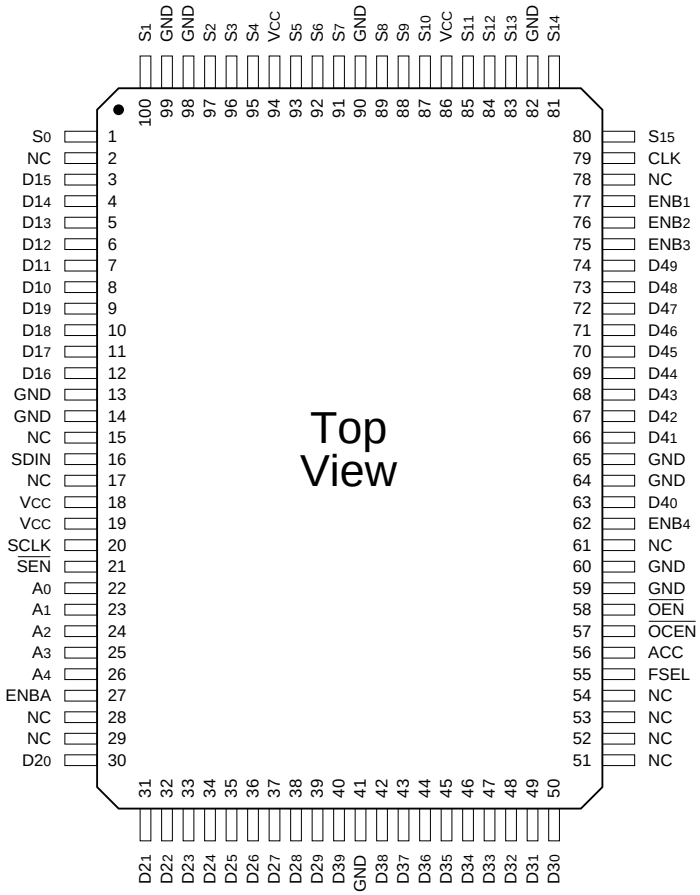
84-pin



Speed	Plastic J-Lead Chip Carrier (J3)
	0°C to +70°C — COMMERCIAL SCREENING
15 ns	LF2247JC15

ORDERING INFORMATION

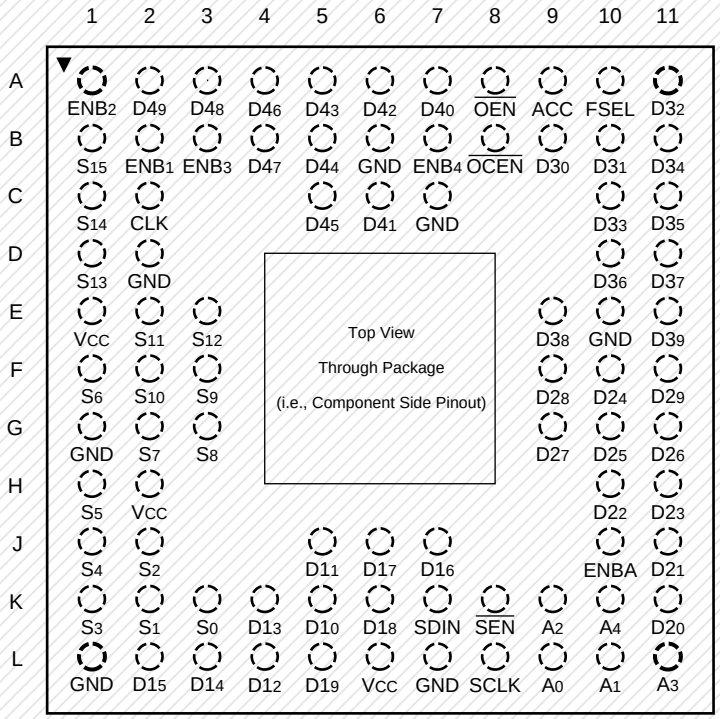
100-pin



Speed	Plastic Quad Flatpack (Q2)
	0°C to +70°C — COMMERCIAL SCREENING
25 ns	LF2247QC25
15 ns	LF2247QC15

ORDERING INFORMATION

84-pin



Discontinued Package

Speed	Ceramic Pin Grid Array (G3)
	0°C to +70°C — COMMERCIAL SCREENING
	–55°C to +125°C — COMMERCIAL SCREENING
	–55°C to +125°C — MIL-STD-883 COMPLIANT