



# LH4004/LH4004C Wideband FET-Input Buffer/Amplifier

## General Description

The LH4004 is an FET input, high speed differential amplifier optimized for unity gain applications. It eliminates most of the drawbacks of conventional open loop buffers and does not require compensation for unity and other low gain operations. It is an ideal choice for video distribution, driving flash converters, and summing amplifiers. Furthermore, the bandwidth does not decrease with increasing gain. At a closed loop gain of 4, the LH4004 still offers a 75 MHz bandwidth.

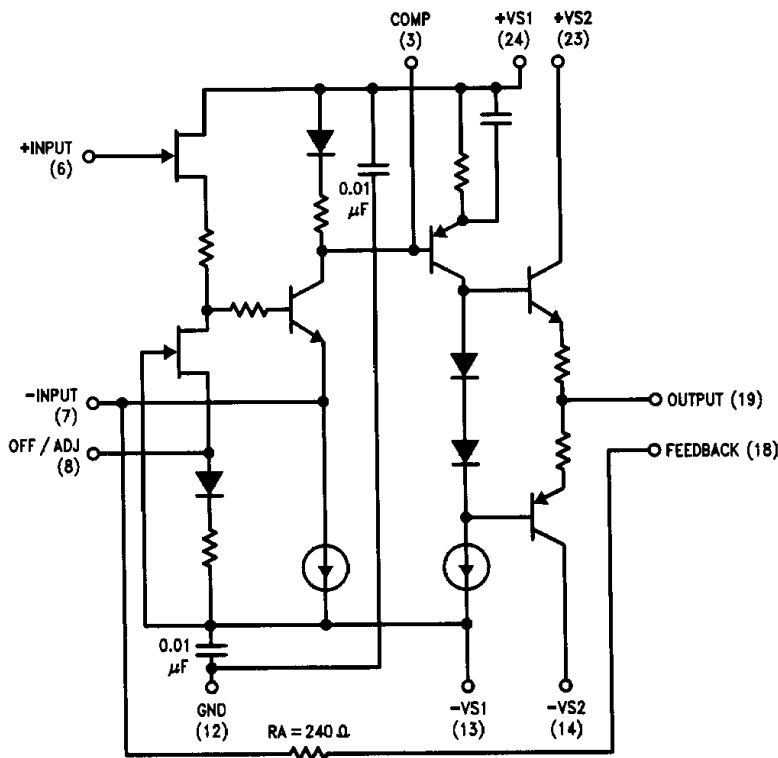
## Features

- $\pm 0.5$  dB gain flatness
- 500 V/ $\mu$ s slew rate
- Drives 50 $\Omega$  directly
- 140 MHz bandwidth
- No external components required for unity gain operation
- Internal power supply bypassing

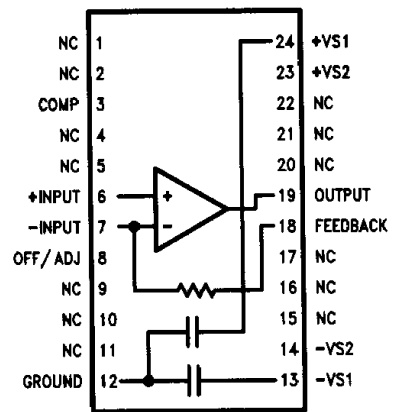
## Applications

- Unity gain buffer
- Low gain op amp

## Simplified Schematic and Connection Diagram



TL/K/8831-1



TL/K/8831-2

**Top View**  
**Order Number**  
**LH4004CD or LH4004D**  
**See NS Package Number D24D**

## Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, $V_S$	$\pm 15V$
Power Dissipation, $P_D$	
$T_A = 25^\circ C$ , derate linearly at $80^\circ C/W$	1.8W
$T_C = 25^\circ C$ , derate linearly at $40^\circ C/W$	3.75W
Input Voltage Range, $V_{IN}$	$\pm V_S$

Operating Temperature Range, $T_A$	
LH4004CD	$-25^\circ C$ to $+85^\circ C$
LH4004D	$-55^\circ C$ to $+125^\circ C$
Storage Temperature Range, $T_{STG}$	$-65^\circ C$ to $+150^\circ C$
Maximum Junction Temperature, $T_J$	$150^\circ C$
Lead Temperature (Soldering, $< 10$ sec)	$300^\circ C$
ESD rating is to be determined.	

## DC Electrical Characteristics $V_S = \pm 12V, R_S = R_L = 50\Omega, T_A = 25^\circ C$ unless otherwise noted (Note 1)

Symbol	Parameter	Conditions	LH4004C			Units (Max Unless Otherwise Stated)	
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)		
$V_{OS}$	Input Offset Voltage	$V_{IN} = 0V, T_A = T_J = 25^\circ C$	8	15		mV	
$V_{OS}/\Delta T$	Offset Voltage Drift	(Note 4)	300			$\mu V/^\circ C$	
$I_B$	Input Bias Current	$T_J = 25^\circ C$ , Pin 6 (Note 4)		400		pA	
	Gain Accuracy	$V_{IN} = \pm 1V$ $A_V = +1$	$R_L = 500\Omega$	0.98	0.96	<b>0.93</b>	V/V
			$R_L = 50\Omega$	0.98	0.96	<b>0.93</b>	(Min)
$V_O$	Output Voltage Swing	$V_{IN} = \pm 10V$	$R_L = 500\Omega$	9.6	9.2	9.2	V (Min)
$V_O$	Output Voltage Current Swing	$V_{IN} = \pm 5V, R_L = 50\Omega$		$\pm 4.5$	$\pm 4$		V (Min)
$I_S$	Supply Current			35	40		mA
PSRR	Power Supply Rejection Ratio	$\pm V_S = \pm 11V$ to $\pm 15V$			40		dB (Min)

## AC Electrical Characteristics $V_S = \pm 12V, R_S = R_L = 50\Omega, T_A = 25^\circ C$ (unless otherwise noted)

Symbol	Parameter	Conditions	LH4004C			Units (Max Unless Otherwise Stated)	
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)		
$t_r$	Small Signal Rise Time	$\Delta V_{IN} = 0.5V$	3			ns	
$t_s$	Settling Time to 0.5%	$V_{IN} = -2.5V$ to $+2.5V$	30			ns	
$f_{-3dB}$	Small Signal Bandwidth	$V_{IN} = -10$ dBm	$A_V = +1$	140	125		MHz
			$A_V = +4$	85	75		(Min)
	Large Signal Bandwidth	$V_{OUT} = \pm 2.5V$	$A_V = +1$		70		MHz
	Gain Flatness	$V_{IN} = -10$ dBm $A_V = +1$ $f = 0-50$ MHz		$\pm 0.5$			dB
	Harmonic Distortion	Second Order $V_{IN} = 4V_{p-p}, f_{IN} = 10$ MHz					dB
SR	Slew Rate	$V_{IN} = -2.5V$ to $+2.5V$	1500		1200		V/ $\mu s$
		$V_{IN} = +2.5V$ to $-2.5V$	600		500		(Min)

**DC Electrical Characteristics** $V_S = \pm 12V$ ,  $R_S = R_L = 50\Omega$ ,  $T_A = 25^\circ C$  unless otherwise noted (Notes 1 & 5)

Symbol	Parameter	Conditions	LH4004			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
$V_{OS}$	Input Offset Voltage	$T_A = T_J = 25^\circ C$ (Note 4)	8	15		mV
$V_{OS}/\Delta T$	Offset Voltage Drift		300			$\mu V/^\circ C$
$I_B$	Input Bias Current	$T_A = T_J = 25^\circ C$ , Pin 6 (Note 4)		400		pA
				<b>400</b>		nA
	Gain Accuracy	$V_{IN} = \pm 1V$ $A_V = +1$	$R_L = 500\Omega$	0.98	0.96	V/V (Min)
				<b>0.93</b>		
			$R_L = 50\Omega$	0.98	0.96	
				<b>0.93</b>		
$V_O$	Output Voltage Swing	$V_{IN} = \pm 10V$	$R_L = 500\Omega$	9.6	9.2	V (Min)
$V_O$	Output Voltage Swing	$V_{IN} = \pm 5V$ , $R_L = 50\Omega$		$\pm 4.5$	$\pm 4$	V (Min)
$I_S$	Supply Current			35	40	
PSRR	Power Supply Rejection Ratio				<b>40</b>	dB (Min)

**AC Electrical Characteristics**  $V_S = \pm 12V$ ,  $R_S = R_L = 50\Omega$ ,  $T_A = 25^\circ C$  unless otherwise noted

Symbol	Parameter	Conditions	LH4004			Units (Max Unless Otherwise Stated)
			Typ	Tested Limit (Note 2)	Design Limit (Note 3)	
$t_r$	Small Signal Rise Time	$\Delta V_{IN} = 0.5V$	3			ns
$t_s$	Settling Time to 0.5%	$V_{IN} = -2.5V$ to $+2.5V$	30			ns
$f_{-3dB}$	Small Signal Bandwidth	$V_{IN} = -10$ dBm	$A_V = +1$	125		MHz (Min)
			$A_V = +4$	75		
	Large Signal Bandwidth	$V_{OUT} = \pm 2.5V$	$A_V = +1$	70		MHz
	Gain Flatness	$V_{IN} = 100$ mV p-p $A_V = +1$ $f = 0-50$ MHz		$\pm 0.5$		dB
	Harmonic Distortion	Second Order $V_{IN} = 4V$ p-p, $f_{IN} = 10$ MHz				dB
SR	Slew Rate	$V_{IN} = -2.5V$ to $+2.5V$	1500		1200	V/ $\mu s$ (Min)
		$V_{IN} = +2.5V$ to $-2.5V$	600		500	

**Note 1:** Boldface limits are guaranteed over full temperature range. Operating ambient temperature range of LH4004C is  $-25^\circ C$  to  $+85^\circ C$ , and LH4004 is  $-55^\circ C$  to  $+125^\circ C$ .

**Note 2:** Tested limits are guaranteed and 100% production tested.

**Note 3:** Design limits are guaranteed (but not 100% production tested) over the indicated temperature range. These limits are not used to calculate outgoing quality levels.

**Note 4:** Specification is at  $25^\circ C$  junction temperature due to requirements of high speed automatic testing. Actual values at operating temperature will exceed value at  $T_J = 25^\circ C$ .

**Note 5:** When the LH4004 is operated at elevated temperature (such as  $125^\circ C$ ), some form of heat sinking or forced air cooling is required. The quiescent power with  $V_S$  of  $\pm 12V$  is 960 mW, whereas the package is only rated to 800 mW without a heatsink at  $125^\circ C$ .

## Application Hints

The front page figure shows the simplified schematic which includes the feedback resistor and the decoupling capacitors.

The essential difference from other op amps is that both inputs are radically different, the non-inverting input goes to a FET buffer follower and the inverting input is connected to the second stage emitter node. This topology is responsible for the unique bandwidth characteristic and transfer function of the amplifier.

Let's consider the connection diagram of *Figure 1*. The typical transfer function in the case of a classical op amp would be:

$$\frac{V_{OUT}}{V_{IN}} = \frac{K(s)}{1 + K(s)/B}$$

where  $B = \frac{R_A + R_B}{R_B}$  and  $K(s)$  is the open loop gain of the amplifier and is frequency dependent. By rearranging the formula, we find;

$$(1) \frac{V_{OUT}}{V_{IN}} = B \cdot \frac{K(s)}{K(s) + B}$$

For the LH4004, a small signal analysis shows that the difference between the two inputs turns the previous typical equation into:

$$(2) \frac{V_{OUT}}{V_{IN}} = B \cdot \frac{K(s)}{K(s) + B + m R_A}$$

where  $m$  is an internal parameter to the device and  $K(s)$  is approximately 70 dB at DC with a 50Ω load.

In both equations, the second term is negligible when the open loop gain of the amplifier,  $K(s)$ , approaches infinity, but in equation (1), when the signal frequency reaches a point where  $K(s)$  is small, say  $K(s) = 10$  or less, then the term will be very sensitive to the value of the closed loop gain  $B$  and  $V_{OUT}/V_{IN}$  will fall earlier as  $B$  increases.

In equation (2),  $m$  is approximately 0.19 and  $R_A$  is provided inside the package, with a value which has been chosen to be 240Ω. The term  $mR_A$  is therefore equal to 46 and will dominate the term  $B$  as long as it is kept below 5. The result is that  $V_{OUT}/V_{IN}$  will not be as dependent on  $B$  as with traditional topologies. The gain will still fall with the open loop gain  $K(s)$  as the frequency increases, but the roll off will be virtually independent of the closed loop gain  $B$ .

Resistor  $R_B$  sets the overall closed loop gain, but has very little effect on stability and bandwidth. Another peculiarity of the LH4004 is that the loop compensation can be accomplished by changing the value of resistor  $R_A$  (*Figure 2*). Even though this such as settling time, overshoot and phase margin, it will not affect the slew rate. Although this resistive compensation scheme is adequate in most cases, an alternate method is to place a capacitor between pins 3 and 19 (*Figure 3*). This method of compensation also reduces the device slew rate (*Figure 4*).

## Low Gain Operation

The small amount of stray capacitance present at the inverting input can cause peaking which increases with decreasing gain. The gain set resistor  $R_B$  (in *Figure 1*) is effectively

in parallel with this capacitance and so a frequency domain pole results. With a small  $R_B$ , this pole is at a high frequency and it affects the closed loop gain of the LH4004 only slightly. At lower values of gain, this pole becomes significant. For example, at a gain of +2, the gain may peak as much as 1.5 dB to 2 dB at 100 MHz.

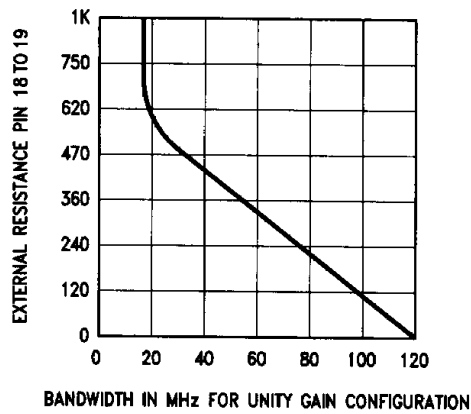


FIGURE 2. Bandwidth vs  $R_{ext}$

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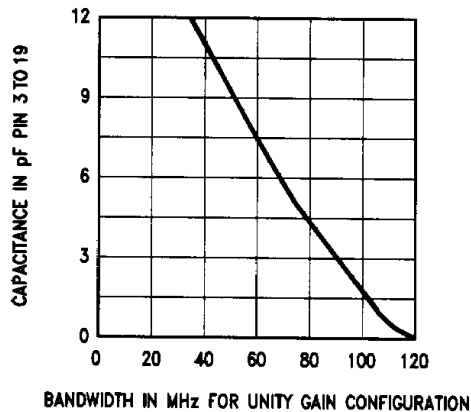


FIGURE 3. Bandwidth vs  $C_{ext}$

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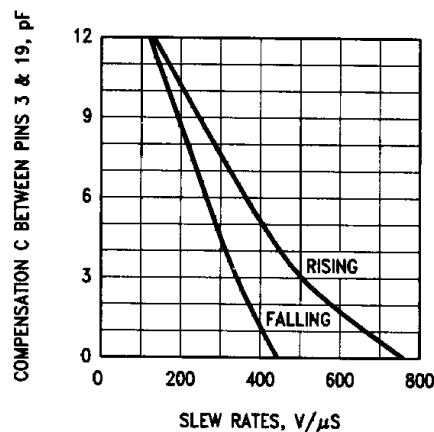


FIGURE 4. Slew Rates vs Compensation C

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## Typical Applications

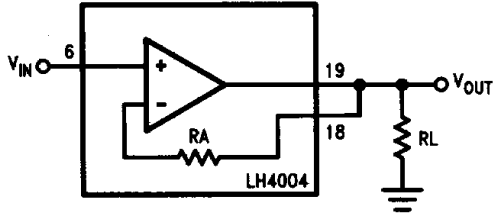
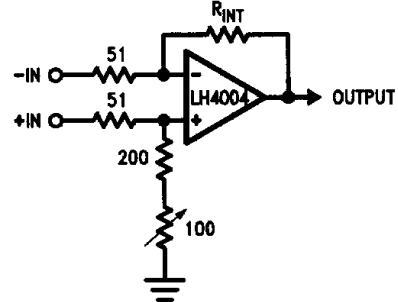


FIGURE 5. Unity Gain Buffer

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Note: Adjust pot for best CMRR.

FIGURE 6. Differential Amplifier

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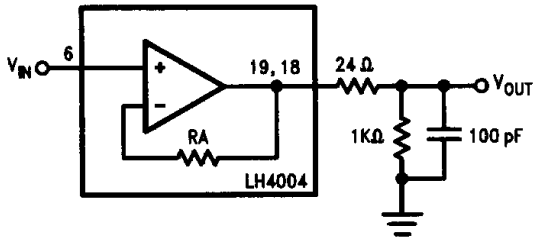


FIGURE 7. Driving Capacitive Loads

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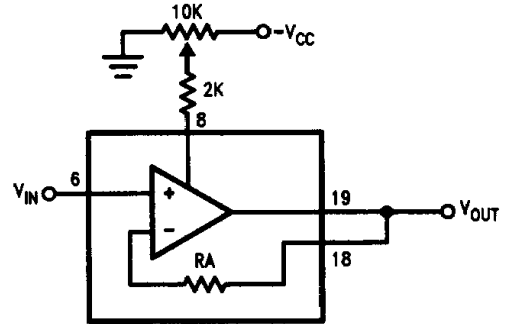


FIGURE 8. Offset Adjust

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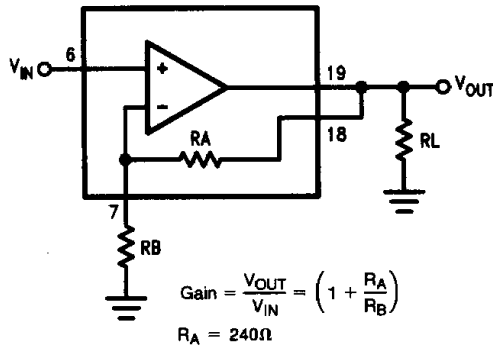
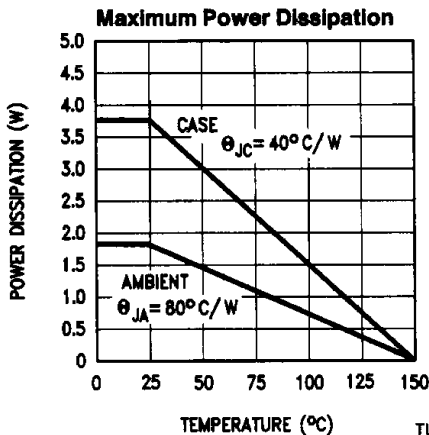


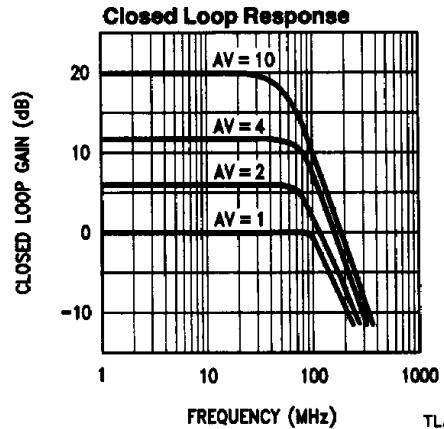
FIGURE 9. LH4004 Used in Amplifier Applications

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## Typical Performance Characteristics

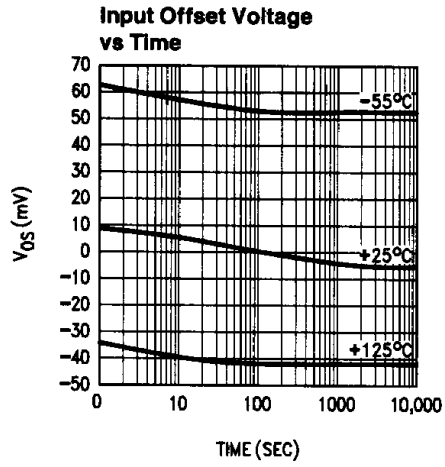


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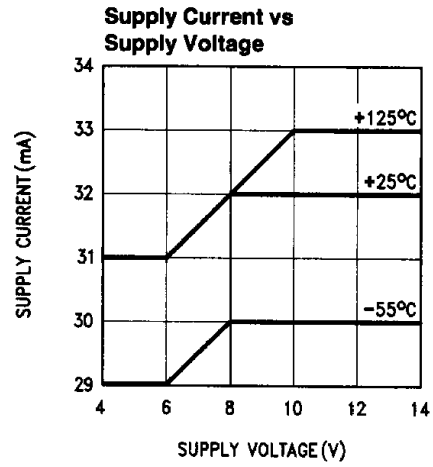


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Typical Performance Characteristics (Continued)

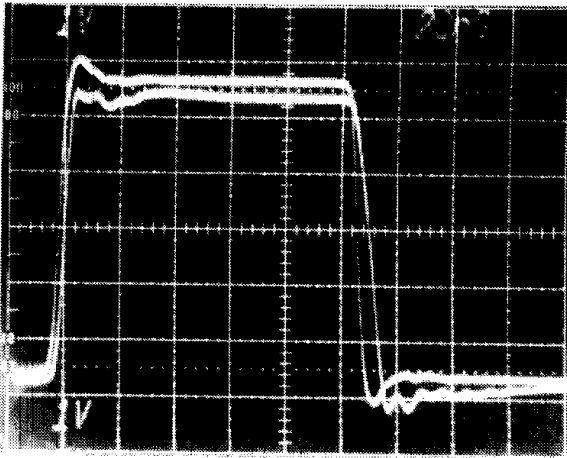


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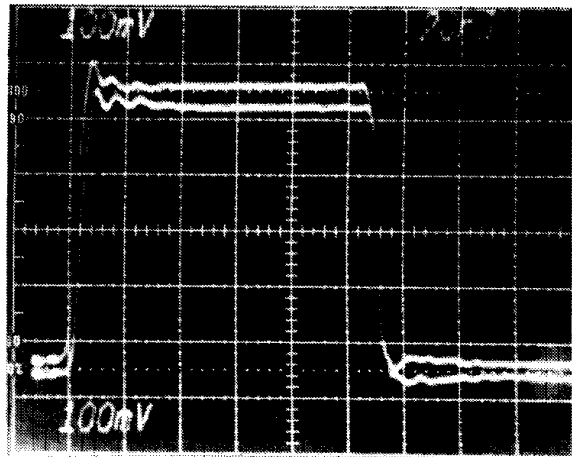
Large Signal Pulse Response



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Top Trace = Input  
Bottom Trace = Output

Small Signal Pulse Response



TL/K/8831-17

Top Trace = Input  
Bottom Trace = Output