LPC2880; LPC2888

16/32-bit ARM microcontrollers; 8 kB cache, up to 1 MB flash, Hi-Speed USB 2.0 device, and SDRAM memory interface

Rev. 01 — 22 June 2006 Preliminary data sheet

1. General description

The LPC2880/LPC2888 are an ARM7-based microcontroller for portable applications requiring low power and high performance. It includes a USB 2.0 Hi-Speed device interface, an external memory interface that can interface to SDRAM and flash, an SD/MMC memory card interface, A/D and D/A converters, and serial interfaces including UART, I^{2}C-bus, and I^{2}S-bus. Architectural enhancements like multi-channel DMA, processor cache, simultaneous operations on multiple internal buses, and flexible clock generation help ensure that the LPC2880/LPC2888 can handle more demanding applications than many competing devices. The chip can be powered from a single battery, from the USB, or from regulated 1.8 V and 3.3 V.

2. Features

2.1 Key features

- ARM7TDMI processor with 8 kB cache, operating at up to 60 MHz
- 1 MB on-chip flash program memory with 128-bit access for high performance
- 64 kB SRAM
- Boot ROM allows execution of flash code, external code, or flash programming via USB
- On-chip DC-to-DC converter can generate all required voltages from a single battery or from USB power
- Multiple internal buses allow simultaneous simple DMA, USB DMA, and program execution from on-chip flash without contention
- External memory controller supports flash, SRAM, ROM, and SDRAM
- Advanced Vectored Interrupt Controller, supporting up to 30 vectored interrupts
- Innovative Event Router allows interrupt, power-up, and clock-start capabilities from up to 107 sources
- Multi-channel GP DMA controller that can be used with most on-chip peripherals as well as for memory-to-memory transfers
- Serial interfaces:
    - Hi-Speed USB 2.0 device (480 Mbit/s or 12 Mbit/s) with on-chip physical layer
    - UART with fractional baud rate generation, flow control, IrDA support, and FIFOs
    - I^{2}C-bus interface
    - I^{2}S-bus (Inter IC Sound bus) interface for independent stereo digital audio input and output
- SD/MMC memory card interface
- 10-bit A/D converter with 5-channel input multiplexing

- 16-bit stereo A/D and D/A converters with amplification and gain control
- Advanced clock generation and power control reduce power consumption
- Two 32-bit timers with selectable prescalers
- 8-bit/4-bit LCD interface bus
- Real Time Clock can be clocked by 32 kHz oscillator or another source
- Watchdog Timer with interrupt and/or reset capabilities.

3. Ordering information

Table 1. Ordering information

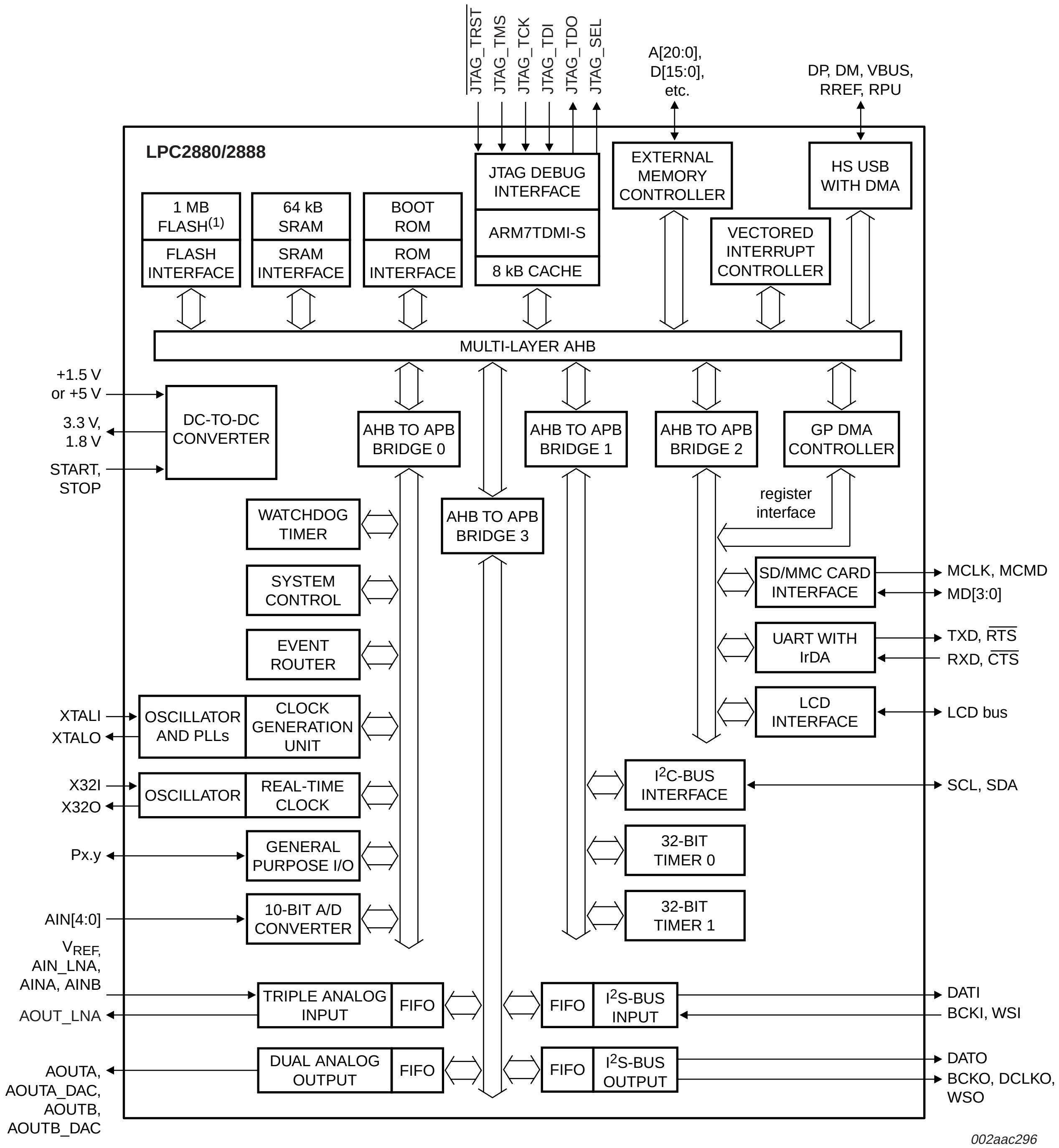
Type number	Package		
	Name	Description	Version
LPC2880FET180	TFBGA180	plastic thin fine-pitch ball grid array package; 180 balls; body 10 × 10 × 0.8 mm	SOT640-1
LPC2888FET180	TFBGA180	plastic thin fine-pitch ball grid array package; 180 balls; body 10 × 10 × 0.8 mm	SOT640-1

3.1 Ordering options

Table 2. Ordering options

Type number	Flash memory	RAM	Temperature range
LPC2880FET180	-	64 kB	–40 °C to +85 °C
LPC2888FET180	1 MB	64 kB	–40 °C to +85 °C

4. Block diagram

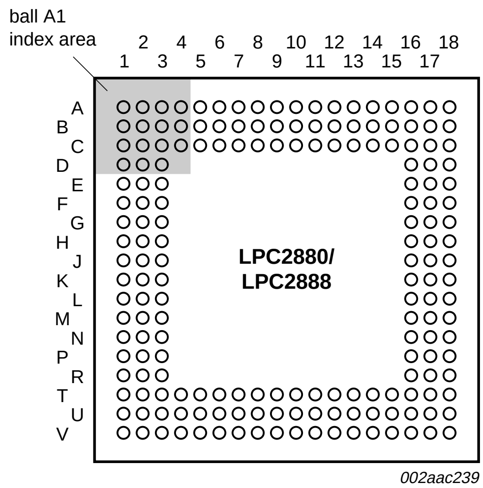


(1) LPC2888 only.

Fig 1. Block diagram

5. Pinning information

5.1 Pinning



Transparent top view

Fig 2. Pin configuration

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	D0/P0[0]	2	D1/P0[1]	3	D3/P0[3]	4	D4/P0[4]
5	D6/P0[6]	6	$V_{SS2(EMC)}$	7	$V_{DD2(EMC)}$	8	$\overline{STCS1}$/P1[5]
9	$\overline{RAS}$/P1[17]	10	MCLKO/P1[14]	11	DQM1/P1[11]	12	$\overline{BLS0}$/P1[12]
13	A18/P1[2]	14	A15/P0[31]	15	$V_{SS1(EMC)}$	16	$V_{DD1(EMC)}$
17	$\overline{OE}$/P1[18]	18	A6/P0[22]		-		-
Row B							
1	$\overline{RPO}$/P1[19]	2	D2/P0[2]	3	LCS/P4[0]	4	D5/P0[5]
5	D7/P0[7]	6	D11/P0[11]	7	D13/P0[13]	8	D15/P0[15]
9	$\overline{DYCS}$/P1[8]	10	CKE/P1[9]	11	$\overline{STCS2}$/P1[5]	12	$\overline{BLS1}$/P1[13]
13	A19/P1[3]	14	A16/P1[0]	15	A13/P0[29]	16	A11/P0[27]
17	A9/P0[25]	18	A7/P0[23]		-		-
Row C							
1	LD1/P4[5]	2	LD0/P4[4]	3	LD2/P4[6]	4	D8/P0[8]
5	D9/P0[9]	6	D10/P0[10]	7	D12/P0[12]	8	D14/P0[14]
9	$\overline{STCS0}$/P1[5]	10	$\overline{CAS}$/P1[16]	11	$\overline{WE}$/P1[15]	12	DQM0/P1[10]
13	A20/P1[4]	14	A17/P1[1]	15	A14/P0[30]	16	A12/P0[28]
17	A10/P0[26]	18	A8/P0[24]		-		-
Row D							
1	LD4/P4[8]	2	LD3/P4[7]	3	LD5/P4[9]	4	-

Table 3. Pin allocation table *...continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
13	-	14	-	15	-	16	A3/P0[19]
17	A4/P0[20]	18	A5/P0[21]		-		-
Row E							
1	$V_{DD1(IO3V3)}$	2	LD6/P4[10]	3	LD7/P4[11]	4	-
13	-	14	-	15	-	16	A0/P0[16]
17	A1/P0[17]	18	A2/P0[18]		-		-
Row F							
1	$V_{SS1(IO)}$	2	LER/P4[3]	3	LRS/P4[1]	4	-
13	-	14	-	15	-	16	DCLKO/P3[3]
17	DATO/P3[6]	18	WSO		-		-
Row G							
1	$V_{SS1(CORE)}$	2	LRW/P4[2]	3	MCLK/P5[0]	4	-
13	-	14	-	15	-	16	DATI/P3[0]
17	WSI/P3[2]	18	BCKO/P3[5]		-		-
Row H							
1	$V_{DD1(CORE1V8)}$	2	MCMD/P5[1]	3	MD0/P5[5]	4	-
13	-	14	-	15	-	16	SCL
17	BCKI/P3[1]	18	$V_{SS4(IO)}$		-		-
Row J							
1	MD2/P5[3]	2	MD1/P5[4]	3	MD3/P5[2]	4	-
13	-	14	-	15	-	16	MODE2/P2[3]
17	SDA	18	$V_{DD4(IO3V3)}$		-		-
Row K							
1	$\overline{\text{RTS}}$/P6[3]	2	$\overline{\text{CTS}}$/P6[2]	3	RXD/P6[0]	4	-
13	-	14	-	15	-	16	P2[0]
17	P2[1]	18	MODE1/P2[2]		-		-
Row L							
1	$V_{DD(DAC3V3)}$	2	VREFP(DAC)	3	TXD/P6[1]	4	-
13	-	14	-	15	-	16	DCDC_GND
17	START	18	STOP		-		-
Row M							
1	VREFN(DAC)	2	AOUTA_DAC	3	AOUTB_DAC	4	-
13	-	14	-	15	-	16	DCDC_$V_{DDI(3V3)}$
17	DCDC_V_{BAT}	18	DCDC_CLEAN		-		-
Row N							
1	AOUTRB	2	AOUTRA	3	AOUTA	4	-
13	-	14	-	15	-	16	DCDC_V_{SS2}
17	DCDC_LX2	18	DCDC_$V_{DDO(1V8)}$		-		-
Row P							
1	$V_{SS2(AMP)}$	2	$V_{SS1(AMP)}$	3	AOUTB	4	-
13	-	14	-	15	-	16	RREF

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
17	DCDC_LX1	18	DCDC_V_{SS1}		-		-
Row R							
1	$V_{DD1(AMP3V3)}$	2	$V_{DD2(AMP3V3)}$	3	AIN_LNA	4	-
13	-	14	-	15	-	16	$V_{SS2(USB)}$
17	$V_{SS1(USB)}$	18	DCDC_$V_{DDO(3V3)}$		-		-
Row T							
1	AINB	2	AOUT_LNA	3	$V_{COM(DADC)}$	4	AINA
5	JTAG_TDI	6	AIN3	7	AIN1	8	X32O
9	$V_{SS(OSC)}$	10	XTALI	11	$V_{SS3(INT)}$	12	$V_{SS1(INT)}$
13	$\overline{\text{JTAG\_TRST}}$	14	$\overline{\text{RESET}}$	15	RPU	16	$V_{SS3(USB)}$
17	DM	18	DCDC_V_{USB}		-		-
Row U							
1	VREF(DADC)	2	VREFP(DADC)	3	$V_{DD(DADC3V3)}$	4	JTAG_SEL
5	AIN4	6	AIN2	7	AIN0	8	$V_{DD(OSC321V8)}$
9	$V_{DD(OSC1V8)}$	10	$V_{SS(ADC)}$	11	$V_{SS2(INT)}$	12	JTAG_TMS
13	JTAG_TDO	14	VBUS/P7[0]	15	$V_{DD1(USB1V8)}$	16	$V_{DD2(USB1V8)}$
17	DP	18	$V_{DD3(USB3V3)}$		-		-
Row V							
1	VREFN(DADC)	2	$V_{SS(DADC)}$	3	$V_{DD(DADC1V8)}$	4	JTAG_TCK
5	$V_{DD2(IO3V3)}$	6	$V_{SS2(IO)}$	7	X32I	8	$V_{SS(OSC32)}$
9	XTALO	10	$V_{DD(ADC3V3)}$	11	$V_{DD2(CORE1V8)}$	12	$V_{SS2(CORE)}$
13	$V_{SS3(IO)}$	14	$V_{DD3(IO3V3)}$	15	$V_{DD1(FLASH1V8)}$	16	$V_{DD2(FLASH1V8)}$
17	$V_{SS3(CORE)}$	18	$V_{DD4(USB3V3)}$		-		-

5.2 Pin description

Table 4. Pin description

Signal name	Ball #	Type[1]	Description
Analog in (dual converter)			
AINA	T4	I	analog input channel A
AINB	T1	I	analog input channel B
AIN_LNA	R3	I	analog input to LNA
AOUT_LNA	T2	O	analog output of LNA; connect to AINA or AINB via external capacitor if used
VCOM(DADC)	T3	RV	ADC common reference voltage and analog output reference voltage combined on-chip
VREF(DADC)	U1	RV	ADC reference voltage
VREFN(DADC)	V1	RV	ADC negative reference voltage
VREFP(DADC)	U2	RV	ADC positive reference voltage
$V_{DD(DADC1V8)}$	V3	P	1.8 V for dual ADC
$V_{DD(DADC3V3)}$	U3	P	3.3 V for dual ADC
$V_{SS(DADC)}$	V2	P	ground for dual ADC

Table 4. Pin description *…continued*

Signal name	Ball #	Type[1]	Description
Analog in (single converter)			
AIN0	U7	I	multiplexed analog input
AIN1	T7	I	multiplexed analog input
AIN2	U6	I	multiplexed analog input
AIN3	T6	I	multiplexed analog input
AIN4	U5	I	multiplexed analog input
$V_{DD(ADC3V3)}$	V10	P	3.3 V analog supply and reference voltage
$V_{SS(ADC)}$	U10	P	ground
Analog out (dual channel)			
AOUTA	N3	O	amplified analog out, channel A
AOUTA_DAC	M2	O	DAC analog out, channel A
AOUTB	P3	O	amplified analog out, channel B
AOUTB_DAC	M3	O	DAC analog out, channel B
AOUTRA	N2	O	amplified analog return, channel A
AOUTRB	N1	O	amplified analog return, channel B
VREFN(DAC)	M1	RV	negative reference voltage
VREFP(DAC)	L2	RV	positive reference voltage
$V_{DD(DAC3V3)}$	L1	P	3.3 V for DAC
$V_{DD1(AMP3V3)}$	R1	P	3.3 V for amplifier
$V_{DD2(AMP3V3)}$	R2	P	3.3 V for amplifier
$V_{SS1(AMP)}$	P2	P	amplifier ground
$V_{SS2(AMP)}$	P1	P	amplifier ground
DAI interface			
BCKI/P3[1]	H17	FI	DAI bit clock; 5 V tolerant GPIO pin
DATI/P3[0]	G16	FI	DAI serial data input; 5 V tolerant GPIO pin
WSI/P3[2]	G17	FI	DAI word select; 5 V tolerant GPIO pin
DAO interface			
BCKO/P3[5]	G18	FO	DAO bit clock; 5 V tolerant GPIO pin
DCLKO/P3[3]	F16	FO	256 × clock output; 5 V tolerant GPIO pin
DATO/P3[6]	F17	FO	DAO serial data output; 5 V tolerant GPIO pin
WSO	F18	O	DAO word select; 5 V tolerant pin
DC-to-DC converters			
START	L17	I	DC-to-DC activation
STOP	L18	I	DC-to-DC deactivation
DCDC_CLEAN	M18	P	reference circuit ground, not connected to substrate
DCDC_GND	L16	P	DC-to-DC main ground and substrate
DCDC_LX1	P17	P	connect to external coil for DC/DC1
DCDC_LX2	N17	P	connect to external coil for DC/DC2
DCDC_V_{BAT}	M17	P	connect to battery +
DCDC_$V_{DDI(3V3)}$	M16	P	DC/DC1 3.3 V input voltage
DCDC_$V_{DDO(1V8)}$	N18	P	DC/DC2 1.8 V output voltage

Table 4. Pin description *...continued*

Signal name	Ball #	Type[1]	Description
DCDC_$V_{DDO(3V3)}$	R18	P	DC/DC1 3.3 V output voltage
DCDC_V_{SS1}	P18	P	ground for DC/DC1, not connected to substrate
DCDC_V_{SS2}	N16	P	ground for DC/DC2, not connected to substrate
DCDC_V_{USB}	T18	P	connect to +5 V pin of USB connector
External memory interface			
D0/P0[0]	A1	FI	external memory data bus, low byte (I/O); GPIO pins
D1/P0[1]	A2		
D2/P0[2]	B2		
D3/P0[3]	A3		
D4/P0[4]	A4		
D5/P0[5]	B4		
D6/P0[6]	A5		
D7/P0[7]	B5		
D8/P0[8]	C4	FI	external memory data bus, high byte (I/O); GPIO pins
D9/P0[9]	C5		
D10/P0[10]	C6		
D11/P0[11]	B6		
D12/P0[12]	C7		
D13/P0[13]	B7		
D14/P0[14]	C8		
D15/P0[15]	B8		
A0/P0[16]	E16	FO	address bus for SDRAM and static memory; GPIO pins
A1/P0[17]	E17		
A2/P0[18]	E18		
A3/P0[19]	D16		
A4/P0[20]	D17		
A5/P0[21]	D18		
A6/P0[22]	A18		
A7/P0[23]	B18		
A8/P0[24]	C18		
A9/P0[25]	B17		
A10/P0[26]	C17		
A11/P0[27]	B16		
A12/P0[28]	C16		
A13/P0[29]	B15		
A14/P0[30]	C15		

Table 4. Pin description *...continued*

Signal name	Ball #	Type[1]	Description
A15/P0[31]	A14	FO	address bus for static memory; GPIO pins
A16/P1[0]	B14		
A17/P1[1]	C14		
A18/P1[2]	A13		
A19/P1[3]	B13		
A20/P1[4]	C13		
$\overline{\text{BLS0}}$/P1[12]	A12	FO	byte lane select for D[7:0], active LOW for static memory; GPIO pin
$\overline{\text{BLS1}}$/P1[13]	B12	FO	byte lane select for D[15:8], active LOW for static memory; GPIO pin
$\overline{\text{CAS}}$/P1[16]	C10	FO	column address strobe, active LOW for SDRAM; GPIO pin
CKE/P1[9]	B10	FO	clock enable; active HIGH for SDRAM; GPIO pin
DQM0/P1[10]	C12	FO	data mask output for D[7:0], active HIGH for SDRAM; GPIO pin
DQM1/P1[11]	A11	FO	data mask output for D[15:8], active HIGH for SDRAM; GPIO pin
$\overline{\text{DYCS}}$/P1[8]	B9	FO	chip select, active LOW for SDRAM; GPIO pin
MCLKO/P1[14]	A10	FO	clock for SDRAM and SyncFlash memory; GPIO pin
$\overline{\text{OE}}$/P1[18]	A17	FO	output enable, active LOW for static memory; GPIO pin
$\overline{\text{RAS}}$/P1[17]	A9	FO	row address strobe, active LOW for SDRAM; GPIO pin
$\overline{\text{RPO}}$/P1[19]	B1	FO	reset power down, active LOW for SyncFlash memory; GPIO pin
$\overline{\text{STCS0}}$/P1[5]	C9	FO	chip select, active LOW for static memory bank 0; GPIO pin
$\overline{\text{STCS1}}$/P1[5]	A8	FO	chip select, active LOW for static memory bank 1; GPIO pin
$\overline{\text{STCS2}}$/P1[5]	B11	FO	chip select, active LOW for static memory bank 2; GPIO pin
$\overline{\text{WE}}$/P1[15]	C11	FO	write enable, active LOW for SDRAM and static memory; GPIO pin
GPIO and mode control			
MODE1/P2[2]	K18	FI	start up MODE PIN1 (pull down); 5 V tolerant GPIO pin
MODE2/P2[3]	J16	FI	start up MODE PIN2 (pull down); 5 V tolerant GPIO pin
P2[0]	K16	FI	5 V tolerant GPIO pin
P2[1]	K17	FI	5 V tolerant GPIO pin
I^{2}C-bus interface			
SCL	H16	I/O	serial clock (input/open-drain output); 5 V tolerant pin
SDA	J17	I/O	serial data (input/open-drain output); 5 V tolerant pin
JTAG interface			
JTAG_SEL	U4	I	JTAG selection (pull-down); 5 V tolerant pin
JTAG_TCK	V4	I	JTAG reset input (pull-down); 5 V tolerant pin
JTAG_TDI	T5	I	JTAG data input (pull-up); 5 V tolerant pin
JTAG_TMS	U12	I	JTAG mode select input (pull-up); 5 V tolerant pin
$\overline{\text{JTAG\_TRST}}$	T13	I	JTAG reset input (pull-down); 5 V tolerant pin
JTAG_TDO	U13	O	JTAG data output; 5 V tolerant pin

Table 4. Pin description *…continued*

Signal name	Ball #	Type[1]	Description
LCD interface			
LCS/P4[0]	B3	FO	chip select to LCD device, programmable polarity; 5 V tolerant GPIO pin
LD0/P4[4]	C2	FO	data bus to/from LCD (I/O) or 5 V tolerant GPIO pins
LD1/P4[5]	C1	FO	
LD2/P4[6]	C3	FO	
LD3/P4[7]	D2	FO	
LD4/P4[8]	D1	FO	
LD5/P4[9]	D3	FO	
LD6/P4[10]	E2	FO	
LD7/P4[11]	E3	FO	
LER/P4[3]	F2	FO	6800 E or 8080 $\overline{RD}$ or 5 V tolerant GPIO pin
LRS/P4[1]	F3	FO	‘high’ data register select, ‘low’ instruction register select, or 5 V tolerant GPIO pin
LRW/P4[2]	G2	FO	6800 W/$\overline{R}$ or 8080 $\overline{WR}$ or 5 V tolerant GPIO pin
Memory card interface			
MCMD/P5[1]	H2	FI	command (I/O); 5 V tolerant GPIO pin
MD0/P5[5]	H3	FI	data bus from/to MCI/SD card (I/O); 5 V tolerant GPIO pin
MD1/P5[4]	J2	FI	data bus from/to MCI/SD card (I/O); 5 V tolerant GPIO pin
MD2/P5[3]	J1	FI	data bus from/to MCI/SD card (I/O); 5 V tolerant GPIO pin
MD3/P5[2]	J3	FI	data bus from/to MCI/SD card (I/O); 5 V tolerant GPIO pin
MCLK/P5[0]	G3	FO	MCI clock output; 5 V tolerant GPIO pin
Oscillator (32.768 kHz)			
X32I	V7	I	32.768 kHz oscillator input
X32O	T8	O	32.768 kHz oscillator output
$V_{DD(OSC321V8)}$	U8	P	1.8 V
$V_{SS(OSC32)}$	V8	P	ground
Oscillator (main)			
XTALI	T10	I	main oscillator input
XTALO	V9	O	main oscillator output
$V_{DD(OSC1V8)}$	U9	P	1.8 V
$V_{SS(OSC)}$	T9	P	ground
Reset			
$\overline{RESET}$	T14	I	master reset, active LOW; 5 V tolerant pin
UART			
$\overline{CTS}$/P6[2]	K2	FI	clear to send or transmit flow control, active LOW; 5 V tolerant GPIO pin
RXD/P6[0]	K3	FI	serial input; 5 V tolerant GPIO pin
$\overline{RTS}$/P6[3]	K1	FO	request to send or receive flow control, active LOW; 5 V tolerant GPIO pin
TXD/P6[1]	L3	FO	serial output; 5 V tolerant GPIO pin

Table 4. Pin description *…continued*

Signal name	Ball #	Type[1]	Description
USB interface			
DM	T17	I/O	negative USB data line
DP	U17	I/O	positive USB data line
VBUS/P7[0]	U14	FI	USB supply detection; 5 V tolerant GPIO pin
RPU	T15	P	external 1.5 kΩ resistor to analog ground
RREF	P16	P	external 12 kΩ resistor to analog supply voltage (3.3 V)
$V_{DD1(USB1V8)}$	U15	P	analog 1.8 V
$V_{DD2(USB1V8)}$	U16	P	analog 1.8 V
$V_{DD3(USB3V3)}$	U18	P	analog 3.3 V
$V_{DD4(USB3V3)}$	V18	P	analog 3.3 V
$V_{SS1(USB)}$	R17	P	analog ground
$V_{SS2(USB)}$	R16	P	analog ground
$V_{SS3(USB)}$	T16	P	analog ground
Digital power and ground			
$V_{DD1(CORE1V8)}$	H1	P	1.8 V for internal RAM and ROM
$V_{DD1(FLASH1V8)}$	V15	P	1.8 V for internal flash memory
$V_{DD1(EMC)}$	A16	P	1.8 V or 3.3 V for external memory controller
$V_{DD1(IO3V3)}$	E1	P	3.3 V for peripherals
$V_{DD2(CORE1V8)}$	V11	P	1.8 V for core
$V_{DD2(EMC)}$	A7	P	1.8 V or 3.3 V for external memory controller
$V_{DD2(FLASH1V8)}$	V16	P	1.8 V for internal flash memory
$V_{DD2(IO3V3)}$	V5	P	3.3 V for peripherals
$V_{DD3(IO3V3)}$	V14	P	3.3 V for peripherals
$V_{DD4(IO3V3)}$	J18	P	3.3 V for peripherals
$V_{SS1(CORE)}$	G1	P	ground for internal RAM and ROM
$V_{SS1(EMC)}$	A15	P	ground for external memory controller
$V_{SS1(INT)}$	T12	P	ground for other internal blocks
$V_{SS1(IO)}$	F1	P	ground for peripherals
$V_{SS2(CORE)}$	V12	P	ground for core
$V_{SS2(EMC)}$	A6	P	ground for external memory controller
$V_{SS2(INT)}$	U11	P	ground for other internal blocks
$V_{SS2(IO)}$	V6	P	ground for peripherals
$V_{SS3(CORE)}$	V17	P	ground for core, substrate, flash
$V_{SS3(INT)}$	T11	P	ground for other internal blocks
$V_{SS3(IO)}$	V13	P	ground for peripherals
$V_{SS4(IO)}$	H18	P	ground for peripherals

[1] I = input; O = output; I/O = input/output; RV = reference voltage; FI = functional input; FO = functional output; P = power or ground

6. Functional description

6.1 Architectural overview

The LPC2880/LPC2888 includes an ARM7TDMI CPU with an 8 kB cache, an AMBA AHB interfacing to high-speed on-chip peripherals and internal and external memory, and four AMBA APBs for connection to other on-chip peripheral functions.

The LPC2880/LPC2888 includes a multi-layer AHB and four separate APBs, in order to minimize interference between the USB controller, other DMA operations, and processor activity. Bus masters include the ARM7 itself, the USB block, and the general purpose DMA controller.

Lower speed peripheral functions are connected to the APB buses. The four AHB-to-APB bridges interface the APB buses to the AHB bus.

6.1.1 ARM7TDMI processor

The ARM7TDMI is a general purpose 32-bit microprocessor that offers high performance and very low power consumption. The ARM architecture is based on RISC principles, and the instruction set and related decode mechanism are much simpler than those of microprogrammed CISCs. This simplicity results in a high instruction throughput and impressive real-time interrupt response from a small and cost-effective processor core.

Pipeline techniques are employed so that all parts of the processing and memory systems can operate continuously. Typically, while one instruction is being executed, its successor is being decoded, and a third instruction is being fetched from memory.

The ARM7TDMI processor also employs a unique architectural strategy known as Thumb, which makes it ideally suited to high-volume applications with memory restrictions, or applications where code density is an issue.

The key idea behind Thumb is that of a super-reduced instruction set. Essentially, the ARM7TDMI processor has two instruction sets:

- The standard 32-bit ARM instruction set.
- A 16-bit Thumb instruction set.

The Thumb set's 16-bit instruction length allows it to approach twice the density of standard ARM code while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. This is possible because Thumb code operates on the same 32-bit register set as ARM code.

Thumb code is able to provide down to 65 % of the code size of ARM, and 160 % of the performance of an equivalent ARM processor connected to a 16-bit memory system.

The ARM7TDMI processor is described in detail on the ARM web site.

6.1.2 On-chip flash memory system

The LPC2880/LPC2888 includes a 1 MB flash memory system. This memory may be used for both code and data storage. Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the USB port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage field firmware upgrades, etc.

The flash is 128 bit wide and includes buffering to allow 3 out of 4 sequential read operations to operate without wait states.

6.1.3 On-chip static RAM

The LPC2880/LPC2888 includes 64 kB of static RAM that may be used for code and/or data storage.

6.1.4 On-chip ROM

The LPC2880/LPC2888 includes an on-chip ROM that contains boot code. Execution begins in on-chip ROM after a Reset.

The boot code in this ROM reads the state of the mode inputs and accordingly does one of the following:

1. Starts execution in internal flash
2. Starts execution in external memory
3. Performs a hardware self-test, or
4. Downloads code from the USB interface into on-chip RAM and transfers control to the downloaded code

6.2 Memory map

The LPC2880/LPC2888 memory map incorporates several distinct regions, as shown in Figure 3. When an application is running, the CPU interrupt vectors are remapped to allow them to reside in on-chip SRAM.

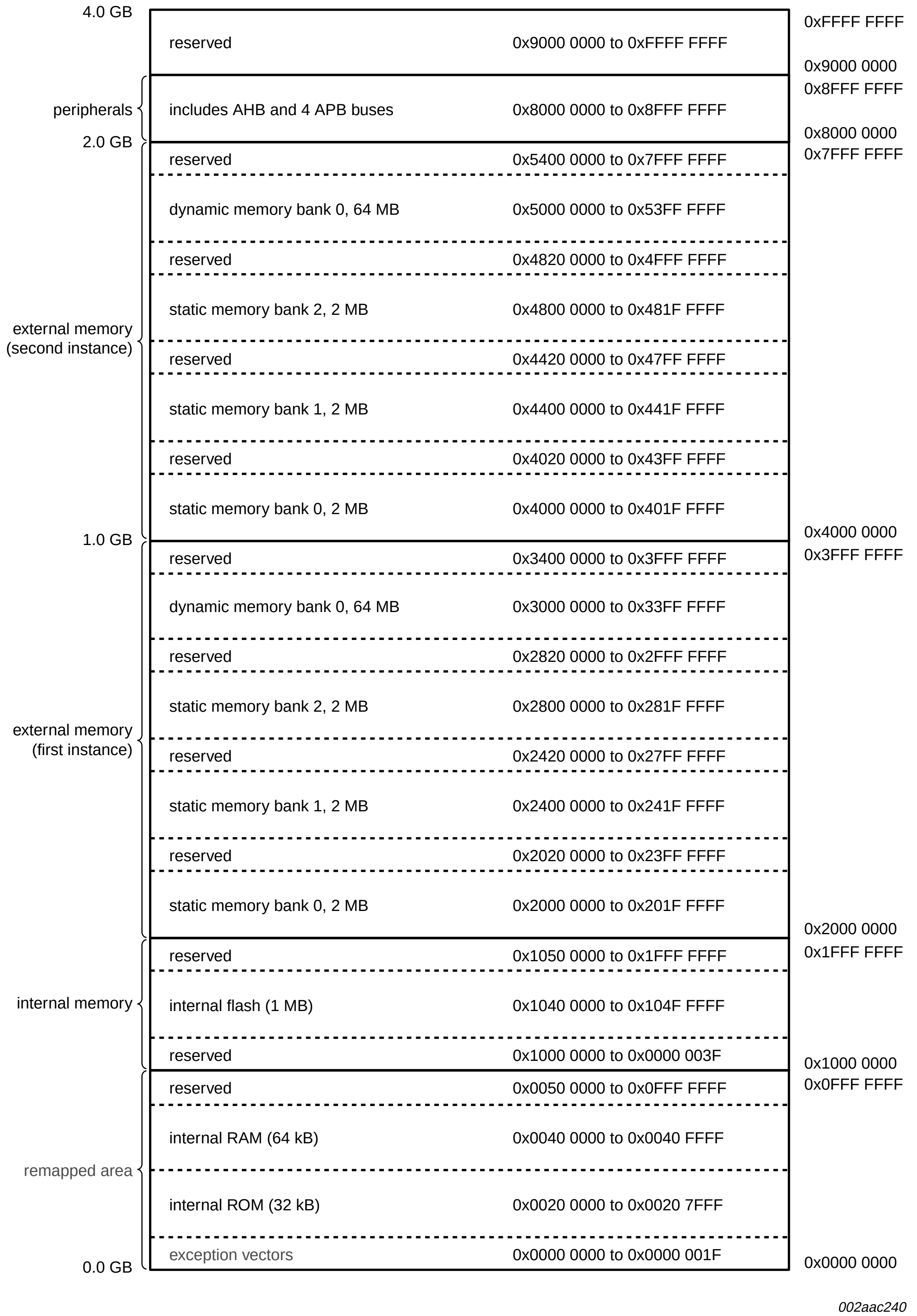


Fig 3. Memory map

6.3 Cache

The CPU of the LPC2880/LPC2888 has been extended with a 2-way set-associative cache controller. The cache is 8 kB in size and can store both data and instruction code.

If code that is being executed is present in the cache from a previous execution, the CPU will not experience code fetch waits. Similarly, if requested data is present in the cache, the CPU will not experience a data access wait.

The trade-off of introducing this cache is that each AHB access that bypasses the cache will have an extra wait state inserted. Therefore it is advisable to enable instruction caching (and preferably data caching as well) for all memories, to provide the highest performance.

6.3.1 Cache operation

This cache works as follows, for each page of which the cache is enabled:

- If a read is requested and the information is not in the cache (a cache miss), a line of eight 32-bit words will be read from the AHB bus. The CPU waits until this process is complete.
- If a read is requested and the information is found in the cache (a cache hit), the information is read from cache, with zero wait states.
- If data is written, and the location is not in the cache (a cache miss), the data will be written directly to memory.
- If data is written, and the location is in the cache, because this location has been read before (a cache hit), then data is written into the cache with zero wait states and the cache line is marked as ‘dirty’.
- If a ‘dirty’ cache line is about to be discarded because of a cache miss on a read request, this line will first be written back to memory (a cache-line flush).

The cache can be set to data-only, instruction-only or combined (unified) caching. The cache has 16 configurable pages, each 2 MB in range. The pages occupy the bottom 32 MB of the memory map. The virtual address and enable/disable status is configurable for each page.

6.3.2 Features

- 8 kB, 2-way set-associative cache.
- May be used as both an instruction and data cache.
- Zero wait states for a cache hit.
- 16 configurable pages, each 2 MB in range.

6.4 Flash memory and programming

The LPC2888 incorporates 1 MB flash memory system, while the LPC2880 is a flash-less device. The flash memory of the LPC2888 may be used for both code and data storage.

Programming of the flash memory may be accomplished in several ways. It may be programmed In System via the USB port. The application program may also erase and/or program the flash while the application is running, allowing a great degree of flexibility for data storage, field firmware upgrades, etc.

Programming the flash in a running application is accomplished via a register interface on the APB bus. The flash module can generate an interrupt request when burning or erasing is completed.

The flash memory contains a buffer to allow for faster execution. Information is read from the flash 128 bits at a time. The buffer holds this entire amount, which can represent four 32-bit ARM instructions. These captured instructions can them be executed without flash read delays, improving system performance.

6.4.1 Features

- Flash access for processor execution and data read is via the AHB bus.
- Flash programming in a running application is via an APB register interface.
- Initial programming or reprogramming is can be accomplished from the USB port.

6.5 External memory controller

The LPC2880/LPC2888 External Memory Controller (EMC) is a multi-port memory controller that supports asynchronous static memory devices such as RAM, ROM and flash, as well as dynamic memories such as Single Data Rate SDRAM. It complies with ARM's AMBA.

6.5.1 Features

- Dynamic memory interface support including Single Data Rate SDRAM.
- Asynchronous static memory device support including RAM, ROM, and flash, with or without asynchronous page mode.
- Low transaction latency.
- Read and write buffers to reduce latency and to improve performance.
- 8-bit and 16-bit static memory support.
- 16-bit SDRAM memory support.
- Static memory features include:
  - Asynchronous page mode read.
  - Programmable wait states.
  - Bus turnaround delay.
  - Output enable, and write enable delays.
  - Extended wait.
  - 2 MB address range with three chip selects.
- One chip select for synchronous memory and three chip selects for static memory devices.
- Power-saving modes dynamically control CKE and CLKOUT to SDRAMs.
- Dynamic memory self-refresh mode controlled by software.
- Controller supports 2 k, 4 k, and 8 k row address synchronous memory parts. That is typically 512 MB, 256 MB, and 128 MB parts, with 4, 8, or 16 data lines per device.

Note: Synchronous static memory devices (synchronous burst mode) are not supported.

6.6 GPIO

Many device pins that are not connected to a specific peripheral function can be used as are GPIOs. These pins can be controlled by the MODE registers. Pins may be dynamically configured as inputs or outputs. Separate registers allow setting or clearing any number of outputs simultaneously. The current state of the port pins may be read back via the PIN registers.

6.6.1 Features

- 81 pins have dual use as a specific function I/O or as a GPIO.
- Each dual use pin can be programmed for functional I/O, drive high, drive low, or hi-Z/input.
- Four pins are dedicated as GPIO, programmable for drive high, drive low, or hi-Z/input.

6.7 Interrupt controller

The interrupt controller accepts all of the interrupt request inputs and categorizes them as FIQ or IRQ. The programmable assignment scheme means that priorities of interrupts from the various peripherals can be dynamically assigned and adjusted.

FIQ has the highest priority. If more than one request is assigned to FIQ, the interrupt controller combines the requests to produce the FIQ signal to the ARM processor.

The interrupt controller combines the requests from all the vectored IRQs to produce the IRQ signal to the ARM processor. The IRQ service routine can start by reading a register from the interrupt controller and jumping there.

6.7.1 Features

- Maps all LPC2880/LPC2888 interrupt sources to processor FIQ and IRQ
- Level sensitive sources
- Programmable priority among sources
- Nested interrupt capability
- Software interrupt capability for each source

6.8 Event router

105 external and internal LPC2880/LPC2888 signals are connected to the Event Router block. Most of them are device pins, plus a selection of internal signals from other LPC2880/LPC2888 modules. GPIO input pins, functional input pins, and even functional outputs can be monitored by the Event Router.

Each signal can act as an interrupt source, or a clock enable or reset source for LPC2880/LPC2888 modules, with individual options for high- or low-level sensitivity or rising- or falling-edge sensitivity. The outputs of the polarity and sensitivity logic can be read from Raw Status Registers 0 to 3.

Each active state is next masked/enabled by a “global” mask bit for that signal. The results can be read from Pending Registers 0 to 3.

All 105 Pending signals are presented to each of the five output logic blocks. Each output logic block includes a set of four Interrupt Output Mask Registers, each set totalling 105 bits, that control whether each signal applies to that output. These are logically ANDed with the corresponding Pending signals, and the 105 results in each logic block are logically ORed to make the output of the block. The 525 results can be read in the Interrupt Output Pending Registers.

Outputs 0 to 3 are routed to the Interrupt Controller, in which each can be individually enabled to cause an interrupt. Output 4 is routed to the Clock Generation Unit, in which it can serve as a wake-up generator. The five outputs can be read in the Output Register.

6.9 General purpose timers

The LPC2880/LPC2888 contains two fully independent general purpose timers. Each timer is a 32-bit wide down counter with selectable prescaler. The prescaler allows either the system clock to be used directly, or the clock to be divided by 16 or 256.

Two modes of operation are available, free-running and periodic timer. In periodic timer mode, the counter will generate an interrupt at a constant interval. In free-running mode the timer will overflow after reaching its zero value and continue to count down from the maximum value.

6.9.1 Features

- Two independent 32-bit timers.
- Free-running or periodic operating modes.
- Generate timed interrupts.

6.10 Watchdog timer

The purpose of the Watchdog Timer is to interrupt and/or reset the microcontroller within a reasonable amount of time if it enters an erroneous state. When enabled, the Watchdog will generate an interrupt or a system reset if the user program fails to reset the Watchdog within a predetermined amount of time. Alternatively, it can be used as an additional general purpose Timer.

The WDT clock increments a 32-bit Prescale Counter, the value of which is continually compared to the value of the Prescale Register. When the Prescale Counter matches the Prescale Register at a WDT clock edge, the Prescale Counter is cleared and the 32-bit Timer Counter is incremented. Thus the Prescale facility divides the WDT clock by the value in the Prescale Register plus one.

The value of the Timer Counter is continually compared to the values in two registers called Match Register 0 and 1. When/if the value of the Timer Counter matches that of Match Register 0 at a WDT clock edge, a signal ‘m0’ can be asserted to the Event Router, which can be programmed to send an interrupt signal to the Interrupt Controller as a result. When/if the value of the Timer Counter matches that of Match Register 1 at a WDT clock edge, a signal ‘m1’ can be asserted to the CGU, which resets the chip as a result. The CGU also includes a flag to indicate whether a reset is due to a Watchdog time-out.

6.10.1 Features

- Optionally resets chip (via Clock Generation Unit) if not periodically reloaded.

- Optional interrupt via Event Router.
- 32-bit Prescaler and 32-bit Counter allow extended watchdog period.

6.11 Real-time clock

The Real Time Clock (RTC) is a set of counters for measuring time when system power is on, and optionally when it is off. It uses little power in either mode.

6.11.1 Features

- Measures the passage of time to maintain a calendar and clock.
- Ultra Low Power design to support battery powered systems.
- Provides Seconds, Minutes, Hours, Day of Month, Month, Year, Day of Week, and Day of Year.
- Dedicated 32 kHz oscillator.
- Dedicated power supply pin can be connected to a battery or to the main 1.8 V.

6.12 General purpose DMA controller

The General Purpose DMA Controller (GPDMA) is an AMBA AHB compliant master allowing selected LPC2880/LPC2888 peripherals to have DMA support. Peripherals that can be serviced by the GPDMA channels include the MCI/SD card interface, UART TX and/or RX, the I^2C-bus interface, the Simple Analog Out (SAO) front-ends to the I2S/DAO and 16-bit dual DACs, the Simple Analog In (SAI) interfaces for data from the I2S/DAI and 16-bit dual ADCs, and the output to the LCD interface.

6.12.1 Features

- Eight DMA channels. Each channel can support a unidirectional transfer, or a pair of channels can be used together to follow a linked list of buffer addresses and transfer counts.

  The GPDMA provides 16 peripheral DMA request lines. Most of these are connected to the peripherals listed above; two can be used for external requests.
- The GPDMA supports a subset of the flow control signals supported by ARM DMA channels, specifically ‘single’ but not ‘burst’ operation.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers.
- Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.
- Rotating channel priority. Each DMA channel has equal opportunity to perform transfers.
- The GPDMA is one of three AHB masters in the LPC2880/LPC2888, the others being the ARM7 processor and the USB interface.
- Incrementing or non-incrementing addressing for source and destination.
- Supports 8-bit, 16-bit, and 32-bit wide transactions.
- GPDMA channels can be programmed to swap data between big- and little-endian formats during a transfer.

- An interrupt to the processor can be generated on DMA completion, when a DMA channel is halfway to completion, or when a DMA error has occurred.

6.13 UART and IrDA

The LPC2880/LPC2888 contains one UART with baud rate generator and IrDA support.

6.13.1 Features

- 32-B Receive and Transmit FIFOs.
- Register locations conform to the 16C650 industry standard.
- Receiver FIFO trigger points at 1 B, 16 B, 24 B, and 28 B.
- Built-in baud rate generator.
- CGU generates UART clock including fractional divider capability.
- Auto baud capability.
- Optional hardware flow control.
- IrDA mode for infrared communication.

6.14 I^2C-bus interface

The LPC2880/LPC2888 I^2C-bus interface is byte oriented and has four operating modes: master Transmit mode, master Receive mode, slave Transmit mode and slave Receive mode. The interface complies with the entire I^2C-bus specification, and allows turning power off to the LPC2880/LPC2888 without causing a problem with other devices on the same I^2C-bus.

6.14.1 Features

- Standard I^2C-bus interface, configurable as Master, Slave, or Master/Slave.
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus.
- Programmable clock allows adjustment of I^2C-bus transfer rates.
- Bidirectional data transfer between masters and slaves.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.
- Supports normal (100 kHz) and fast (400 kHz) operation.

6.15 10-bit A/D converter

The LPC2880/LPC2888 contains a single 10-bit successive approximation analog to digital converter with five multiplexed channels.

6.15.1 Features

- 10-bit successive approximation analog to digital converter.
- Input multiplexing among 5 pins.

- Power-down mode.
- Measurement range 0 V to 3.3 V.
- 10-bit conversion time ≥ 2.44 μs.
- Single or continuous conversion mode.

6.16 Analog I/O

The analog I/O system includes an I^2S input channel, an I^2S output channel, a dual A/D converter, and a dual D/A converter. Each channel includes a separate 4 sample FIFO.

Each of the two ADC inputs includes a Programmable Gain Amplifier (PGA). A separate input, which can be routed to either ADC, also include an additional Low Noise Amplifier (LNA).

Each DAC has associated pins for unbuffered and amplified outputs.

6.16.1 Features

- I^2S-bus input channel with a 4 sample FIFO for stereo Digital Analog Input (DAI).
- I^2S-bus output channel with a 4 sample FIFO for stereo Digital Analog Output (DAO).
- Dual 16-bit A/D converters with individual inputs routed through programmable gain amplifiers. Each ADC can alternatively take its input from a single pin that includes an additional low noise amplifier. Input takes place through a 4 sample FIFO.
- Dual 16-bit D/A converters. Each DAC includes both a direct output and an amplified output. Output takes place through a 4 sample FIFO.

6.17 USB 2.0 high-speed device controller

The USB is a 4 wire bus that supports communication between a host and a number (127 max.) of peripherals. The host controller allocates the USB bandwidth to attached devices through a token based protocol. The bus supports hot plugging, un-plugging and dynamic configuration of the devices. All transactions are initiated by the host controller.

The host schedules transactions in 1 ms frames. Each frame contains an SoF marker and transactions that transfer data to/from device endpoints. Each device can have a maximum of 16 logical or 32 physical endpoints. There are 4 types of transfers defined for the endpoints. Control transfers are used to configure the device. Interrupt transfers are used for periodic data transfer. Bulk transfers are used when rate of transfer is not critical. Isochronous transfers have guaranteed delivery time but no error correction.

The LPC2880/LPC2888 USB controller enables 480 Mbit/s or 12 Mbit/s data exchange with a USB host controller. It includes a USB controller, a DMA engine, and a USB 2.0 ATX physical interface.

The USB controller consists of the protocol engine and buffer management blocks. It includes an SRAM that is accessible to the DMA engine and to the processor via the register interface.

The DMA engine is an AHB master, having direct access to all ARM memory space but particularly to on-chip RAM. Each USB endpoint that requires its data to be transferred via DMA is allocated to a logical DMA channel in the DMA engine.

Endpoints with small packet sizes can be handled by software via registers in the USB controller. In particular, Control Endpoint 0 is always handled in this way.

6.17.1 Features

- Fully compliant with USB 2.0 specification (HS and FS).
- 16 physical endpoints.
- Supports Control, Bulk, Interrupt and Isochronous endpoints.
- Endpoint type selection by software
- Endpoint maximum packet size setting by software
- Supports Soft Connect feature (requires an external 1.5 kΩ resistor connected to the USB_RPU pad).
- Supports bus-powered capability with low suspend current.
- Four Read/Write DMA channels.
- Supports Burst data transfers on the AHB.
- Supports Retry and Split transactions on the AHB.

6.18 SD/MMC card interface

The Secure Digital and Multimedia Card Interface (MCI) is an interface between the Advanced Peripheral Bus (APB) system bus and multimedia and/or secure digital memory cards.

The interface provides all functions specific to the Secure Digital/MultiMedia memory card, such as the clock generation unit, power management control, command, data transfer, interrupt generation, and DMA request generation.

6.18.1 Features

- Conformance to Multimedia Card Specification v2.11.
- Conformance to Secure Digital Memory Card Physical Layer Specification, v0.96.
- Use as a multimedia card bus or a secure digital memory card bus host. It can be connected to several multimedia cards, or a single secure digital memory card.
- DMA transfers are supported through the Simple DMA facility.

6.19 LCD interface

The LCD interface contains logic to interface to a 6800 or 8080 bus compatible LCD controller. The LCD interface is compatible with the 6800 bus standard and the 8080 bus standard, with one address pin (RS) for selecting the data or instruction register.

The LCD interface makes use of a configurable clock (programmed in the CGU) to adjust the speed of the 6800/8080 bus to the speed of the connected peripheral.

6.19.1 Features

- 8-bit or 4-bit parallel interface mode: 6800-series, 8080-series.
- Supports multiple frequencies for the bus, to support high and low speed LCD controllers.

- Supports polling the busy flag from the LCD controller to avoid CPU polling.
- Contains a 16 B FIFO for sending control and data information to the LCD controller.
- Contains a serial interface which uses the same FIFO for serial transmissions.
- Supports FIFO level flow control to the General Purpose DMA controller.

6.20 Clocking and power control

Clocking in the LPC2880/LPC2888 is controlled by a versatile Clock Generation Unit (CGU), so that system and peripheral requirements may be met, while allowing optimization of power consumption. Clocks to most functions may be turned off if not needed, and may be enabled and disabled by selected events through the Event Router.

Clock sources include a high frequency (1 MHz to 20 MHz) crystal oscillator and a 32 kHz RTC oscillator. Higher frequency clocks may be generated through the use of two programmable PLLs.

Reset of individual functional blocks is also controlled by the CGU. Full chip reset can be initiated by the external reset pin or by the watchdog timer.

6.20.1 Features

- Power and performance control provided by versatile clock generation to individual functional blocks.
- Multiple clock sources including external crystal and programmable PLLs.
- Watchdog timer to monitor software integrity.
- Individual control of software reset to many functional blocks.
- Lower speed peripherals are connected to an APB bus for lower power consumption.

6.20.2 Reset

The LPC2880/LPC2888 has two sources of reset: the RESET_N pin and the watchdog reset. The RESET pin includes an on-chip pull-up. The RESET_N pin must remain asserted at power-up for 1 ms after power supply voltages are stable. This includes on-chip DC-to-DC converter voltages.

When a chip reset is removed, the processor begins executing at address 0, which is the Reset vector. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

The on-chip watchdog timer can cause a chip reset if not updated within a user programmable amount of time. A status register allows software to determine if a chip reset was caused by the watchdog timer. The watchdog timer can also be configured to generate an interrupt if desired.

Software reset of many individual functional blocks may be performed via registers within the CGU.

6.20.3 Crystal oscillator

The main oscillator is the basis for the clocks most chip functions use by default. The oscillator may be used with crystal frequencies from 1 MHz to 20 MHz.

6.20.4 PLLs

The LPC2880/LPC2888 includes two PLLs: a low power PLL that may be used to provide clocks to most chip functions; a high-speed PLL that may be used to generate faster clocks for selected chip functions, if needed. Each PLL can be driven from several clock sources. These include the main oscillator (1 MHz to 20 MHz), the RTC oscillator (32 kHz), the bit clock or word select inputs of the I^2S input channel, the clock input from the SD/MMC Card interface, or the output clock from the other PLL.

The low power PLL takes the input clock and multiplies it up to a higher frequency (by 1 to 32), then divides it down (by 1, 2, 4, or 8) to provide the output clock used by the CGU. The output frequency of this PLL can range from 9.75 MHz to 160 MHz. Functional blocks may have limitations below this upper limit.

The high-speed PLL takes the input clock, optionally divides it down (by 1 to 256), then multiplies it up to a higher frequency (by 1 to 1024), then divides it down (by 1 to 16) to provide the output clock used by the CGU. The output frequency of this PLL can range from 17 MHz to 550 MHz. Functional blocks may have limitations below this upper limit.

6.20.5 Power control and modes

Power control on the LPC2880/LPC2888 is accomplished by detailed control over the clocking of each functional block via the CGU. The LPC2880/LPC2888 includes a very versatile clocking scheme that provides a great deal of control over performance and power usage.

On-chip functions are divided into 11 groups. Each group has a selection for one of several basic clock sources. Graceful (glitch-free) switching between these clock sources is provided.

Three of these functional groups include a fractional divider that allows any rate below the selected clock to be derived. Three other functional groups include more than one fractional divider (up to six), allowing several different clock rates to be generated within the group. Each function within the group can then be assigned to use any one of the generated clocks.

Each function within any group can also be individually turned off by disabling the clock to that function. When added to the versatile clock rate selection, this allows very detailed control of power utilization.

Each function also can be configured to have clocks automatically turned on and off based on a signal from the Event Router.

6.20.6 APB bus

Many peripheral functions are accessed by on-chip APB buses that are attached to the higher speed AHB bus. The APB bus performs reads and writes to peripheral registers in three peripheral clocks.

6.21 Emulation and debugging

The LPC2880/LPC2888 supports emulation via a dedicated JTAG serial port. The dedicated JTAG port allows debugging of all chip features without impact to any pins that may be used in the application.

Standard ARM EmbeddedICE logic provides on-chip debug support. The debugging of the target system requires a host computer running the debugger software and an EmbeddedICE protocol converter. The EmbeddedICE protocol converter converts the Remote Debug Protocol commands to the JTAG data needed to access the ARM core.

7. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		–0.5	+1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		–0.5	+3.6	V
$V_{DD(EMC)}$	external memory controller supply voltage	in 1.8 V range	–0.5	+1.95	V
		in 3.3 V range	–0.5	+3.6	V
V_{IA}	analog input voltage		–0.5	$V_{VDD(ADC3V3)}$	V
V_I	input voltage	[2][3][4]	–0.5	+5.0	V
		[2][3][5]	–0.5	+3.6	V
I_{DD}	supply current	[6]	<tbd>	<tbd>	mA
I_{SS}	ground current	[7]	<tbd>	<tbd>	mA
T_{stg}	storage temperature		–40	+125	°C
$P_{tot(pack)}$	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	<tbd>	W
V_{esd}	electrostatic discharge voltage	human body model [8]			
		all pins	–2000	+2000	V
		machine model [9]			
		all pins	–200	+200	V

[1] The following applies to Table 5:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] All inputs are 5 V tolerant except external memory bus and USB pins.

[3] Including voltage on outputs in 3-state mode.

[4] 5 V tolerant pins

[5] Other I/O pins.

[6] Per supply pin.

[7] Per ground pin.

[8] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[9] Machine model: equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω series resistor.

8. Static characteristics

Table 6. Static characteristics

T_a = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V8)}$	supply voltage (1.8 V)		[2]	1.7	1.8	1.95	V
$V_{DD(3V3)}$	supply voltage (3.3 V)		[3]	3	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		[4]	3	3.3	3.6	V
$V_{DD(EMC)}$	external memory controller supply voltage	in 1.8 V range	[5]	1.7	1.8	1.95	V
		in 3.3 V range	[5]	2.7	3.3	3.6	V
V_{DCDC_VBAT}	voltage on pin DCDC_V_{BAT}			0.9	1.2	1.6	V
I_{IL}	LOW-state input current	V_I = 0 V; no pull-up		-	-	3	µA
I_{IH}	HIGH-state input current	V_I = V_{DD}; no pull-down	[6]	-	-	3	µA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = V_{DD}; no pull-up/down	[6]	-	-	3	µA
I_{latch}	I/O latch-up current	−(1.5V_{DD}) < V_I < (1.5V_{DD})	[6]	-	-	100	mA
V_I	input voltage		[6][7][8]	0	-	V_{DD}	V
V_{IH}	HIGH-state input voltage		[9]	1.6	-	-	V
			[10]	2.0	-	-	V
V_{IL}	LOW-state input voltage		[9]	-	-	0.6	V
			[10]	-	-	0.8	V
V_{OH}	HIGH-state output voltage	I_{OH} = −1 mA	[9][11]	V_{DD} − 0.4	-	-	V
		I_{OH} = −4 mA	[10][11]	V_{DD} − 0.4	-	-	V
V_{OL}	LOW-state output voltage	I_{OL} = 4 mA	[9][11]	-	-	0.4	V
		I_{OL} = 4 mA	[10][11]	-	-	0.4	V
I_{OH}	HIGH-state output current	V_{OH} = V_{DD} − 0.4 V	[6][11]	-	−4	-	mA
I_{OL}	LOW-state output current	V_{OL} = 0.4 V	[6][11]	-	4	-	mA
I_{OHS}	HIGH-state short-circuit output current	V_{OH} = 0 V	[12]	-	−45	-	mA
I_{OLS}	LOW-state short-circuit output current	V_{OL} = V_{DD}	[6][12]	-	45	-	mA
$I_{DD(CORE)}$	core supply current	V_{DD} = 1.8 V	[13]	-	60	-	mA
$I_{DD(EMC)}$	external memory controller supply current	$V_{DD(EMC)}$ = 1.8 V		-	<tbd>	-	mA
		$V_{DD(EMC)}$ = 3.3 V		-	<tbd>	-	mA
I_{BAT}	battery supply current	V_{DCDC_VBAT} = 1.2 V		-	<tbd>	-	mA
$I_{CC(osc)}$	oscillator supply current	oscillator running	[14]	-	300	-	µA
		oscillator powered down		-	-	10	µA
$I_{DD(RTC)}$	RTC supply current	oscillator running	[15]	-	300	-	µA
		oscillator powered down		-	-	10	µA
$I_{DD(ADC)}$	ADC supply current	normal	[16]	-	-	400	µA
		powered down		-	-	<1	µA
I_{DDIA}	analog input supply current	normal	[17]	-	<tbd>	-	mA
		powered down		-	<tbd>	-	µA

Table 6. Static characteristics *...continued*

T_a = –40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$I_{DDO(DAC)}$	DAC output supply current	normal [18]	-	<tbd>	-	mA
		powered down [18]	-	<tbd>	-	µA
I_{DDOA}	analog output supply current	normal [19]	-	<tbd>	-	mA
		powered down [19]	-	<tbd>	-	µA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (+25 °C), nominal supply voltages.

[2] Applies to pins $V_{DD1(CORE1V8)}$, $V_{DD2(CORE1V8)}$, $V_{DD1(FLASH1V8)}$, $V_{DD2(FLASH1V8)}$, $V_{DD(OSC1V8)}$, $V_{DD(OSC321V8)}$, $V_{DD1(USB1V8)}$, $V_{DD2(USB1V8)}$.

[3] External supply voltage; applies to pins $V_{DD3(USB3V3)}$, $V_{DD4(USB3V3)}$, $V_{DD1(IO3V3)}$, $V_{DD2(IO3V3)}$, $V_{DD3(IO3V3)}$, $V_{DD4(IO3V3)}$.

[4] Applies to pins $V_{DD(DADC3V3)}$, $V_{DD(ADC3V3)}$, $V_{DD(DAC3V3)}$, $V_{DD1(AMP3V3)}$, $V_{DD2(AMP3V3)}$.

[5] External supply voltage; applies to pins $V_{DD1(EMC)}$, $V_{DD2(EMC)}$.

[6] Referenced to the applicable V_{DD} for the pin.

[7] Including voltage on outputs in 3-state mode.

[8] The applicable V_{DD} voltage for the pin must be present.

[9] 1.8 V inputs.

[10] 3.3 V inputs.

[11] Accounts for 100 mV voltage drop in all supply lines.

[12] Only allowed for a short time period.

[13] Applies to pins $V_{DD1(CORE1V8)}$, $V_{DD2(CORE1V8)}$, $V_{DD1(FLASH1V8)}$, $V_{DD2(FLASH1V8)}$

[14] Applies to pin $V_{DD(OSC1V8)}$.

[15] Applies to pin $V_{DD(OSC321V8)}$.

[16] Applies to pin $V_{DD(ADC3V3)}$.

[17] Applies to pins $V_{DD(DADC1V8)}$, $V_{DD(DADC3V3)}$.

[18] Applies to pin $V_{DD(DAC3V3)}$.

[19] Applies to pins $V_{DD1(AMP3V3)}$, $V_{DD2(AMP3V3)}$.

9. Dynamic characteristics

Table 7. Dynamic characteristics

T_a = −40 °C to +85 °C, unless otherwise specified.[1]

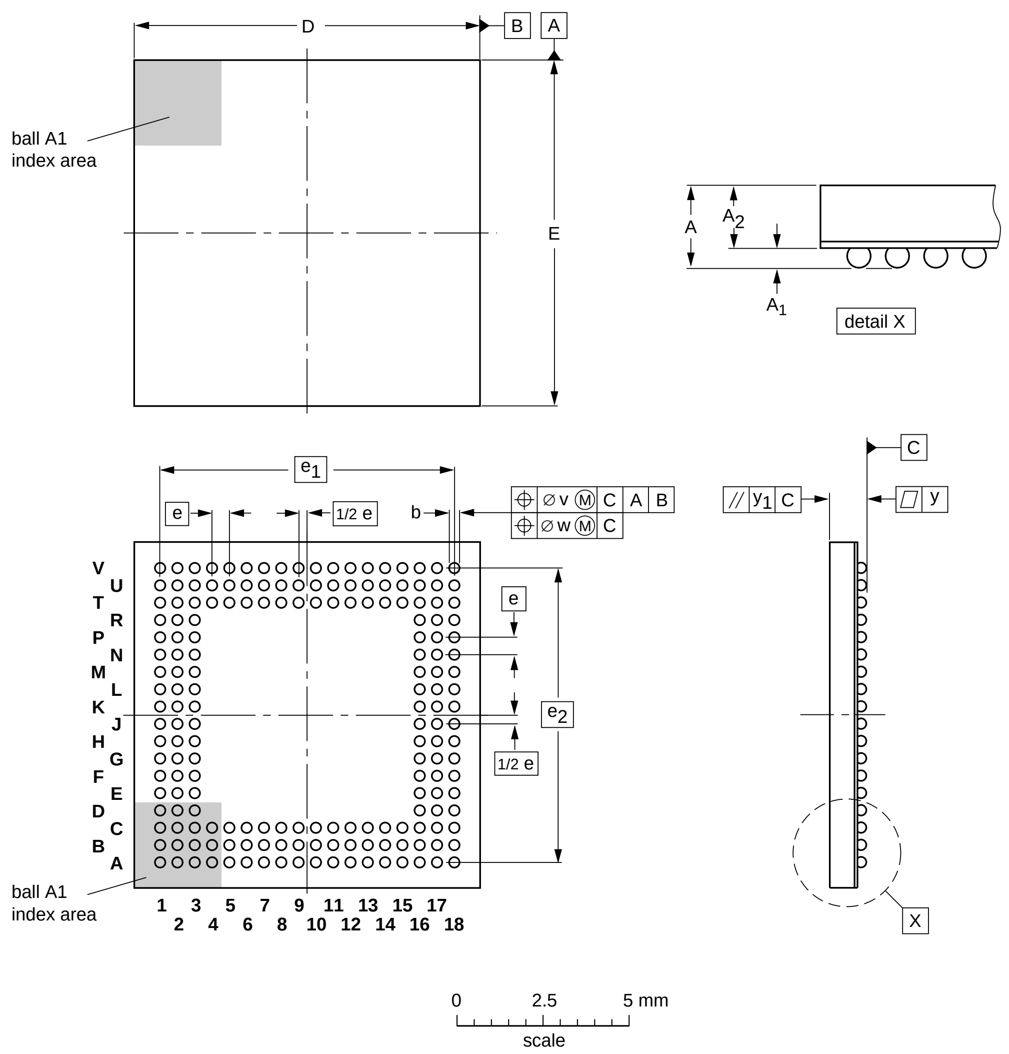
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External clock						
f_{ext}	external clock frequency	[2]	1	12	20	MHz
Port pins						
t_r	rise time		-	5	-	ns
t_f	fall time		-	5	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Supplied by an external crystal.

10. Package outline

TFBGA180: plastic thin fine-pitch ball grid array package; 180 balls; body 10 x 10 x 0.8 mm **SOT640-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.11	0.31 0.19	0.84 0.76	0.39 0.29	10.1 9.9	10.1 9.9	0.5	8.5	8.5	0.1	0.15	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT640-1		MO-195				~~01-06-07~~ 03-03-03

Fig 4. Package outline SOT640-1 (TFBGA180)

11. Abbreviations

Table 8. Acronym list

Acronym	Description
ADC	Analog-to-Digital Converter
AMBA	Advanced Microcontroller Bus Architecture
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
CISC	Complex Instruction Set Computer
CGU	Clock Generation Unit
DAC	Digital-to-Analog Converter
DMA	Direct Memory Access
FIQ	Fast Interrupt Request
GPIO	General Purpose Input/Output
IrDA	Infrared Data Association
IRQ	Interrupt Request
LCD	Liquid Crystal Display
PLL	Phase-Locked Loop
RISC	Reduced Instruction Set Computer
SD/MMC	Secure Digital/MultiMedia Card
SDRAM	Synchronous Dynamic Random Access Memory
SRAM	Static Random Access Memory
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

12. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC2880_LPC2888_1	20060622	Preliminary data sheet	-	-

13. Legal information

13.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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15. Contents

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