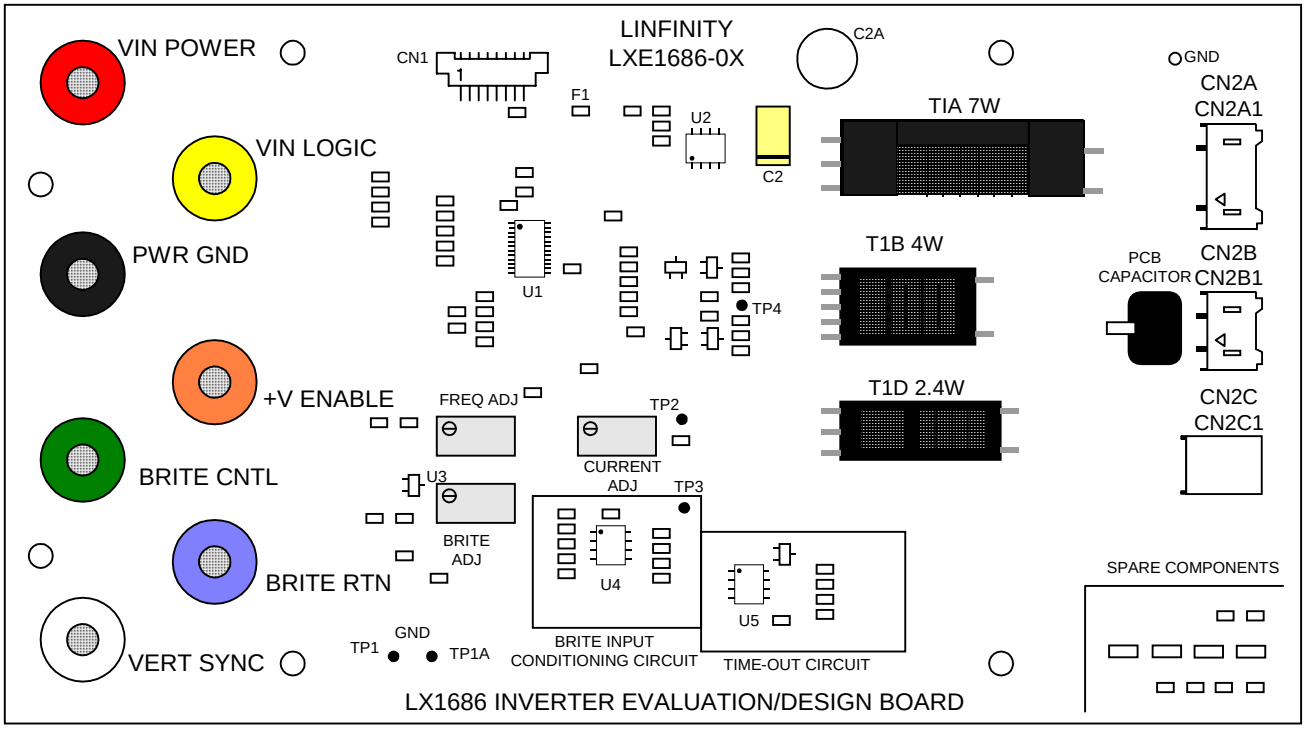
LXE1686-0x, INVERTER EVALUATION BOARD DESIGN GUIDE

LX1686 BACKLIGHT CONTROLLER

LINFINITY
A MICROSEMI COMPANY



DESCRIPTION

The LXE1686-0x CCFL Inverter Evaluation Boards are designed to demonstrate Linfinity's LX1686 Backlight Controller IC. It consists of a fully assembled and tested inverter circuit board. This design guide complements the LX1686 controller application note AN-13 that discusses the overall inverter design considerations. The purpose of the evaluation board is to allow a designer to quickly modify the basic inverter circuit to match his LCD panel requirements. It will allow easy customization of the inverter's input and output characteristics to optimize the inverter design.

LX1686 INVERTER TOPOLOGY

The LX1686 based inverter is a single-stage controller that regulates lamp current for load and line variation using a high frequency (60 to 100kHz) PWM switching technique.

Wide range digital dimming is achieved in a similar (but separate) manner using a low frequency (100 to 1000Hz) PWM lamp current burst mode technique.

Together, this topology can offer the lowest power consumption and highest electrical operating efficiencies achievable from a DC to AC CCFL inverter.

As with any high performance device, component load matching is a must to gain the most efficiency possible. Proper output transformer selection (see 'Output Transformer Selection') based on input voltage and CCFL load should be given careful consideration, for best inverter performance.

EVALUATION BOARD FEATURES

- **Brightness control input conditioning:** linear DC, potentiometer and/or PWM op-amp circuit
- **Over-voltage sensing:** output voltage limiting, open load protection circuit
- **Over-current sensing:** output current limiting, shorted load/output protection circuit
- **Open/short circuit output disabling:** timeout output disabling comparator circuit
- **Input interface:** full functionality, Banana jacks or 8 pin Molex connector
- **Output connector:** fly wire or choose from a variety of most the common industry standards
- **Output transformer:** choose from three power level transformer offerings from LINFINITY

LX1686 CONTROLLER FEATURES

- **Vertical frame rate synchronization input:** programmable to accept 45 to 500Hz
- **Brightness control input**: linear DC control input
- **Direct PWM dimming input:** logic level 100 to 1000Hz PWM, lamp current burst mode

LX1686 CONTROLLER FEATURES (CONT.)

- **Digital brightness control:** wide range dimming, lamp current burst mode control
- **Analog brightness control:** limited dimming, traditional lamp current amplitude control
- **Reverse dimming control:** positive or negative control action
- **Lamp current regulation input:** operational error amplifier
- **Over-voltage sensing input:** optional hardware configurable for voltage and/or current
- **Open lamp sensing input:** open lamp detection and strike mode activation
- **Dual output FET gate driver:** dual N-channel power FET required
- **Inverter enable/disable input:** control inverter on/off state, low off state sleep current

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1. WHAT IS INCLUDED WITH YOUR LXE1686-0X?

The items in Table 1, 2 or 3 should have been included when you received your version of the LXE1686-0x depending on the output transformer power requirements. If any of them are damaged or missing, contact LINFINITY or the distributor from which you received the kit for assistance. In order to utilize the inverter evaluation kit you must provide certain items. They are listed in Table 4.

TABLE 1. LXE1686-01 PACKING LIST

Item No.	Quantity	Description	
1	1	6.75" X 3.75" printed circuit board with components installed	
2	1	This LXE1686-01 evaluation guide	
		7WTransformer	Turns Ratio
3	1	SGE2692-1, or -3	85.0
4	1	SGE2641-1, or -3	47.2
5	1	SGE2643-1, or -3	42.5
6	1	SGE2642-1, or -3	38.6
7	1	SGE2648-1, or -3	30.4

TABLE 2. LXE1686-02 PACKING LIST

Item No.	Quantity	Description	
1	1	6.75" X 3.75" printed circuit board with components installed	
2	1	This LXE1686-02 evaluation guide	
		4W Transformer	Turns Ratio
3	1	SGE2687-1	80.0
4	1	SGE2688-1	61.5
5	1	SGE2686-1	50.0
6	1	SGE2689-1	42.1
7	1	SGE2681-1	36.4

TABLE 3. LXE1686-03 PACKING LIST

Item No.	Quantity	Description	
1	1	6.75" X 3.75" printed circuit board with components installed	
2	1	This LXE1686-03 evaluation guide	
		2.4WTransformer	Turns Ratio
3	1	SGE2690-1	80.0
4	1	SGE2668-1	61.5
5	1	SGE2671-1	50.0
6	1	SGE2680-1	42.1
7	1	SGE2675-1	36.4

TABLE 4. EQUIPMENT YOU NEED IN YOUR LAB

Item No.	Quantity	Description
1	1	Dual Variable Power Supply: Source 1 3-5.5V @500mA Source 2 Full range of system power source @1A
2	1	Multiple channel oscilloscope: 1Mhz BW, 10mV or better sensitivity.
3	1	DMM: 50V/2A range, 10mV/mA sensitivity or better, optional AC capability 500Khz BW.
4	1	Luminance Meter: 1 to 50K-unit range, 0.25 unit sensitivity or better White scale capable, typical unit of measurement, cd/m^2 (nit).
5	1	AC current probe: 500Khz BW, 1mA to 10A range, 250uA sensitivity or better.
6	1	High Voltage probe: 500Khz BW, 10kV, 10Megohm / 3pf loading or better.
7	Various	Connect leads for banana jacks or input cable with mate for Molex 53261-0890, flat blade screwdriver for pots.

2. BEFORE GETTING STARTED

LCD PANEL CHARACTERISTICS

The LCD panel manufacturers specification for your application should define CCFL (CCFT) lamp load parameters critical for proper inverter design. These parameters are usually defined as follows for minimum, typical and maximum ratings:

- Lamp current (mA rms)
- Lamp (run) voltage (V rms)
- Lamp power (Watt rms)
- Lamp current frequency (kHz)
- Lamp strike voltage (cold) at rated temperature (°C)
- Lamp connector pin-out orientation (hot and cold CCFL lead assignment)
- Lamp lifetime anticipated if lamp current is maintained within a specified range (Hours)
- Center screen or five point average light output at a reference lamp current (cd/m² or Nit)

WHAT YOU SHOULD KNOW ABOUT LCD PANEL MANUFACTURES SPECIFICATIONS:

Several of the CCFL characteristics are often those specified by the CCFL manufacturer based on their burn-in screening process. Lamp (run) voltage parameters may be padded for manufacturing process tolerance and may take into account 'near end of life' deviation values. Lamp strike voltage values may represent a bare lamp condition without benefit of the final LCD panel assembly. Lamp run voltage ratings may be up to 20% higher and strike voltage ratings may be up to 100% higher than the actual value for a CCFL mounted within an LCD assembly.

Many panel manufactures specify minimum lamp current and maximum lamp frequency ratings based on limitations of analog dimming methods. This is specified mainly to guarantee acceptable light output uniformity. Linfinity's digital wide range dimming technique eliminates low light level uniformity issues based on minimum lamp current or maximum operating frequency. Additionally, Linfinity's lamp life tests show no significant lamp life degradation due to wide range digital dimming.

Lamp wiring polarity has a significant effect on inverter performance and should be carefully observed. The 'hot' lead, or shortest lead in the LCD panel assembly, is usually the color pink or red. The 'cold' lead, or longest lead in the LCD panel assembly, is usually the color white. The 'cold' lead, or return lead, is also the lead that lamp current measurement is taken from in the LCD panel specification.

An important note (one that is often overlooked during development phase) is that the LCD panel metal framework around the CCFL must be grounded to insure proper inverter operation as well as preventing electrical shock and reducing EMI emission.

Light transmission through the LCD is typically specified for a white spectrum emission perpendicular to the panel's center, at a specified lamp current. This also includes the presence of video (blank page) at a specified contrast bias setting (if applicable). Larger panel's, greater than 7" diagonal, may specify light transmission as the average of four corner screen locations and the center. The presence of video and contrast bias is critical for proper light measurement using STN type LCD. However, light transmission through a TFT type LCD may only be affected as little 10% with or without video. Touch screens will reduce light emission as a whole and should be taken into consideration as to how this affects the LCD panel specification.

STN type LCD typically uses a split screen vertical frame rate that often requires vertical synchronization with the LINFINITY inverter's burst mode dimming, so as to avoid visual 'spook' disturbance. LINFINITY wide range digital inverters provide the 'Vsync' feature for this purpose. Often, TFT type LCD can be operated with LINFINITY inverter burst mode technique without need of vertical synchronization. In either case, experimentation is recommended to determine the need or the proper vertical synchronization rate to eliminate undesirable visual 'spook' disturbances.

APPLICATION SYSTEM POWER

Your application system power may be derived from a battery or typical AC to DC power source. In either case, fixed regulated supplies are likely in use for logic devices. The LINFINITY inverters low power logic can also share from one of these supplies, if it is fixed between 3.3V to 5.5V. Ideally, a 4.5V to 5.5V supply should be considered, as it will allow for a greater selection of lower cost power FET devices required to power the CCFL output transformer. This voltage range also allows for better dynamic range in the inverter lamp current regulation scheme.

The main inverter power can be drawn directly from the battery or main power source. However, it is not

recommended that the voltage variation exceed a 1½ to 1 range. It is possible to supply both inverter logic and main power draw to the same fixed 3.3V to 5.5V source, if application system power can accommodate. Precautions regarding inverter effects on application system power:

LINFINITY inverter topology incorporates both high frequency PWM power switching of the CCFL output transformer and low frequency PWM burst current dimming techniques. If inverter power draw is not properly conditioned or isolated from application system logic devices, interference from inverter switching frequencies may occur. Example, interference may occur in visual form, as a result of inverter noise imposed on power source shared by video processor logic.

APPLICATION SYSTEM CONTROL INTERFACE

Inverter functional controls, such as vertical synchronization and remote enable/disable should be addressed by digital means. Brightness control can be done by either linear and/or digital means. The lowest inverter parts count brightness control method would require a direct PWM logic input in the 100 to 1000Hz range. This control method should ideally have the PWM logic signal synchronized with the vertical frame rate, especially if the panel application is an STN type LCD. Other brightness control methods could be configured such as to convert a digital logic signal into a DC potential with less than 10mVpk-pk ripple from a 495mV to 2.55V range. Conversion device examples: DAC, digital potentiometer, op-amp/integrator, and R/C network.

Special consideration as to how control interfaces are presented to the inverter during system power-up sequence will affect things like initial screen brightness and stability. If various control interfaces undergo unstable transitions during system power-up, then suspending inverter enable during such time periods is recommended to avoid undesirable visual flashes or flicker.

OUTPUT TRANSFORMER SELECTION

Output transformer selection needs to be based on two criteria:

1. Maximum operational lamp power
2. Secondary to primary turns count ratio

The first criteria is simply selecting from one of three LINFINITY transformer styles based on your applications maximum lamp power. This selection will lead to which version of the LXE1686-0x evaluation board you require. Lamp power consumption can be derived from the LCD MFR specification (or actual lab measurements) of lamp current multiplied by lamp run voltage.

Linfinity offers the following three transformer types for the indicated maximum recommended power level. Each power level is matched with a corresponding version of the evaluation board:

- LMT3811 : 7.0Watt LXE1686-01
- LMT2110 : 4.0Watt LXE1686-02
- LMT2608 : 2.4Watt LXE1686-03

The second criteria for transformer turns ratio, can be estimated from the following definitions and formula:

Tratio Transformer secondary / primary wire turns count

Vlamp Maximum lamp run voltage value (actual value at maximum operational lamp current)

Vin Minimum voltage value of inverter main input power

f Transformer correlation factor, typical value = 1.85 (unless otherwise specified)

Estimation formula: $Tratio = \frac{Vlamp}{Vin \times f}$

Select from available LMI output transformer turns ratios that are closest to the value that you estimate. If one does not yet exist, please contact an LMI inverter applications engineer to specify a custom.

Mount transformer choice in one of the three T1-A, B, C locations that matches transformer footprint.

INVERTER DESIGN BOARD FEATURES

The LXE1686-0x inverter evaluation/design board will require separate main (VIN POWER) and logic(VIN LOGIC) power supplies.

All critical inverter input and output interfaces are provided via a variety of fly wire, banana jack and common connector options.

Inverter board is pre-configured with optional brightness control conditioning circuit that can be adjusted via the BRITE CNTL input or a board mounted multi-turn potentiometer (R30B). This flexible conditioning circuit allows for linear DC or PWM brightness control from 0 to 2.5V and 500 to 5000Hz. Minimum and maximum brightness thresholds are established thru this configurable

combination op-amp/integrator conditioning circuit as well.

An optional open/short lamp timeout-disable comparator circuit is also available, and can be implemented with one jumper placement at RJ8.

Inverter board is pre-configured to deliver from 3 to 18mArms lamp current, adjustable via the Current ADJ on board multi-turn potentiometer (R11B).

Inverter board is pre-configured to operate from 65 to 75kHz lamp current, adjustable via the FREQ ADJ on board multi-turn potentiometer (R10B).

Three critical inverter setup probe test points are provided, including twenty-seven information test points to help you design as well as understand the LMI LX1686 inverter operating concept. Oscilloscope pictures of typical inverter waveforms at a number of these test points are also provided for reference.

3. BOARD SETUP PROCEDURE, CRITERIA & OPTIONS

BASIC INPUT/OUTPUT INTERCONNECTS & MEASUREMENT

Ground panel frame to electrical system ground. If panel is an STN style LCD, apply a blank (white) screen video for light measurements.

Determine your method of lamp current measurement; current probe, percentage of inverter input power to known lamp power (~ 120%) or known light output for a given lamp current. If using the light output measurement, allow for CCFL temperature stabilization (usually 20 to 40 minutes).

Setup inverter for nominal application system logic supply voltage at 'VIN LOGIC' & 'PWR GND' terminals.

Simulate application system main power source with a variable power supply that can be adjusted over the full variation range of the application system at 'VIN POWER' & 'PWR GND' terminals. Adjust 'BRITE ADJ' R30B full clockwise for maximum brightness condition.

Adjust 'FREQ ADJ' R10B for desired lamp current operating frequency (70kHz nominal).

RECOMMENDED LAMP CURRENT OPERATING FREQUENCY

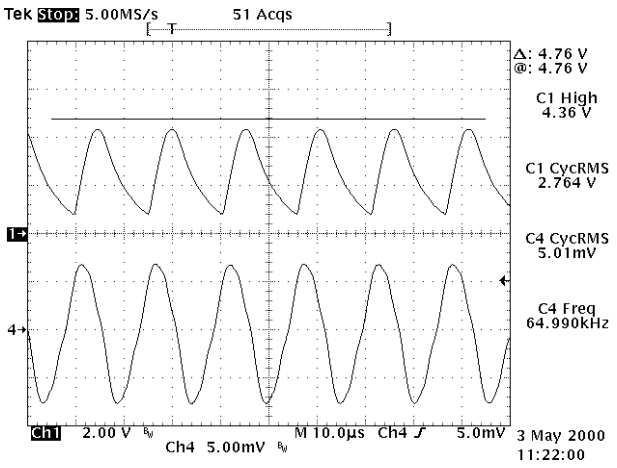
Recommended operating frequencies for the LMI magnetic types: 70 to 100kHz for 2.4 and 4.0Watt, 65 to 75kHz for 7.0Watt. C6 may be reduced in value (120pF provided as spare component C26) to obtain a higher operating frequency range.

Lamp current regulation

Establish the lowest main input voltage (VIN POWER) where target design lamp current, input power or light output can be maintained. This will require an initial high 'Current ADJ' setting at R11B (full clockwise) to gain maximum inverter drive capability. Optimum transformer turns ratio selection is achieved when lowest main input voltage is that of the lowest application system potential, where design target condition are maintainable. Decrease 'Current ADJ' R11B until noted reference begins to decrease at lowest input voltage condition.

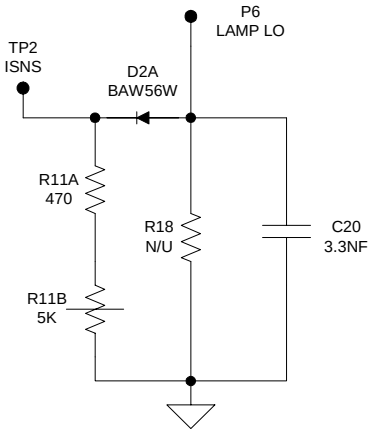
Ideally, use the light output reference measurement for final setting as follows; increase inverter input voltage to the midrange or nominal input power potential. Readjust 'Current ADJ' R11B until reference light output level condition is re-established.

Using an O-scope probe, determine the dc potential at P4. This DC potential is the equivalent to the 'common-mode' threshold voltage of the lamp current regulation op-amp. Make a reference of this potential on the scope scale gradient and place the scope probe on TP2. Observe TP2 waveform over the entire main input supply range. The end goal will be to achieve an AC waveform peak on P2 that doesn't exceed the DC reference potential, but ideally rides just below it. In the scope shot below the bar indicates the level at P4 (VDD) channel 1 is TP2 (ISNS) and channel 4 show the output current low return side. Note that the peak value of TP2 is below the P4 level. In this scope shot the main input supply was at the nominal input voltage, not the extremes.



To reduce TP2 peak amplitude, increase C13 (2.2nF) value or vise-versa (this will change lamp current setting, requiring readjustment of 'Current ADJ' R11B). Observe light output over the entire inverter input supply range. Light output variations over low to high supply condition may be balanced out by varying the ratios of R11A + R11B to R18. Often R18 is not needed to accomplish balanced light output, but when

balance is required, the best results usually occur when R18 and the sum of R11A & R11B are equal in value.



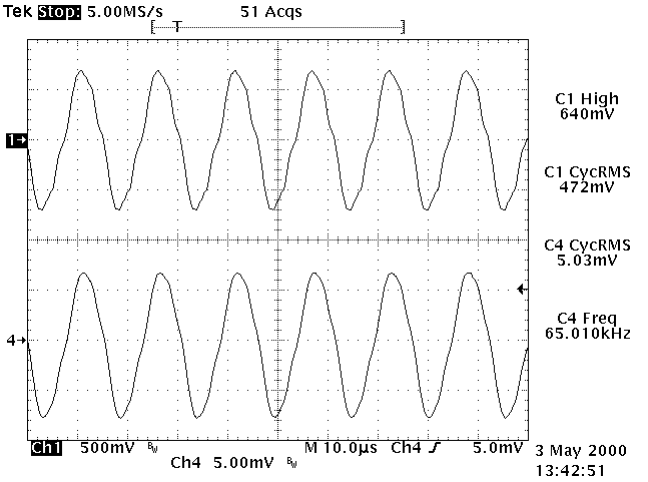
OUTPUT VOLTAGE LIMITING, SENSING & MEASUREMENT

The degree of open load or lamp strike potential can be limited to either the lamp MFR requirement or the breakdown rating of the magnetic (1800Vrms, for all three styles). The effective threshold is set by the ratios of C18 (2.2pF PCB reference) to C19 (2.2nF).

Capacitor tolerance and circuit response time will effect how accurately this threshold limit can be maintained. A safe operating margin should be taken into consideration for your design expectations. The recommended pre-assembled component values noted will limit output to approximately 1500Vrms (2100Vpk).

If higher strike output potentials are desired but cannot be achieved, then the maximum strike sweep frequency may need increasing. This can be accomplished by reducing the impedance of both R2 (51K) and R3 (9.1K) by approximately the same percentage. The pre-assembled component values noted will sweep strike frequency by approximately 3 times the normal operating frequency to excite the open load resonance of the output transformer.

The waveform present at TP4 will closely reflect that of the high voltage potential presented to the lamp. TP4 potential is represented as the ratio of C18 (2.2pF PCB reference) to C19 (2.2nF). The pre-assembled component values noted create an approximate 1000:1 divider network that could be used to help determine both open load and normal run lamp voltage potentials. In the scope picture below channel 1 is TP4 the center of the 1000:1 capacitive divider and channel four is the lamp low side run current. This node indicates that the nominal RMS lamp voltage @ 5mARMS is 472V.



Once again, capacitor tolerance will effect how accurately TP4 measurement might actually be. The benefit of this node, as a means of measurement, is that there is no additional capacitive or resistive loading to the circuit, as would be associated with a measurement probe placed directly on the output.

DIMMING CONTROL CIRCUIT CONDITIONING

There are many ways to interface inverter dim control from any given application system. The following criteria are required at the inverter TP3 'BRITE' input (with the exception of direct PWM control):

- BRITE signal should have low ripple content, ideally, less than 10mVpk-pk.
- BRITE signal should have high and low threshold voltage points that represent desired minimum and maximum brightness settings.
- Tolerance of the minimum brightness threshold setting should be relative to the optical dynamic dimming range desired.
- BRITE signal should not exceed the setting that establishes minimum desired brightness during inverter operation.

The LXE1686-0x inverter evaluation/design board is pre-assembled with a precision voltage reference (U3) and an op-amp integrator conditioning circuit (U4) to establish brightness control range with high and low threshold settings. This circuitry is furnished as an example of one method to accomplish wide dynamic range brightness control while accepting both PWM and or linear DC input signals. Your application may not require these added components if the aforementioned design criteria could be met by some other means.

The LXE1686-0x inverter evaluation/design board can be configured numerous ways for brightness control by jumper option placement. Basic brightness control options are as follows:

- Brightness control can be configured for linear DC input (bypass optional U4 conditioning circuit) with the following jumper and component changes: RJ3=N/U, RJ4=N/U, R5=2.0K & C10=220nF
- Brightness control polarity can be reversed such that a low level input results in maximum brightness by placing a 10-Ohm jumper at RJ1.
- Brightness control action can be configured as a direct function of amplitude lamp current (traditional non-burst mode) by placing a 10-Ohm jumper at RJ2.
- Direct PWM input (wide dynamic range burst mode) can be configured with the following jumper and component changes: RJ3=N/U, RJ4=N/U, RJ5=10-Ohm, RJ6=N/U, RJ7=10-Ohm, VERT SYNC grounded, R5=2.0K, C5=10-Ohm & C7=10-Ohm

Note that configuration option component and jumper change items can be found in the 'Spare Components' section of the LXE1686-0x inverter evaluation/design board. These components; C24 thru C27, R34 thru R35, and RJ9 thru RJ12 can all be identified on LXE1686 schematic page.

- Direct PWM input is a highly recommended method to achieve wide dynamic (burst mode) brightness control, with minimum component count. The following criteria is required for direct PWM method brightness control:
- PWM signal logic level amplitude should be no less than 65% of the VIN LOGIC supply voltage.
- PWM signal frequency should range from 100 to 1000Hz (lower frequency offers wider optical dynamic dimming range).
- PWM frequency and duty should remain stable and jitter free during inverter operation.
- PWM signal positive duty should not drop below the minimum duty that establishes minimum desired brightness during inverter operation.
- PWM frequency should ideally be synchronized to application system vertical refresh rate during inverter operation. This is particularly necessary for STN style LCD panels, to avoid visual spook interference.

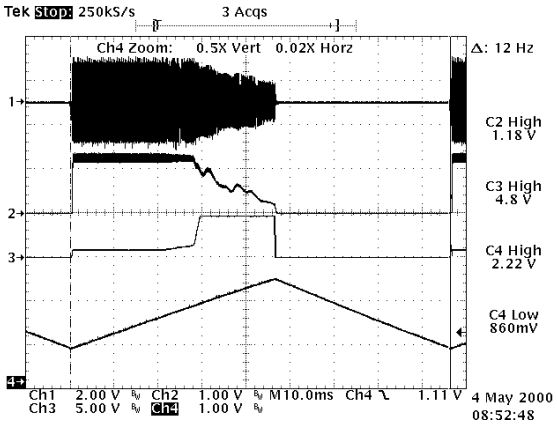
OPTIONAL OPEN LOAD TIME-OUT COMPARATOR CIRCUIT

For safety reasons, inverter design applications may require high voltage output to be quickly disabled, in the event of an open load condition (such as a broken lamp). The LXE1686-0x inverter evaluation/design board is pre-assembled with an optional comparator circuit (U5) that provides this function. By placing a 10-Ohm jumper at RJ8, this feature will be fully enabled for design evaluation. The preset time-out period is approximately 2 seconds. Vary the RC time constant values of R33 or C23 if a change in time-out period is desired.

SHORTED OUTPUT CURRENT LIMITING CIRCUIT

For safety reasons, such as UL (or similar) requirement, inverter design applications may require output current to be limited to a specified value, in the event of a shorted load condition that defeats normal output current regulation. The LXE1686-0x inverter evaluation/design board is pre-assembled with a current limiting sensing circuit (Q1 & R14) that provides this function. The preset output current limiting value is approximately 25mA-pk (within UL requirement). Change the value of R14 (82 Ohm) inversely for a desired change in output current limiting.

Channel 1 below shows P13 the top on the current sense resistor. Channel 2 connects to P14 (VSNS), channel 3 to P15 (VCOMP) and channel 4 to P24 (TRI_C). Since the lamp regulation circuit is defeated the controller will proceed to the lamp strike configuration of ramping the output frequency following the TRI_C ramp generator.

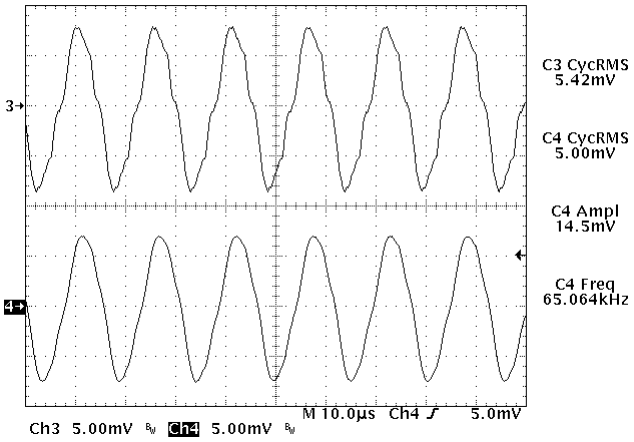


Note that this circuit is not required for normal inverter operation. It does however; provide protection against inverter damage as well as user safety, in the event of a shorted load condition that defeats normal output current regulation.

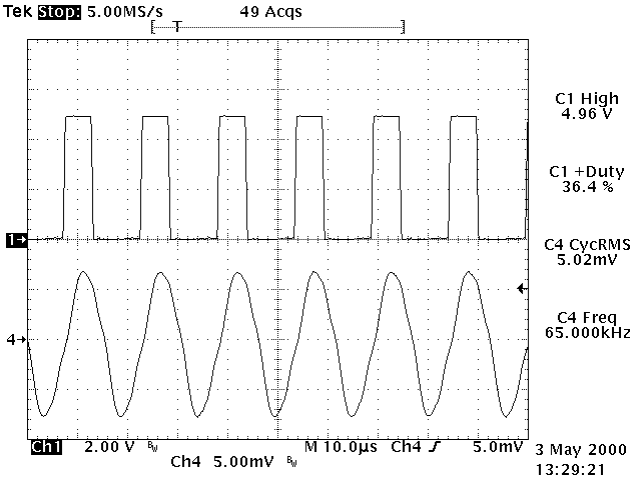
4. OSCILLOSCOPE WAVEFORM PICTURES

The following oscilloscope waveform pictures are provided as a reference to illustrate typical inverter operating conditions under a typical lamp load, for test points of visual interest. Variation in waveforms that

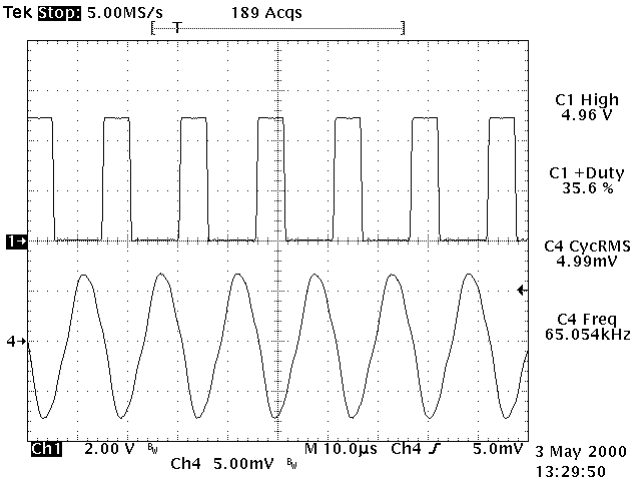
might be compared to these may result based on differences in operating conditions, lamp load, and component selection.



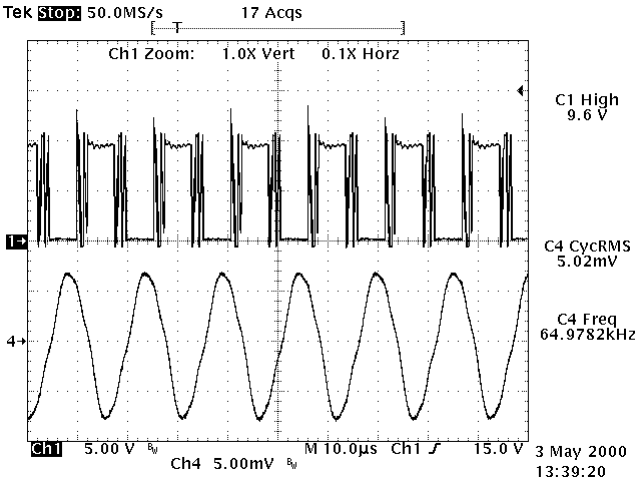
Chan 3 lamp high side (hot) output current
Chan 4 lamp low side return wire RMS current

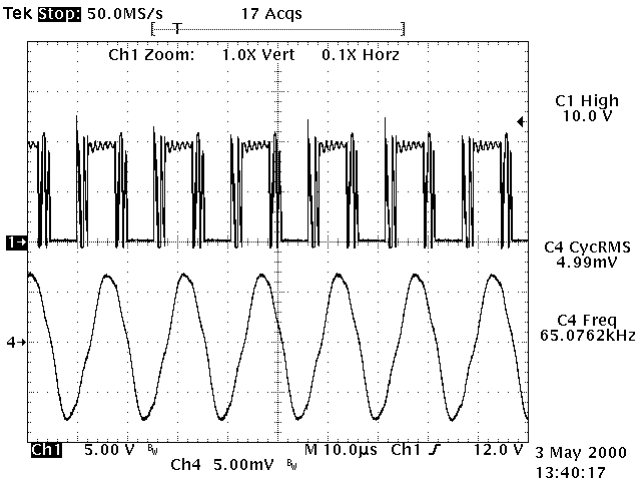


The scope shots above and below show P9 and P10 respectively. The LX1686 AOUT and BOUT FET drive

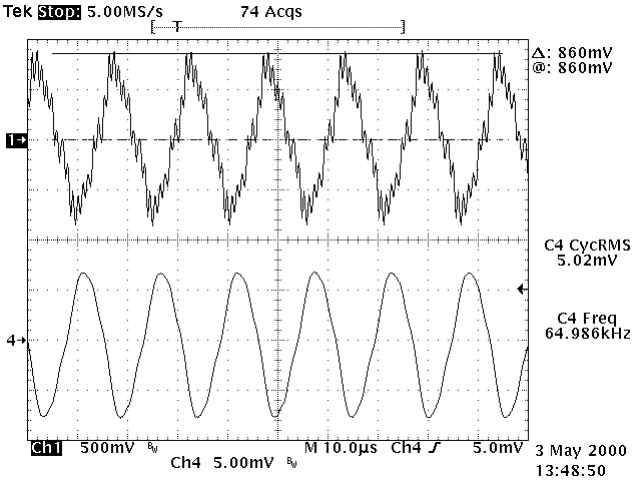


The next two shots are P11,12 outputs of the FETS driving the transformer primary windings. Note the ringing is a expected condition.

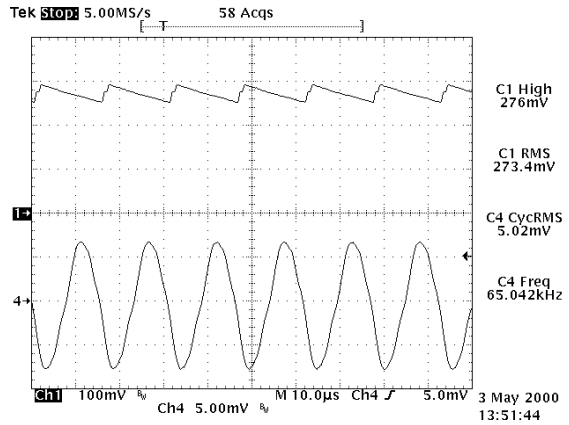




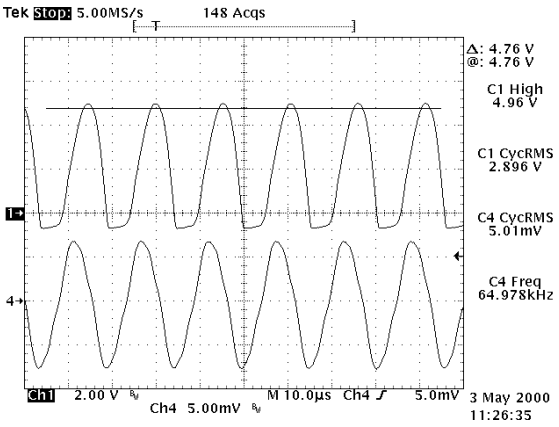
This scope picture below shows P13 the voltage developed across R14. This is during the normal run condition and is below the threshold needed to shutdown the output drive.



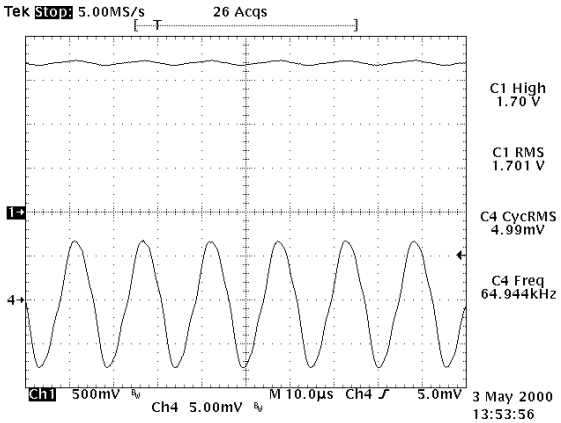
Chan 1 P14 (VSNS)



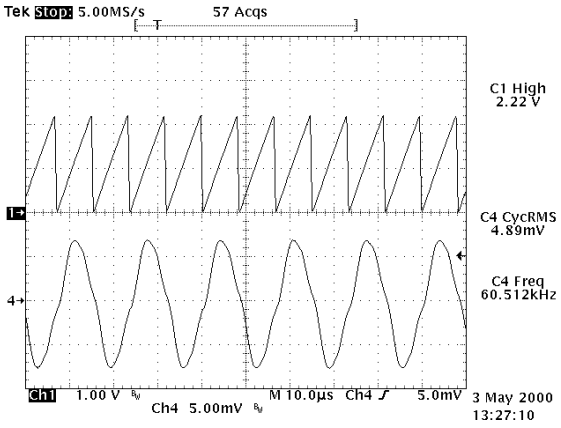
Chan 1 P6 (clamped lamp return)



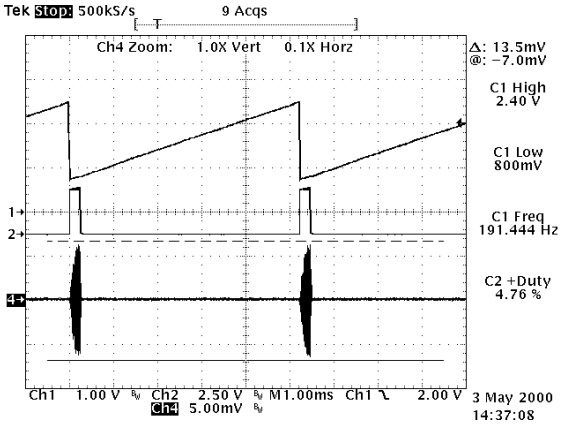
Chan 1 P7 (ICOMP)



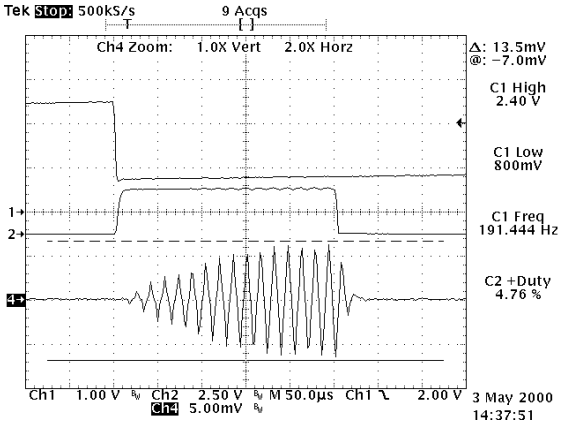
Chan 1 P8 (Ramp_C)



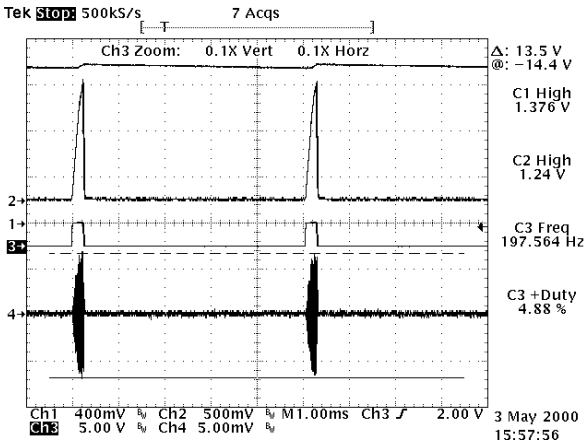
Chan 1 P16 (VCO_C) Free Run
Chan 2 P17 (BRT)
Chan 4 Output Current (~5% duty cycle)



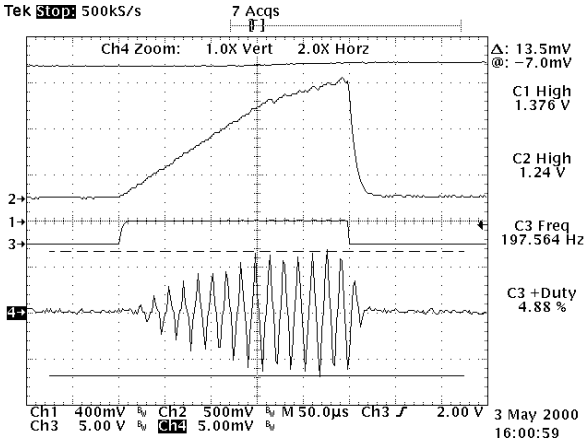
Zoom shot of previous



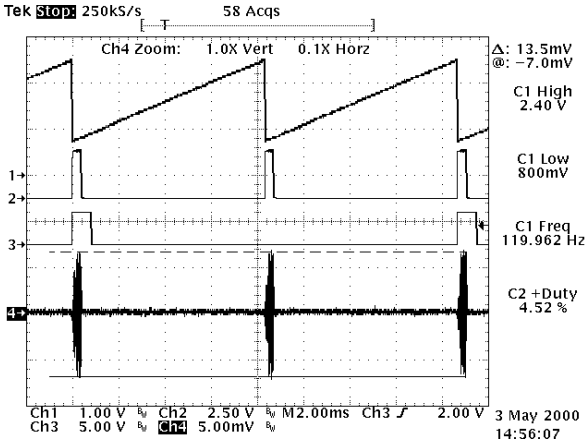
Chan 1 P5 (OLSNS)
Chan 2 P7 (ICOMP)
Chan 3 P17 (BRT)
Chan 4 Output Current



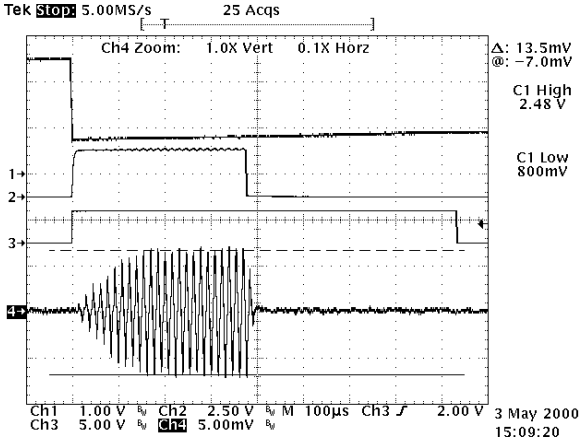
Zoom shot of above



Chan 1 P16 (VCO_C)
Chan 2 P17 (BRT)
Chan 3 P26 (FVERT)
Chan 4 Output Current

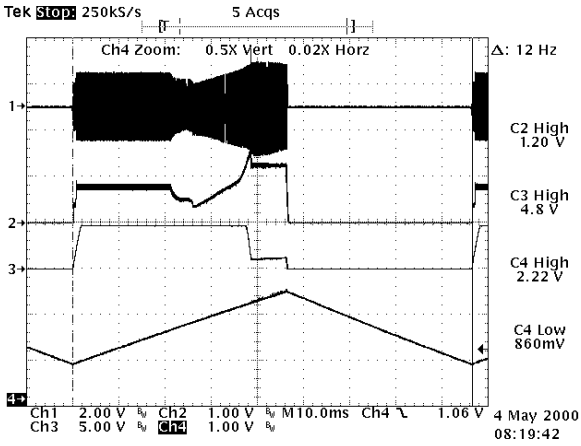


Chan 1 P16 (VCO_C)
Chan 2 P17 (BRT)
Chan 3 P26 (FVERT)
Chan 4 Output Current

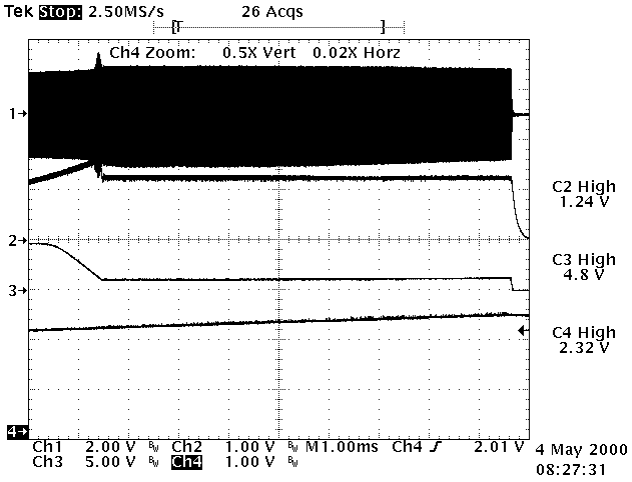


This next shot shows the strike method and open circuit clamp. As the TRI_C ramp oscillator increases the output frequency stays fixed until TRI_C reaches the ramp change threshold of about 1.6V. Above this threshold the output frequency and correspondingly the output voltage increases until it hits the overvoltage clamp. It remains at or near the clamp voltage until the timeout period during the fall time of TRI_C, after which it will attempt to strike the lamp again.

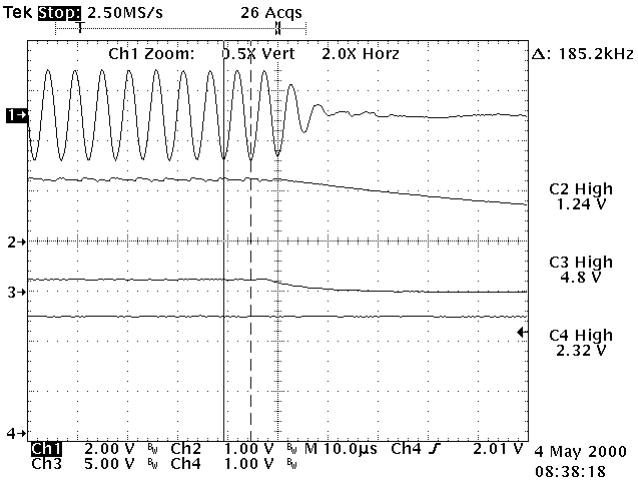
Chan 1 TP4 (capacitive divider)
Chan 2 P14 (VSNS)
Chan 3 P15 (VCOMP)
Chan 4 P24 (TRI_C)



Zoomed in shot of strike and overvoltage clamp.



The shot below shows the peak frequency reached at the peak of the TRI_C ramp 185KHz. This is in contrast to the nominal run frequency of 65KHz.



5. PCB LAYOUT CONSIDERATIONS

POWER AND SIGNAL PLANE

Inverter PCB layout should be initially separated into power and signal/analog level planes. Grounding of these two planes should only be connected at one common node, to avoid noise induction on sensitive circuits. Ideally, this common node should be at the main power filtering capacitor. Power level components begin with the main power input connector and end with the output transformer center-tap. The FET sources conduct high current levels back onto the power ground plane. The main filtering capacitor should be located in close proximity to the FET sources and output transformer center-tap. The LX1686 VSS_P (pin2) and VDD_P (pin23) should also be treated as power level nodes, as they represent FET gate driver circuitry internal to the LX1686. All other circuitry can be treated as signal/analog level.

HIGH VOLTAGE CREEPAGE

Precautions with the high voltage secondary side of the output transformer need to be observed. As this inverter evaluation board is a single-ended concept, only one pole of the output transformer will be at high potential. This pole will connect to a ballast capacitor, a capacitor divider then terminate to the high side lamp output connector. These items will all be at high potential and need at least 3mm of creepage separation from all lower potential circuitry. Solder masking of trace layout is required. It is a popular

practice to provide a 1mm wide thru slot between exposed solder contact points that are within 4mm of one another (where high voltage potential exists) to help disperse dust collection. No surface side traces should route directly beneath the secondary portion of the output transformer to avoid high voltage breakdown.

HEAT TRANSFER AND NOISE RADIATION

It is acceptable and recommended to place large copper areas beneath the output transformer primary (but not beyond bobbin insulator) to help transfer heat radiation. It is also recommended to enlarge the copper areas connecting the FET drains and sources for the same reason. It is not recommendable to place any component circuitry (other than output transfer) within 4mm of the output transformer secondary to avoid the effects of high field noise radiation.

PCB CAPACITOR FABRICATION

A small Pico-Farad value high voltage capacitor is recommended for use on LX1686 inverter designs.

This capacitor accomplishes two critical functions:

- Reduce the open circuit self resonance of the output transformer
- Configuration of a capacitive divider network to sense and limit output transformer voltage potential

This capacitor (if used) can be either a vendor component or it can be fabricated within your PCB layout.

Follow the definitions and approximated formula below to fabricate a PCB capacitor (accuracy of ± 20%).

A	Copper area of each opposing PCB plate surface (millimeter ²)
D	Distance between opposing PCB plate surfaces (millimeter)
C	Desired capacitance (Farad)
f	Correlation factor (~ 20E12 millimeter/Farad)

Approximate formula: $A = D \times C \times f$

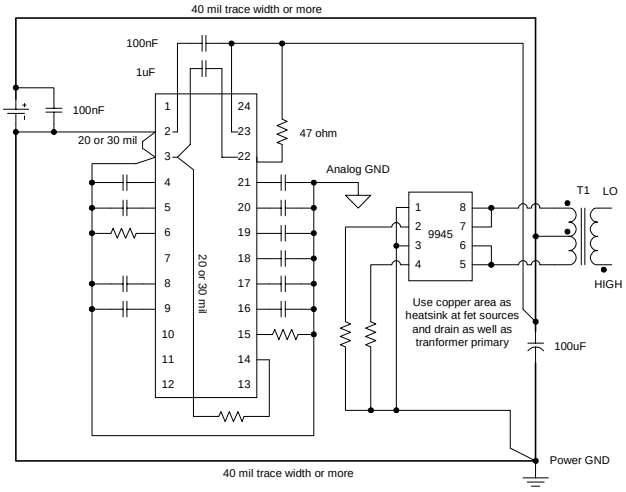
Notes:

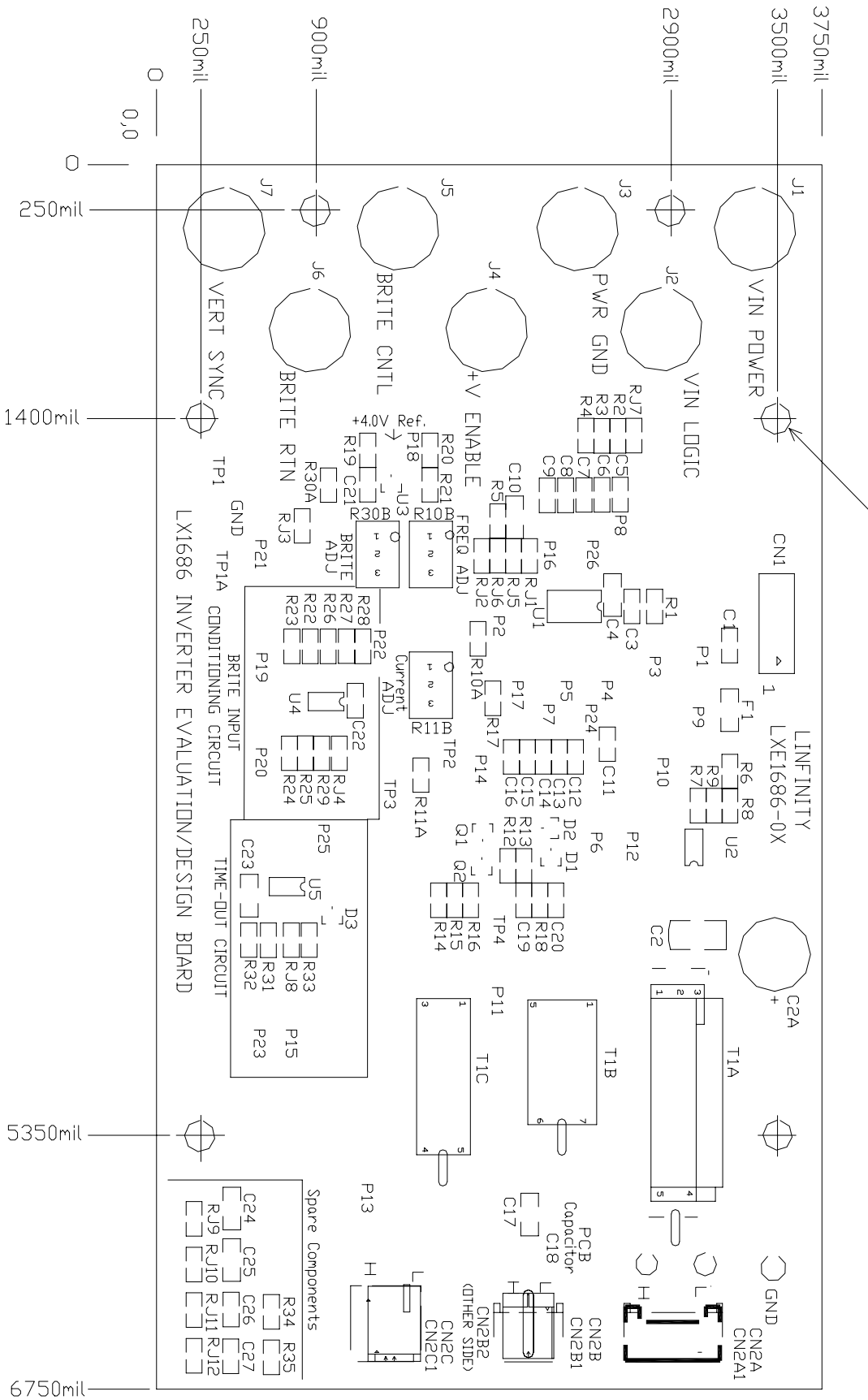
'D' should not be less than 0.70mm and should discount for copper thickness.

'A' should be round or have radius edges if rectangular in shape.

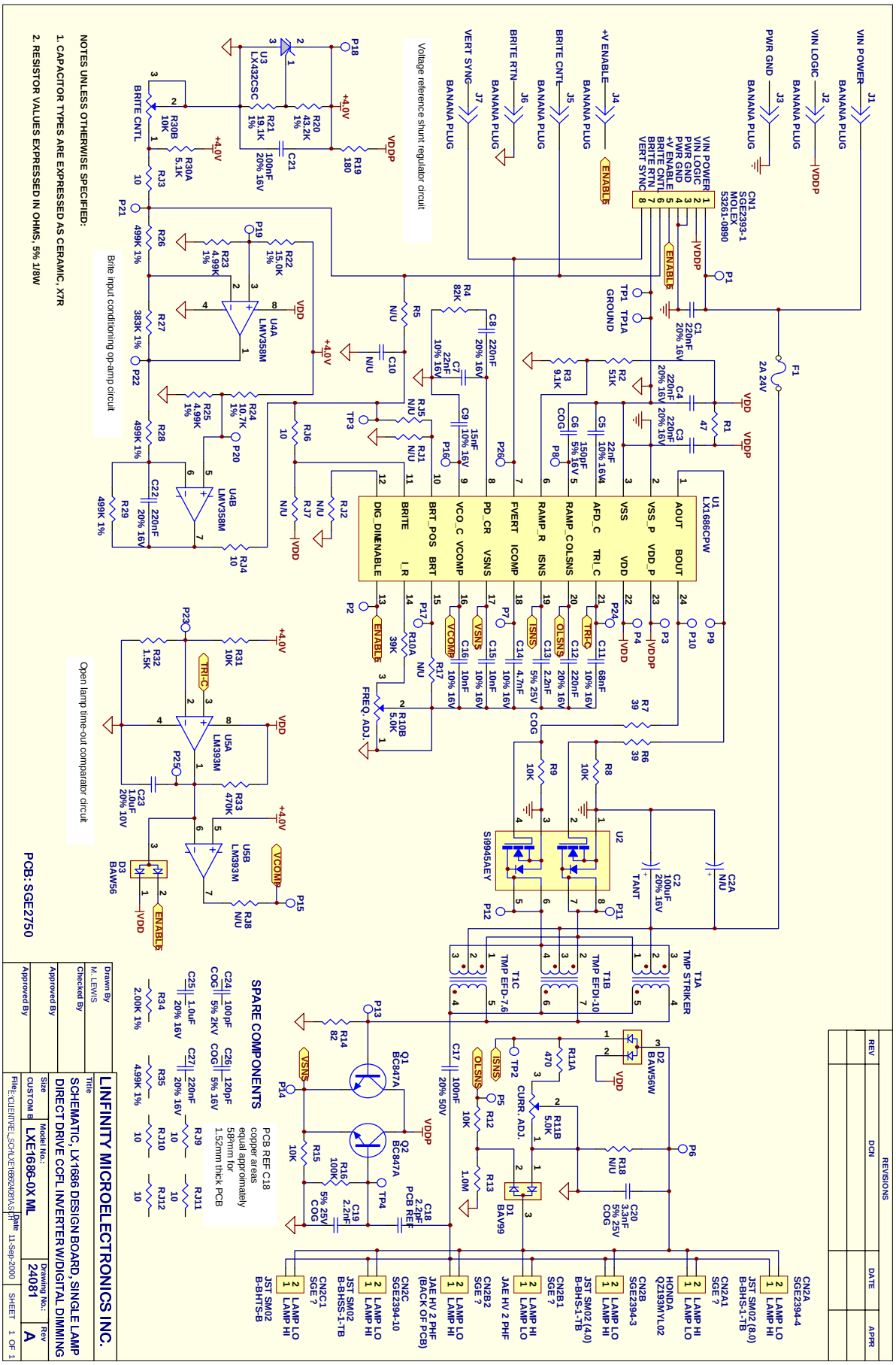
The following drawing will provide a reference for critical component placement and power and ground PCB trace routing as described in the first paragraph of this section.

LX1686 Ideal PCB Power Trace Routing and Critical Component Placement





Appendix A: Board component Placement/Test Points



Appendix B: Circuit Schematics