

M2001 Series

5x7 mm, 3.3 Volt, CMOS/LVPECL/LVDS, Clock Oscillator



- Low cost oscillator series with jitter performance optimized specifically for Fibre Channel applications. CMOS, LVPECL, and LVDS versions available.
- Ideal for Fibre Channel, Storage Area Networks (SAN), and HDD Control

Ordering Information		M2001		1	5	T	L	N	00.0000 MHz
Product Series									
Temperature Range									
1: 0°C to +70°C	2: -40°C to +85°C								
6: -20°C to +70°C	7: -0°C to +85°C								
8: 0°C to +50°C									
Stability									
3: ±100 ppm	4: ±50 ppm								
6: ±25 ppm	5: ±35 ppm								
Output Type									
F: Fixed	T: Tristate								
Symmetry/Output Logic Type									
C: 45/55% CMOS	L: 45/55% LVDS								
P: 45/55% PECL									
Package/Lead Configurations									
N: Leadless Ceramic									
Frequency (customer specified)									

	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
	Frequency Range	F	53.125		125	MHz	CMOS
			53.125		156.25	MHz	PECL/LVDS
	Operating Temperature	T _A	(See Ordering Information)				
	Storage Temperature	T _S	-55		+125	°C	
	Frequency Stability	ΔF/F	(See Ordering Information)				See Note 1
	Aging						
	1st Year			±2		ppm	
	Thereafter (per year)			±1		ppm	
	Input Voltage	V _{CC} /V _{DD}	3.135	3.3	3.465	V	
	Input Current	V _{DD} /I _{DD}			60	mA	CMOS/LVDS
					100	mA	PECL
	Output Type						CMOS/PECL/LVDS
	Load		15 pF 50 Ohms to V _{CC} -2 VDC 100 Ohm differential load				CMOS (See Note 2) PECL (See Note 3) LVDS (See Note 4)
	Symmetry (Duty Cycle) (Per Symmetry Code)		45	50	55	%	50% V _{DD} (CMOS)
			45	50	55	%	V _{CC} -1.3 VDC (PECL)
			45	50	55	%	1.25 VDC (LVDS)
	Output Skew				200	ps	PECL
	Differential Voltage	V _O	250	340	450	mV	LVDS
	Logic "1" Level	V _{OH}	90% V _{DD} V _{CC} -1.02 1.375			V V V	CMOS PECL LVDS
	Logic "0" Level	V _{OL}			10% V _{DD} V _{CC} -1.63 1.125	V V V	CMOS PECL LVDS
	Output Current		-4		+4	mA	CMOS
	Rise/Fall Time	T _r /T _f		0.35 .50	3 0.55 1.0	ns ns ns	CMOS @ 20/80% LVPECL @ 20/80% LVDS @ 20/80%
	Tristate Function		80% V _{DD} min or floating: output active 20% V _{DD} max: output disables to high-Z				
	Start up Time		5				ms
	Peak to Peak Jitter (+/-)	T _J		10 15	15 20	ps ps	@ BER 1E-12 (See Note 5) CMOS PECL/LVDS

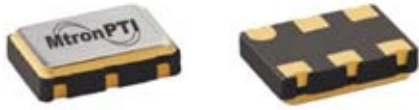
1. Inclusive of initial tolerance, deviation over temperature, shock, vibration, voltage, and aging.
2. See load circuit diagram #2.
3. See load circuit diagram #5.
4. See load circuit diagram #9.
5. See jitter test circuit in Figure 1.

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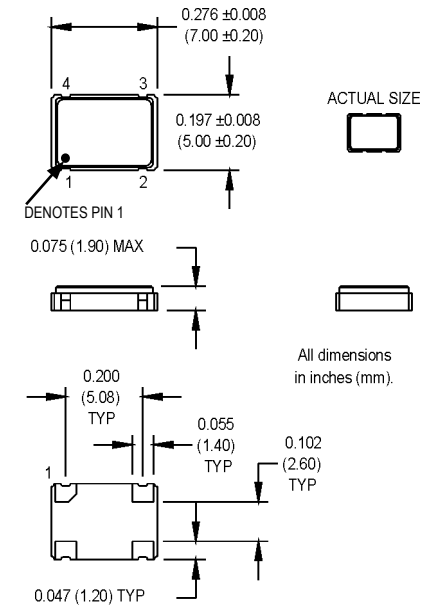
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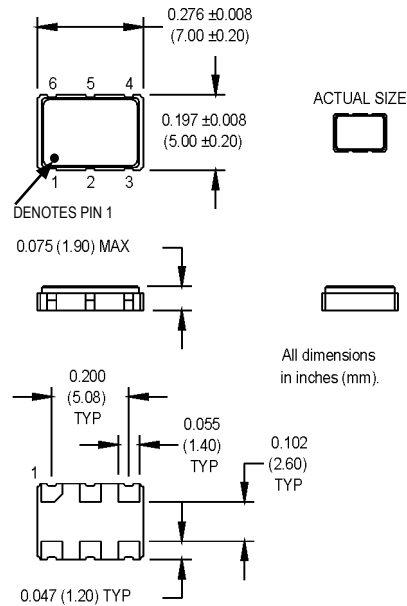
CMOS Output



Pin Connections

PIN	FUNCTION
1	Tristate/NC
2	Ground
3	Output
4	+Vdd

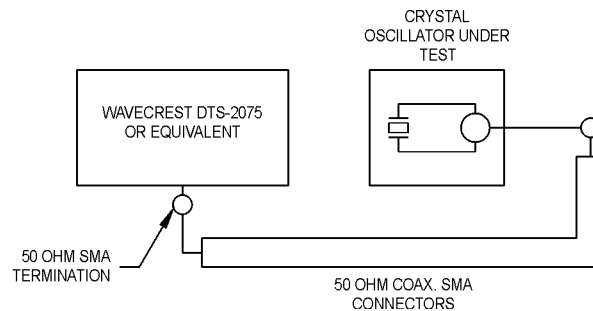
LVPECL/LVDS Output



Pin Connections

PIN	FUNCTION
1	Tristate
2	N/C
3	Ground
4	Output1/ Q
5	Output2/ $\overline{Q}$
6	+Vdd

Figure 1



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