M29F080D

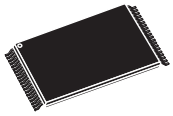
8 Mbit (1Mb x8, Uniform Block) 5V Supply Flash Memory

PRELIMINARY DATA

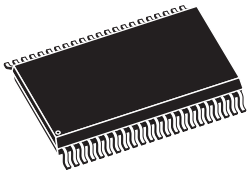
FEATURES SUMMARY

- SUPPLY VOLTAGE
  - V_{CC} = 5V ±10% for PROGRAM, ERASE and READ OPERATIONS
- ACCESS TIME: 55, 70, 90ns
- PROGRAMMING TIME
  - 10µs per Byte typical
- 16 UNIFORM 64Kbyte MEMORY BLOCKS
- PROGRAM/ERASE CONTROLLER
  - Embedded Byte Program algorithms
- ERASE SUSPEND and RESUME MODES
  - Read and Program another Block during Erase Suspend
- UNLOCK BYPASS PROGRAM COMMAND
  - Faster Production/Batch Programming
- TEMPORARY BLOCK UNPROTECTION MODE
- COMMON FLASH INTERFACE
  - 64 bit Security Code
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code: F1h

Figure 1. Packages



TSOP40 (N)
10 x 20mm



SO44 (M)

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SUMMARY DESCRIPTION

The M29F080D is a 8 Mbit (1Mb x8) non-volatile memory that can be read, erased and reprogrammed. These operations can be performed using a single low voltage 5V supply. On power-up the memory defaults to its Read mode where it can be read in the same way as a ROM or EPROM.

The memory is divided into 16 uniform blocks of 64Kbytes (see Figure 5, Block Addresses) that can be erased independently so it is possible to preserve valid data while old data is erased. Blocks can be protected in groups of 4 to prevent accidental Program or Erase commands from modifying the memory. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The memory is offered in TSOP40 (10 x 20mm) and SO44 packages. Access times of 55, 70 and 90ns are available. The memory is supplied with all the bits erased (set to '1').

Figure 2. Logic Diagram

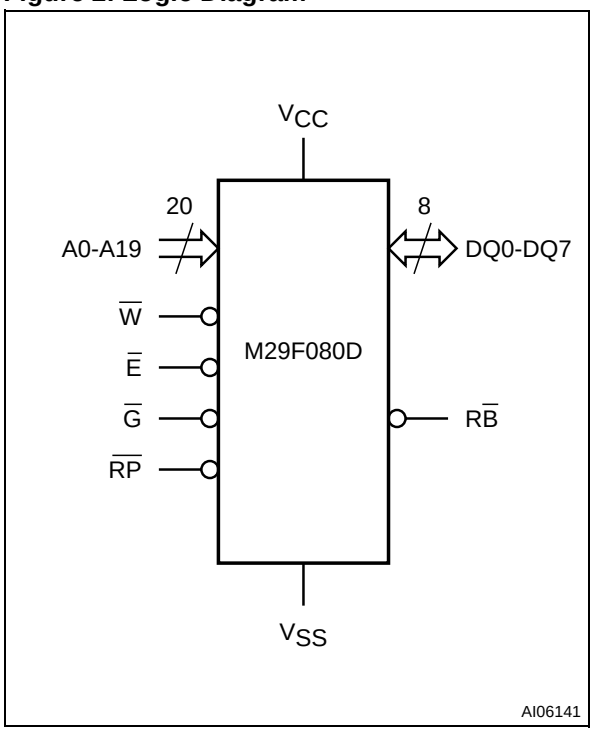


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 3. TSOP Connections

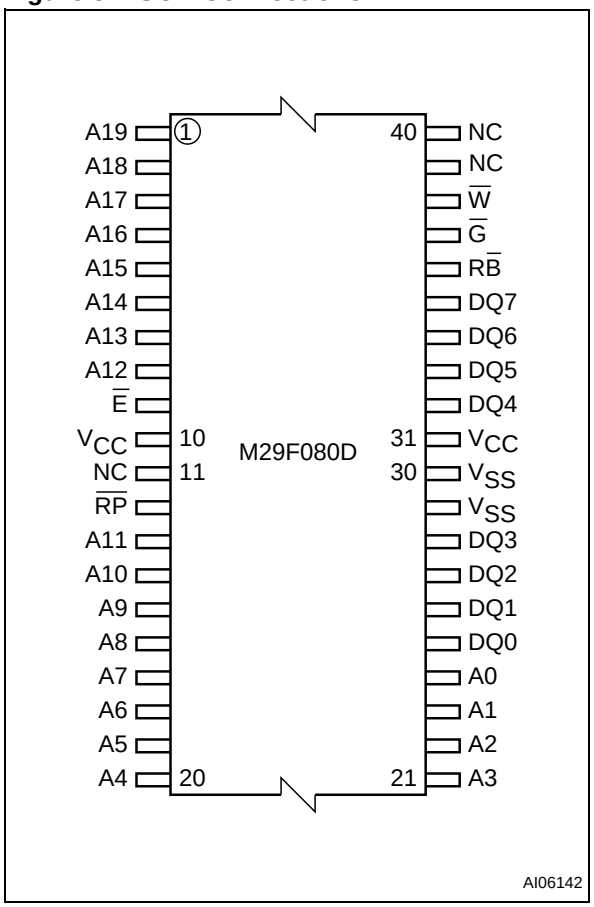


Figure 4. SO Connections

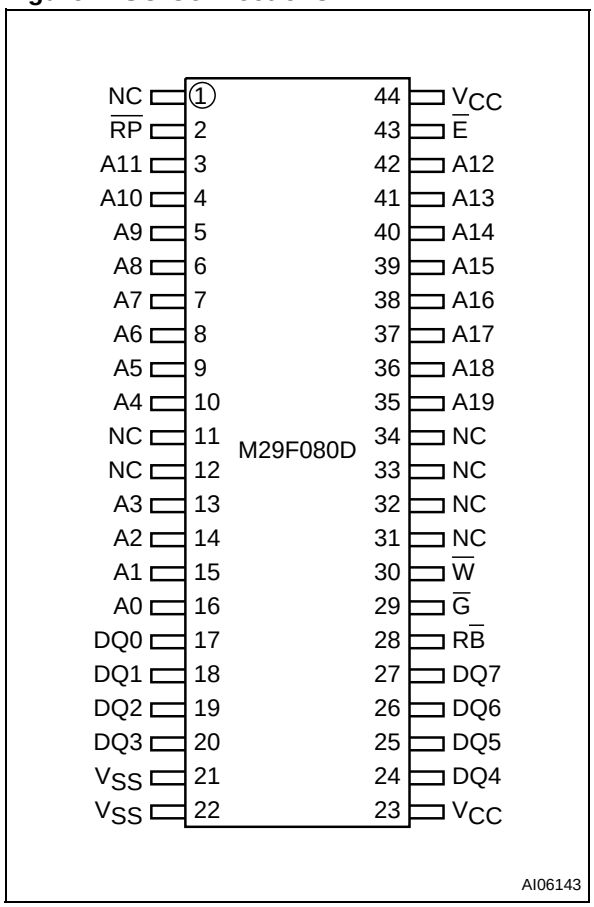
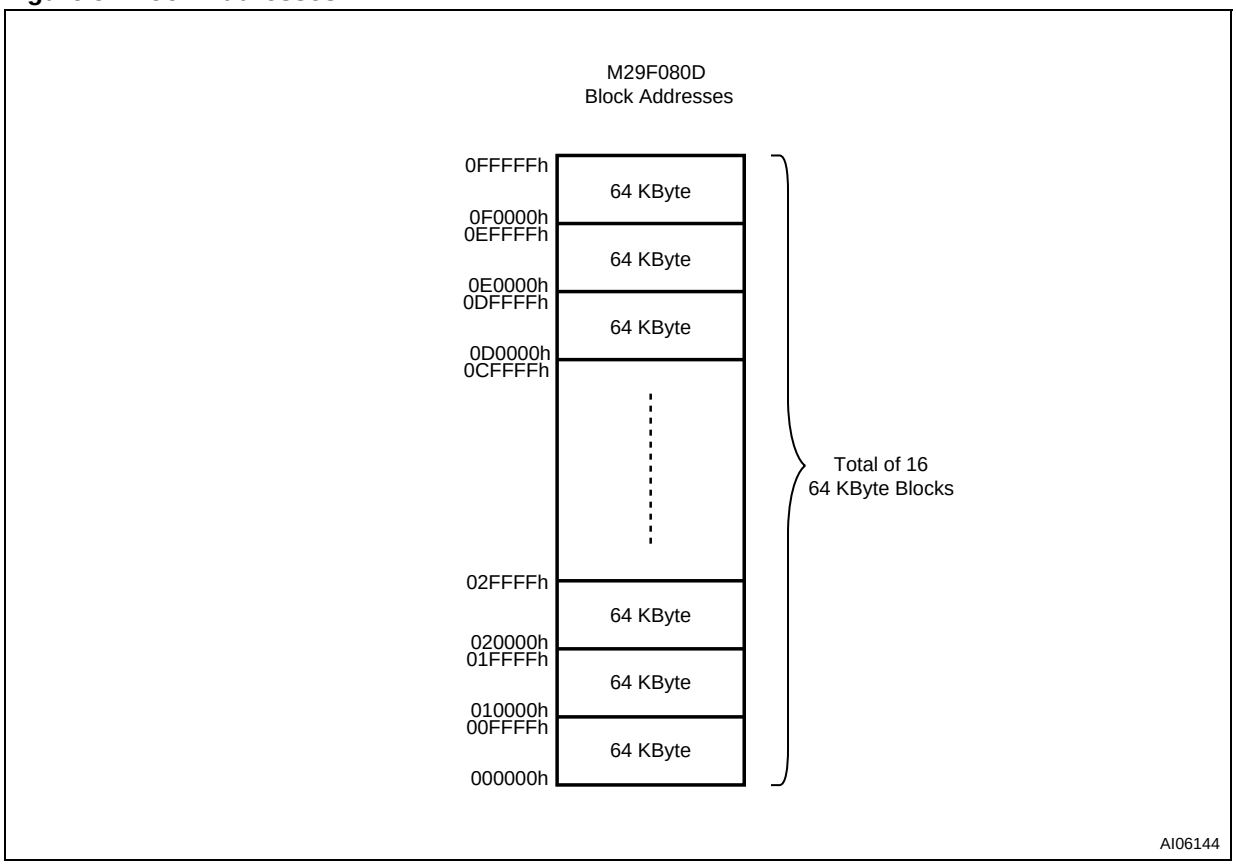


Figure 5. Block Addresses



Note: Also see Appendix A, Table 16 for a full listing of the Block Addresses.

SIGNAL DESCRIPTIONS

See Figure 2, Logic Diagram, and Table 1, Signal Names, for a brief overview of the signals connected to this device.

Address Inputs (A0-A19). The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the internal state machine.

Data Inputs/Outputs (DQ0-DQ7). The Data I/O outputs the data stored at the selected address during a Bus Read operation. During Bus Write operations they represent the commands sent to the Command Interface of the internal state machine.

Chip Enable ($\overline{E}$). The Chip Enable, $\overline{E}$, activates the memory, allowing Bus Read and Bus Write operations to be performed. When Chip Enable is High, V_{IH}, all other pins are ignored.

Output Enable ($\overline{G}$). The Output Enable, $\overline{G}$, controls the Bus Read operation of the memory.

Write Enable ($\overline{W}$). The Write Enable, $\overline{W}$, controls the Bus Write operation of the memory's Command Interface.

Reset/Block Temporary Unprotect (RP). The Reset/Block Temporary Unprotect pin can be used to apply a Hardware Reset to the memory or to temporarily unprotect all Blocks that have been protected.

A Hardware Reset is achieved by holding Reset/Block Temporary Unprotect Low, V_{IL}, for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, the memory will be ready for Bus Read and Bus Write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See the Ready/Busy Output section, Table 13 and Figure 13, Reset/Temporary Unprotect AC Characteristics for more details.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the protected Blocks in the memory. Program and Erase operations on all blocks will be possible. The transition from V_{IH} to V_{ID} must be slower than t_{PHPHH}.

Ready/Busy Output ($\overline{RB}$). The Ready/Busy pin is an open-drain output that can be used to identify when the device is performing a Program or Erase operation. During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy is high-impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high-impedance. See Table 13 and Figure 13, Reset/Temporary Unprotect AC Characteristics.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

V_{CC} Supply Voltage (5V). V_{CC} provides the power supply for all operations (Read, Program and Erase).

The Command Interface is disabled when the V_{CC} Supply Voltage is less than the Lockout Voltage, V_{LKO}. This prevents Bus Write operations from accidentally damaging the data during power up, power down and power surges. If the Program/Erase Controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply, see Figure 10, AC Measurement Load Circuit. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC3}.

V_{SS} Ground. V_{SS} is the reference for all voltage measurements.

BUS OPERATIONS

There are five standard bus operations that control the device. These are Bus Read, Bus Write, Output Disable, Standby and Automatic Standby. See Tables 2, Bus Operations, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect bus operations.

Bus Read. Bus Read operations read from the memory cells, or specific registers in the Command Interface. A valid Bus Read operation involves setting the desired address on the Address Inputs, applying a Low signal, V_{IL}, to Chip Enable and Output Enable and keeping Write Enable High, V_{IH}. The Data Inputs/Outputs will output the value, see Figure 10, Read Mode AC Waveforms, and Table 10, Read AC Characteristics, for details of when the output becomes valid.

Bus Write. Bus Write operations write to the Command Interface. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation. See Figures 11 and 12, Write AC Waveforms, and Tables 11 and 12, Write AC Characteristics, for details of the timing requirements.

Output Disable. The Data Inputs/Outputs are in the high impedance state when Output Enable is High, V_{IH}.

Standby. When Chip Enable is High, V_{IH}, the memory enters Standby mode and the Data Inputs/Outputs pins are placed in the high-impedance state. To reduce the Supply Current to the Standby Supply Current, I_{CC2}, Chip Enable should be held within $V_{CC} \pm 0.2V$. For the Standby current level see Table 9, DC Characteristics.

During program or erase operations the memory will continue to use the Program/Erase Supply Current, I_{CC3}, for Program or Erase operations until the operation completes.

Automatic Standby. If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and the bus is inactive for 300ns or more the memory enters Automatic Standby where the internal Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Data Inputs/Outputs will still output data if a Bus Read operation is in progress.

Special Bus Operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

Electronic Signature. The memory has two codes, the manufacturer code and the device code, that can be read to identify the memory. These codes can be read by applying the signals listed in Tables 2, Bus Operations.

Block Protection and Blocks Unprotection.

Blocks can be protected in groups of 4 against accidental Program or Erase. See Appendix A, Table 16, Block Addresses, for details of which blocks must be protected together as a group. Protected blocks can be unprotected to allow data to be changed.

There are two methods available for protecting and unprotecting the blocks, one for use on programming equipment and the other for in-system use. Block Protect and Chip Unprotect operations are described in Appendix C.

Table 2. Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A19	Data Inputs/Outputs DQ7-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	Cell Address	Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	Command Address	Data Input
Output Disable	X	V_{IH}	V_{IH}	X	Hi-Z
Standby	V_{IH}	X	X	X	Hi-Z
Read Manufacturer Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	20h
Read Device Code	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IH}, A1 = V_{IL}, A9 = V_{ID}, Others V_{IL} or V_{IH}	F1h

Note: X = V_{IL} or V_{IH}.

COMMAND INTERFACE

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security.

Refer to Table 3, Commands, in conjunction with the following text descriptions.

Read/Reset Command. The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset Command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. Once the program or erase operation has started the Read/Reset command is no longer accepted. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

Auto Select Command. The Auto Select command is used to read the Manufacturer Code, the Device Code and the Block Protection Status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until a Read/Reset command is issued. Read CFI Query and Read/Reset commands are accepted in Auto Select mode, all other commands are ignored.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = V_{IL} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Manufacturer Code for STMicroelectronics is 20h.

The Device Code can be read using a Bus Read operation with A0 = V_{IH} and A1 = V_{IL}. The other address bits may be set to either V_{IL} or V_{IH}. The Device Code for the M29F080D F1h.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = V_{IL}, A1 = V_{IH}, and A12-A19 specifying the address of the block. The other address bits may be set to either V_{IL} or V_{IH}. If the addressed block is protected then 01h is output on Data Inputs/Outputs DQ0-DQ7, otherwise 00h is output.

Program Command. The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in Table 4. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Unlock Bypass Command. The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the cycle time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

Unlock Bypass Program Command. The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two Bus Write operations, the final write operation latches the address and data in the internal state machine and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. A protected block cannot be programmed; the operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass Mode. See the Program command for details on the behavior.

Unlock Bypass Reset Command. The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset

command does not exit from Unlock Bypass Mode.

Chip Erase Command. The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in Table 4. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to '1'. All previous data is lost.

Block Erase Command. The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller about 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register section for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command. Typical block erase times are given in Table 4. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Block Erase Command sets all of the bits in the unprotected selected blocks to '1'. All previous data in the selected blocks is lost.

Erase Suspend Command. The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within 15µs of the Erase Suspend Command being issued. Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, Read CFI Query and Unlock Bypass commands during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

Erase Resume Command. The Erase Resume command must be used to restart the Program/Erase Controller after an Erase Suspend. The device must be in Read Array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

Read CFI Query Command. The Read CFI Query Command is used to read data from the Common Flash Interface (CFI) Memory Area. This command is valid when the device is in the Read Array mode, or when the device is in Autoselected mode.

One Bus Write cycle is required to issue the Read CFI Query Command. Once the command is issued subsequent Bus Read operations read from the Common Flash Interface Memory Area.

The Read/Reset command must be issued to return the device to the previous mode (the Read Array mode or Autoselected mode). A second Read/Reset command would be needed if the device is to be put in the Read Array mode from Autoselected mode.

See Appendix B, Tables 17, 18, 19, 20, 21 and 22 for details on the information contained in the Common Flash Interface (CFI) memory area.

Block Protect and Chip Unprotect Commands. Groups of blocks can be protected against accidental Program or Erase. The Protection Groups are shown in Appendix A, Table 16. The whole chip can be unprotected to allow the data inside the blocks to be changed.

Block Protect and Chip Unprotect operations are described in Appendix C.

Table 3. Commands

Command	Length	Bus Write Operations											
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read/Reset	1	X	F0										
	3	555	AA	2AA	55	X	F0						
Auto Select	3	555	AA	2AA	55	555	90						
Program	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass	3	555	AA	2AA	55	555	20						
Unlock Bypass Program	2	X	A0	PA	PD								
Unlock Bypass Reset	2	X	90	X	00								
Chip Erase	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase	6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BA	30
Erase Suspend	1	X	B0										
Erase Resume	1	X	30										
Read CFI Query	1	55	98										

Note: X Don't Care, PA Program Address, PD Program Data, BA Any address in the Block. All values in the table are in hexadecimal.

Table 4. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	Min	Typ (1)	Typical after 100k W/E Cycles (1)	Max	Unit
Chip Erase		12	12	60	s
Block Erase (64 Kbytes)		0.8		6	s
Program (Byte)		10		200	µs
Chip Program (Byte by Byte)		12		60	s
Program/Erase Cycles (per Block)	100,000				cycles

Note: 1. T_A = 25°C, V_{CC} = 5V.

STATUS REGISTER

Bus Read operations from any address always read the Status Register during Program and Erase operations. It is also read during Erase Suspend when an address within a block being erased is accessed.

The bits in the Status Register are summarized in Table 5, Status Register Bits.

Data Polling Bit (DQ7). The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs '0', the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a '1' during a Bus Read operation within a block being erased. The Data Polling Bit will change from a '0' to a '1' when the Program/Erase Controller has suspended the Erase operation.

Figure 6, Data Polling Flowchart, gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

Toggle Bit (DQ6). The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

If any attempt is made to erase a protected block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 100µs. If any attempt is made to program a protected block or a suspended block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 1µs.

Figure 7, Data Toggle Flowchart, gives an example of how to use the Data Toggle Bit.

Error Bit (DQ5). The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to '1' when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to '0' back to '1' and attempting to do so will set DQ5 to '1'. A Bus Read operation to that address will show the bit is still '0'. One of the Erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

Erase Timer Bit (DQ3). The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to '1'. Before the Program/Erase Controller starts the Erase Timer Bit is set to '0' and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.

Alternative Toggle Bit (DQ2). The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from '0' to '1' to '0', etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from '0' to '1' to '0', etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Table 5. Status Register Bits

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	RB
Program	Any Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program During Erase Suspend	Any Address	$\overline{DQ7}$	Toggle	0	–	–	0
Program Error	Any Address	$\overline{DQ7}$	Toggle	1	–	–	0
Chip Erase	Any Address	0	Toggle	0	1	Toggle	0
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle	0
	Non-Erasing Block	0	Toggle	0	0	No Toggle	0
Block Erase	Erasing Block	0	Toggle	0	1	Toggle	0
	Non-Erasing Block	0	Toggle	0	1	No Toggle	0
Erase Suspend	Erasing Block	1	No Toggle	0	–	Toggle	1
	Non-Erasing Block	Data read as normal					1
Erase Error	Good Block Address	0	Toggle	1	1	No Toggle	0
	Faulty Block Address	0	Toggle	1	1	Toggle	0

Note: Unspecified data bits should be ignored.

Figure 6. Data Polling Flowchart

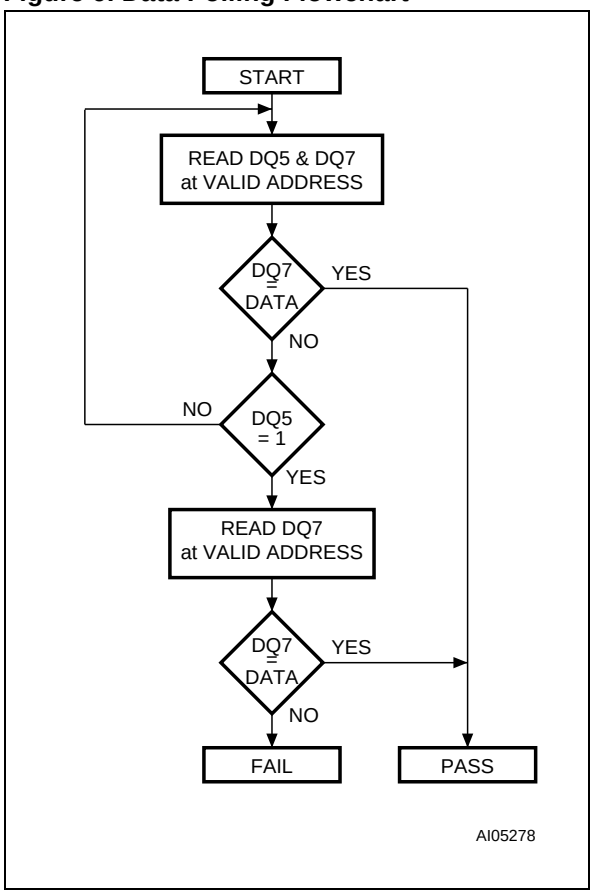
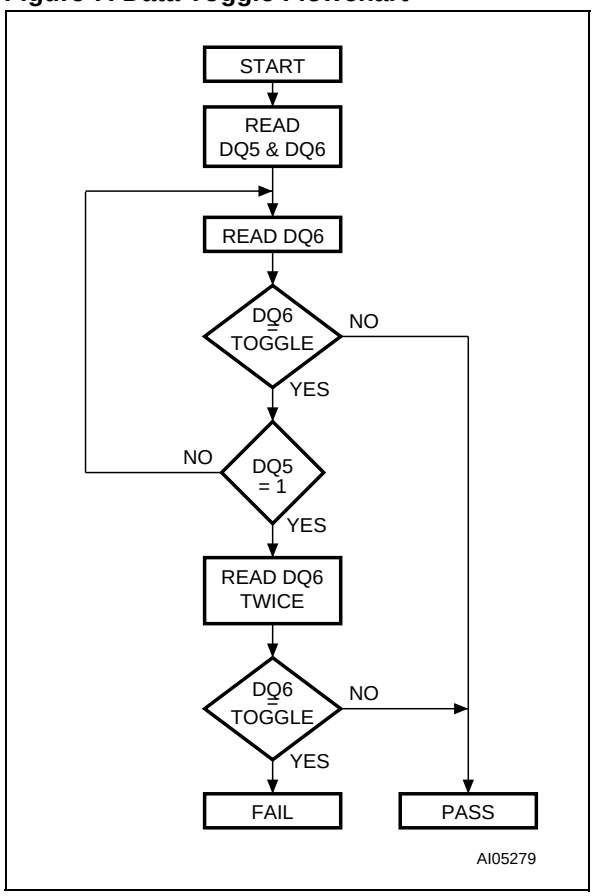


Figure 7. Data Toggle Flowchart



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature Under Bias	–50	125	°C
T_{STG}	Storage Temperature	–65	150	°C
V_{IO}	Input or Output Voltage (1)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply Voltage	–0.6	6	V
V_{ID}	Identification Voltage	–0.6	13.5	V

Note: 1. Minimum Voltage may undershoot to –2V or overshoot to V_{CC} +2V during transition for a maximum of 20ns.

DC AND AC PARAMETERS

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in Table 7, Operating and AC Measurement Conditions. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 7. Operating and AC Measurement Conditions

Parameter	M29F080D				Unit
	55		70/ 90		
	Min	Max	Min	Max	
V_{CC} Supply Voltage	4.5	5.5	4.5	5.5	V
Ambient Operating Temperature	– 40	85	– 40	85	°C
Load Capacitance (C_L)	30		100		pF
Input Rise and Fall Times		10		10	ns
Input Pulse Voltages	0 to 3		0.45 to 2.4		V
Input and Output Timing Ref. Voltages	1.5		0.8 and 2.0		V

Figure 8. AC Measurement I/O Waveform

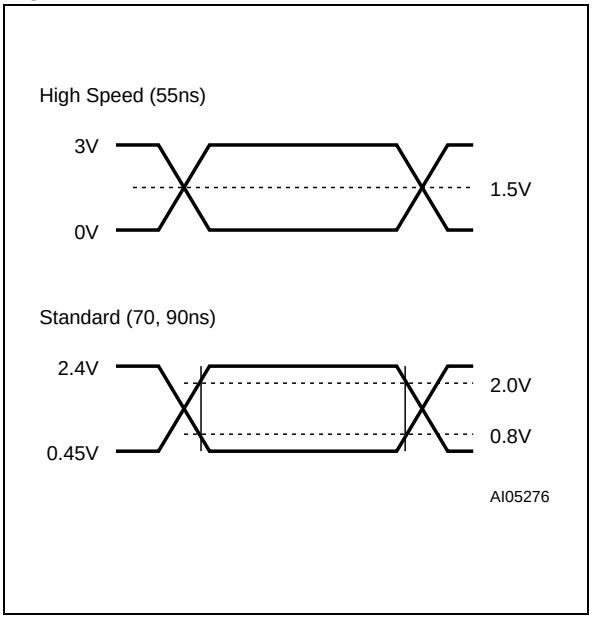


Figure 9. AC Measurement Load Circuit

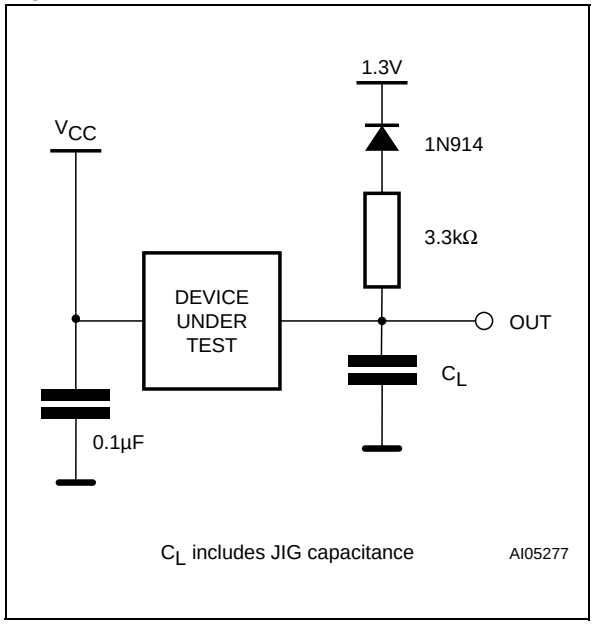


Table 8. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 9. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		20	mA
I_{CC2}	Supply Current (Standby) TTL	$\overline{E} = V_{IH}$		2	mA
I_{CC3}	Supply Current (Standby) CMOS	$\overline{E} = V_{CC} \pm 0.2V$, $\overline{RP} = V_{CC} \pm 0.2V$		150	µA
I_{CC4} (1)	Supply Current (Program/Erase)	Program/Erase Controller active		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		2	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 5.8mA		0.45	V
V_{OH}	Output High Voltage TTL	I_{OH} = –2.5mA	2.4		V
	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} – 0.4		V
V_{ID}	Identification Voltage		11.5	12.5	V
I_{ID}	Identification Current	$A9 = V_{ID}$		100	µA
V_{LKO} (1)	Program/Erase Lockout Supply Voltage		3.2	4.2	V

Note: 1. Sampled only, not 100% tested.

Figure 10. Read AC Waveforms

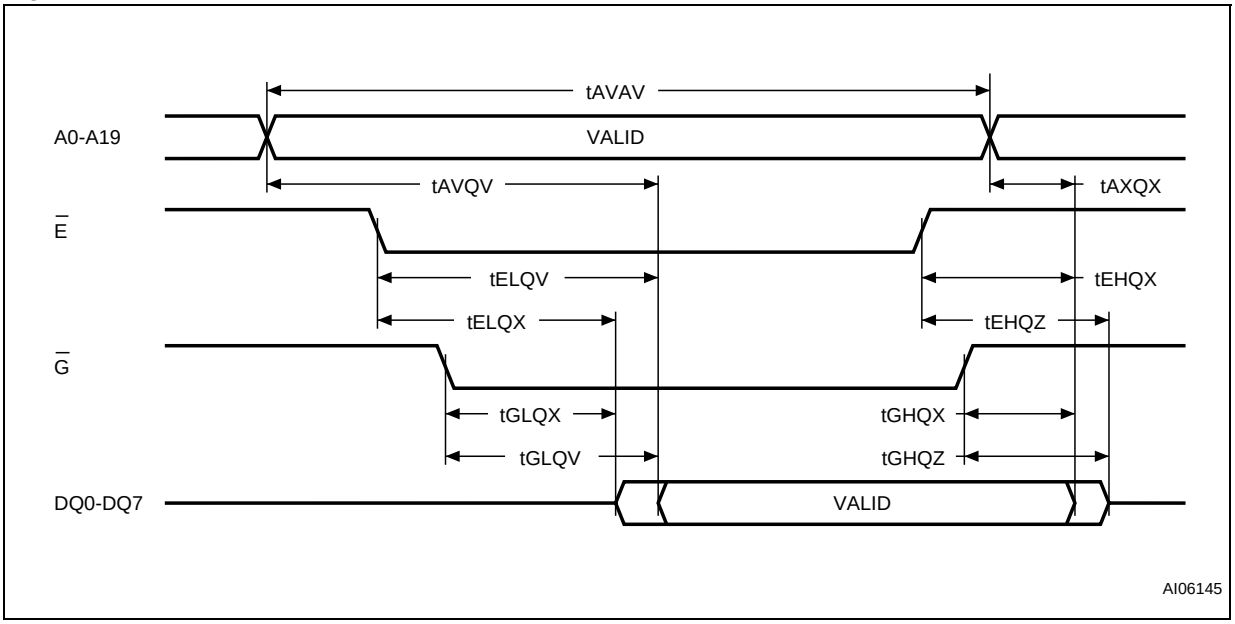


Table 10. Read AC Characteristics

Symbol	Alt	Parameter	Test Condition		M29F080D		Unit
					55	70/ 90	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	55	70	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	55	70	ns
t_{ELQX} (1)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQV}	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	55	70	ns
t_{GLQX} (1)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	30	30	ns
t_{EHQZ} (1)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	18	20	ns
t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	18	20	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns

Note: 1. Sampled only, not 100% tested.

Figure 11. Write AC Waveforms, Write Enable Controlled

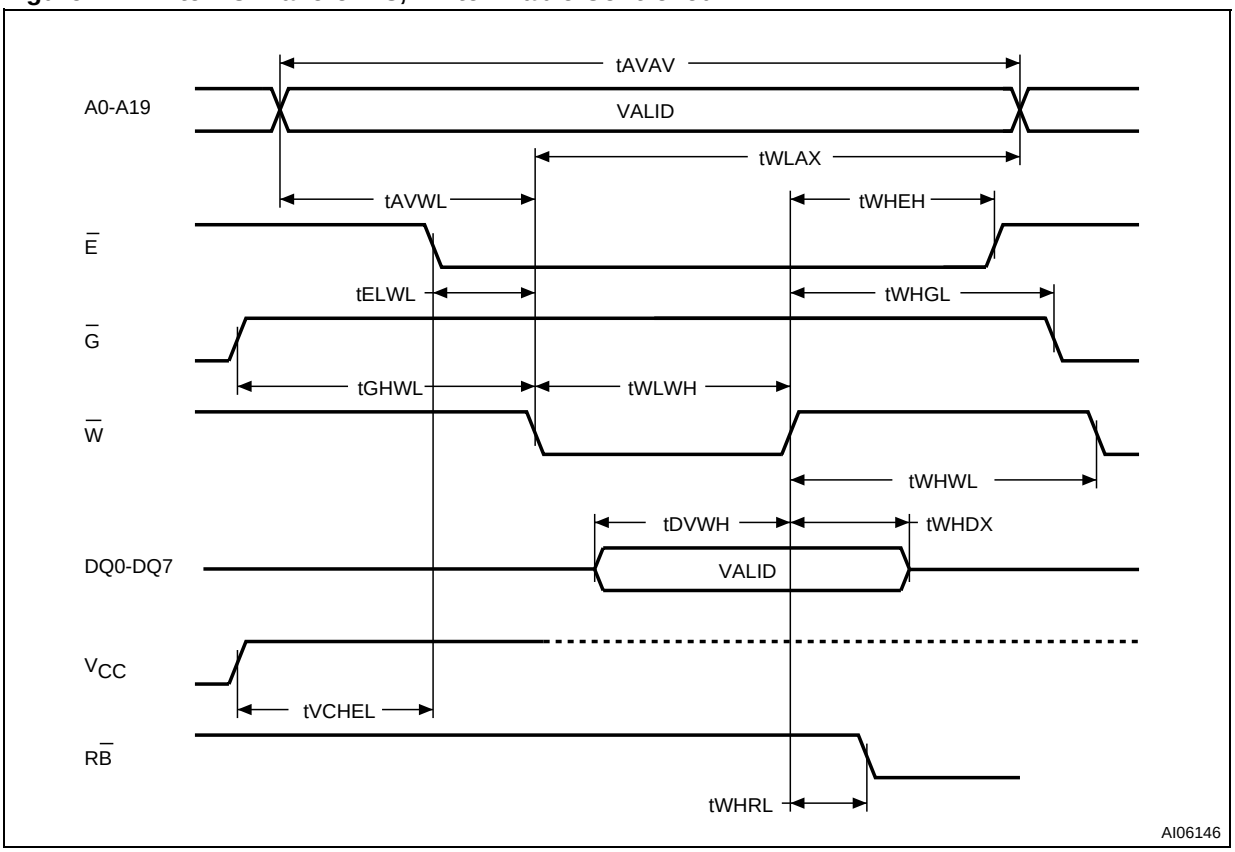


Table 11. Write AC Characteristics, Write Enable Controlled

Symbol	Alt	Parameter		M29F080D		Unit
				55	70/ 90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	55	70	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	45	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	20	20	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{WHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs

Note: 1. Sampled only, not 100% tested.

Figure 12. Write AC Waveforms, Chip Enable Controlled

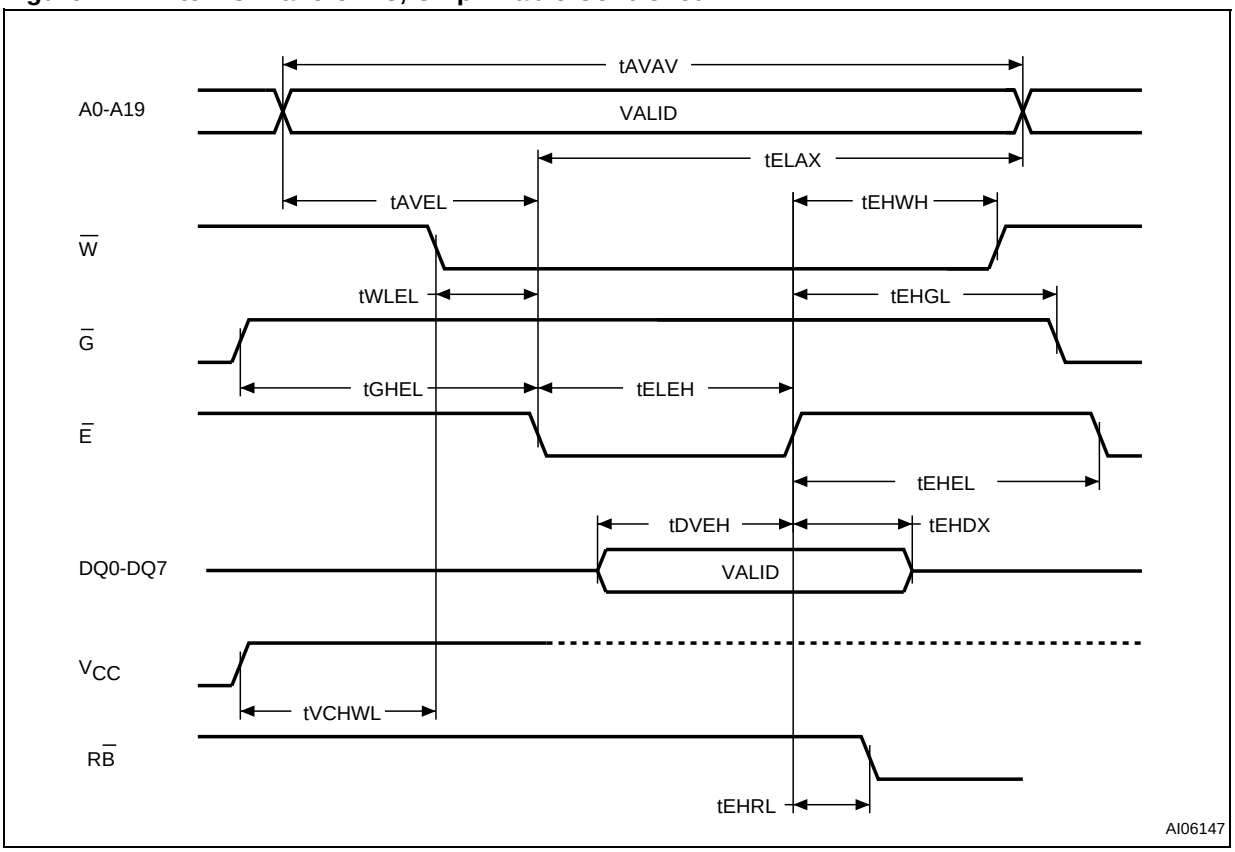


Table 12. Write AC Characteristics, Chip Enable Controlled

Symbol	Alt	Parameter		M29F080D		Unit
				55	70/ 90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	55	70	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	45	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	45	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	20	20	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{EHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs

Note: 1. Sampled only, not 100% tested.

Figure 13. Reset/Block Temporary Unprotect AC Waveforms

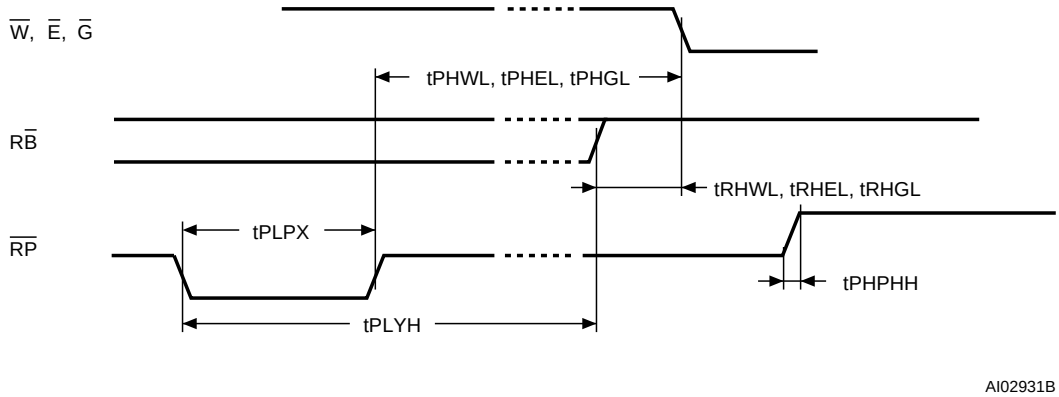


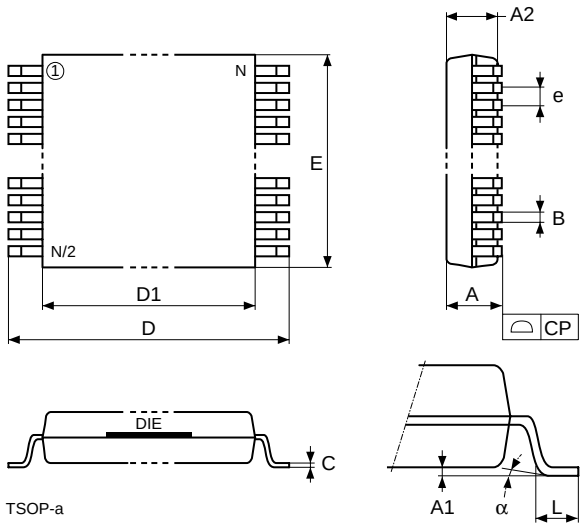
Table 13. Reset/Block Temporary Unprotect AC Characteristics

Symbol	Alt	Parameter		M29F080D		Unit
				55	70/ 90	
t_{PHWL} (1) t_{PHEL} t_{PHGL} (1)	t_{RH}	RP High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	ns
t_{RHWL} (1) t_{RHEL} (1) t_{RHGL} (1)	t_{RB}	RB High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	ns
t_{PLPX}	t_{RP}	RP Pulse Width	Min	500	500	ns
t_{PLYH} (1)	t_{READY}	RP Low to Read Mode	Max	10	10	µs
t_{PHPHH} (1)	t_{VIDR}	RP Rise Time to V_{ID}	Min	500	500	ns

Note: 1. Sampled only, not 100% tested.

PACKAGE MECHANICAL

TSOP40 – 40 lead Plastic Thin Small Outline, 10 x 20mm, Package Outline

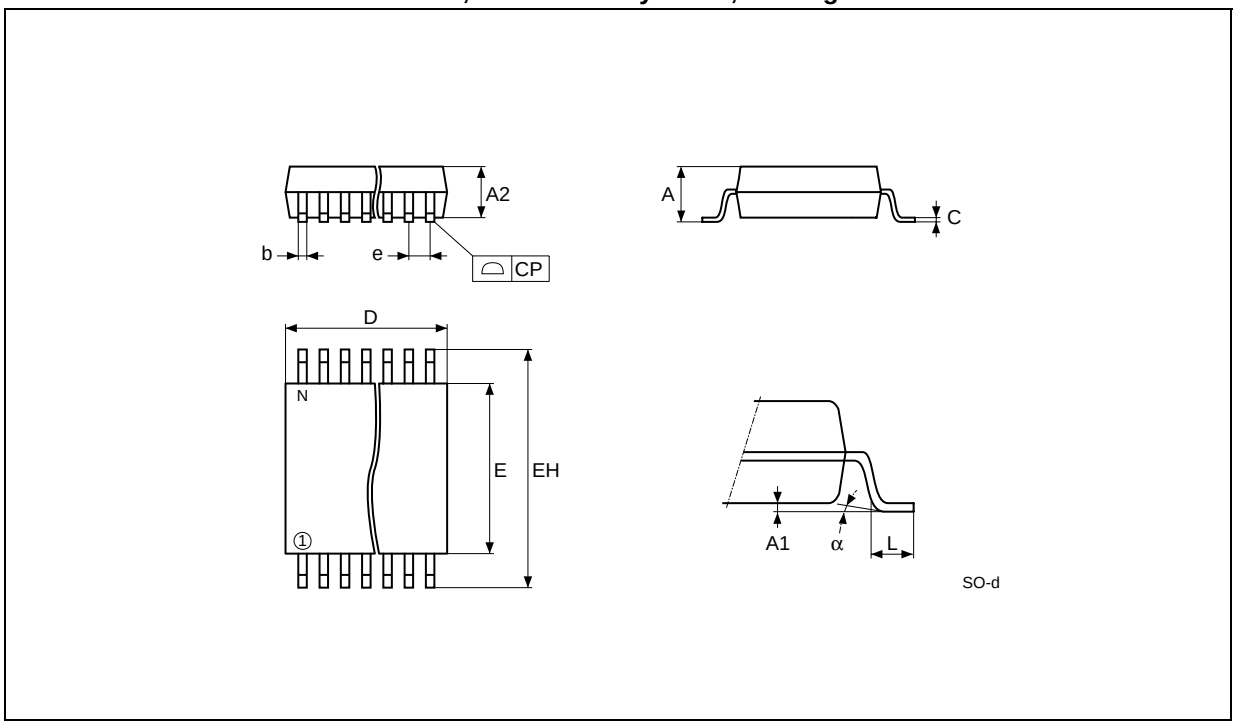


Note: Drawing is not to scale.

TSOP40 – 40 lead Plastic Thin Small Outline, 10 x 20mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.050	0.150		0.0020	0.0059
A2		0.950	1.050		0.0374	0.0413
B		0.170	0.270		0.0067	0.0106
C		0.100	0.210		0.0039	0.0083
D		19.800	20.200		0.7795	0.7953
D1		18.300	18.500		0.7205	0.7283
E		9.900	10.100		0.3898	0.3976
e	0.500	–	–	0.0197	–	–
L		0.500	0.700		0.0197	0.0276
α		0°	5°		0°	5°
N	40			40		
CP			0.100			0.0039

SO44 – 44 lead Plastic Small Outline, 525 mils body width, Package Outline



Note: Drawing is not to scale.

SO44 – 44 lead Plastic Small Outline, 525 mils body width, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			2.80			0.1102
A1		0.10			0.0039	
A2	2.30	2.20	2.40	0.0906	0.0866	0.0945
b	0.40	0.35	0.50	0.0157	0.0138	0.0197
C	0.15	0.10	0.20	0.0059	0.0039	0.0079
CP			0.08			0.0030
E	13.30	13.20	13.50	0.5236	0.5197	0.5315
D	28.20	28.00	28.40	1.1102	1.1024	1.1181
e	1.27	–	–	0.0500	–	–
HE	16.00	15.75	16.25	0.6299	0.6201	0.6398
L	0.80			0.0315		
N		44			44	
α			8			8

PART NUMBERING

Table 14. Ordering Information Scheme

Example: M29F080D 55 N 1 T

Device Type
M29

Operating Voltage
F = V_{CC} = 5V ± 10%

Device Function
080D = 8 Mbit (1Mb x8), Uniform Block

Speed
55 = 55 ns
70 = 70 ns
90 = 90 ns

Package
N = TSOP40: 10 x 20 mm
M = SO44

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
T = Tape & Reel Packing

Devices are shipped from the factory with the memory content bits erased to '1'.

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

REVISION HISTORY

Table 15. Document Revision History

Date	Version	Revision Details
03-Dec-2001	-01	First Issue
05-Apr-2002	-02	Description of Ready/Busy signal clarified (and Figure 13 modified) Clarified allowable commands during block erase Clarified the mode the device returns to in the CFI Read Query command section

APPENDIX A. BLOCK ADDRESS TABLE

Table 16. Block Addresses, M29F080D

#	Size, KByte	Address Range	Protection Group
15	64	0F0000h-0FFFFFh	3
14	64	0E0000h-0EFFFFh	
13	64	0D0000h-0DFFFFh	
12	64	0C0000h-0CFFFFh	
11	64	0B0000h-0BFFFFh	2
10	64	0A0000h-0AFFFFh	
9	64	090000h-09FFFFh	
8	64	080000h-08FFFFh	
7	64	070000h-07FFFFh	1
6	64	060000h-06FFFFh	
5	64	050000h-05FFFFh	
4	64	040000h-04FFFFh	
3	64	030000h-03FFFFh	0
2	64	020000h-02FFFFh	
1	64	010000h-01FFFFh	
0	64	000000h-00FFFFh	

APPENDIX B. COMMON FLASH INTERFACE (CFI)

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. Tables 17, 18, 19, 20, 21 and 22 show the addresses used to retrieve the data.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see Table 22, Security Code area). This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST. Issue a Read command to return to Read mode.

Table 17. Query Structure Overview

Address	Sub-section Name	Description
10h	CFI Query Identification String	Command set ID and algorithm data offset
1Bh	System Interface Information	Device timing & voltage information
27h	Device Geometry Definition	Flash device layout
40h	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
61h	Security Code Area	64 bit unique device number

Note: Query data are always presented on the lowest order data outputs.

Table 18. CFI Query Identification String

Address	Data	Description	Value
10h	51h	Query Unique ASCII String "QRY"	"Q"
11h	52h		"R"
12h	59h		"Y"
13h	02h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm	AMD Compatible
14h	00h		
15h	40h	Address for Primary Algorithm extended Query table (see Table 20)	P = 40h
16h	00h		
17h	00h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported	NA
18h	00h		
19h	00h	Address for Alternate Algorithm extended Query table	NA
1Ah	00h		

Table 19. CFI Query System Interface Information

Address	Data	Description	Value
1Bh	45h	V_{CC} Logic Supply Minimum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	4.5V
1Ch	55h	V_{CC} Logic Supply Maximum Program/Erase voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 mV	5.5V
1Dh	00h	V_{PP} [Programming] Supply Minimum Program/Erase voltage 00h not supported	NA
1Eh	00h	V_{PP} [Programming] Supply Maximum Program/Erase voltage 00h not supported	NA
1Fh	04h	Typical timeout per single byte program = 2^n µs	16µs
20h	00h	Typical timeout for minimum size write buffer program = 2^n µs	NA
21h	0Ah	Typical timeout per individual block erase = 2^n ms	1s
22h	00h	Typical timeout for full chip erase = 2^n ms	see note (1)
23h	04h	Maximum timeout for byte program = 2^n times typical	256µs
24h	00h	Maximum timeout for write buffer program = 2^n times typical	NA
25h	03h	Maximum timeout per individual block erase = 2^n times typical	8s
26h	00h	Maximum timeout for chip erase = 2^n times typical	see note (1)

Note: 1. Not supported in the CFI

Table 20. Device Geometry Definition

Address	Data	Description	Value
27h	14h	Device Size = 2^n in number of bytes	1 MByte
28h 29h	00h 00h	Flash Device Interface Code description	x8 only Async.
2Ah 2Bh	00h 00h	Maximum number of bytes in multi-byte program or page = 2^n	NA
2Ch	01h	Number of Erase Block Regions within the device. It specifies the number of regions within the device containing contiguous Erase Blocks of the same size.	1
2Dh 2Eh	0Fh 00h	Region 1 Information Number of identical size erase block = 000Fh+1	16
2Fh 30h	00h 01h	Region 1 Information Block size in Region 1 = 0100h * 256 byte	64 Kbyte

Table 21. Primary Algorithm-Specific Extended Query Table

Address	Data	Description	Value
40h	50h	Primary Algorithm extended Query table unique ASCII string “PRI”	"P"
41h	52h		"R"
42h	49h		"I"
43h	31h	Major version number, ASCII	"1"
44h	30h	Minor version number, ASCII	"0"
45h	00h	Address Sensitive Unlock (bits 1 to 0) 00 = required, 01= not required Silicon Revision Number (bits 7 to 2)	Yes
46h	02h	Erase Suspend 00 = not supported, 01 = Read only, 02 = Read and Write	2
47h	04h	Block Protection 00 = not supported, x = number of blocks per group	4
48h	01h	Temporary Block Unprotect 00 = not supported, 01 = supported	yes
49h	04h	Block Protect /Unprotect 04 = M29W400B mode	4
4Ah	00h	Simultaneous Operations, 00 = not supported	No
4Bh	00h	Burst Mode, 00 = not supported, 01 = supported	No
4Ch	00h	Page Mode, 00 = not supported, 01 = 4 page word, 02 = 8 page word	No

Table 22. Security Code Area

Address	Data	Description
61h	XX	64 bit: unique device number
62h	XX	
63h	XX	
64h	XX	
65h	XX	
66h	XX	
67h	XX	
68h	XX	

APPENDIX C. BLOCK PROTECTION

Block protection can be used to prevent any operation from modifying the data stored in the memory. The blocks are protected in groups, refer to Appendix A, Table 16 for details of the Protection Groups. Once protected, Program and Erase operations within the protected group fail to change the data.

There are three techniques that can be used to control Block Protection, these are the Programmer technique, the In-System technique and Temporary Unprotection. Temporary Unprotection is controlled by the Reset/Block Temporary Unprotection pin, $\overline{RP}$; this is described in the Signal Descriptions section.

To protect the Extended Block issue the Enter Extended Block command and then use either the Programmer or In-System technique. Once protected issue the Exit Extended Block command to return to read mode. The Extended Block protection is irreversible, once protected the protection cannot be undone.

Programmer Technique

The Programmer technique uses high (V_{ID}) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a group of blocks follow the flowchart in Figure 14, Programmer Equipment Block Protect Flowchart. To unprotect the whole chip it is necessary to protect all of the groups first, then all groups can be unprotected at the same time. To unprotect the chip follow Figure 15, Programmer Equipment Chip Unprotect Flowchart. Table 23, Programmer Technique Bus Operations, gives a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

In-System Technique

The In-System technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, $\overline{RP}$. This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the memory has been fitted to the system.

To protect a group of blocks follow the flowchart in Figure 16, In-System Block Protect Flowchart. To unprotect the whole chip it is necessary to protect all of the groups first, then all the groups can be unprotected at the same time. To unprotect the chip follow Figure 17, In-System Chip Unprotect Flowchart.

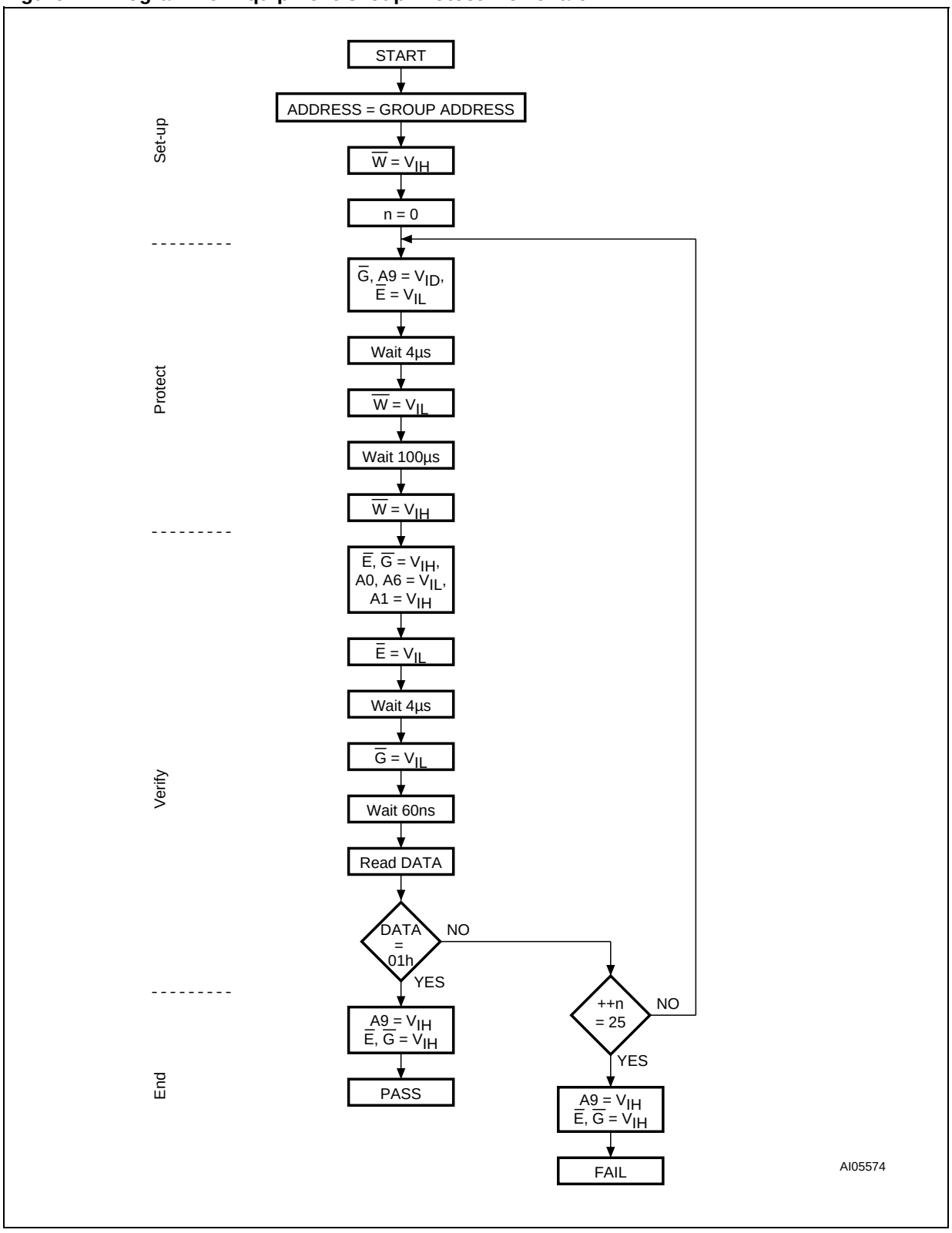
The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

Table 23. Programmer Technique Bus Operations, $\overline{BYTE}$ = V_{IH} or V_{IL}

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A19	Data Inputs/Outputs DQ15A–1, DQ14-DQ0
Block (Group) Protect(1)	V_{IL}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12-A19 Block Address Others = X	X
Chip Unprotect	V_{ID}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A12 = V_{IH}, A15 = V_{IH} Others = X	X
Block (Group) Protection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, A12-A19 Block Address Others = X	Pass = XX01h Retry = XX00h
Block (Group) Unprotection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IH}, A9 = V_{ID}, A12-A19 Block Address Others = X	Retry = XX01h Pass = XX00h

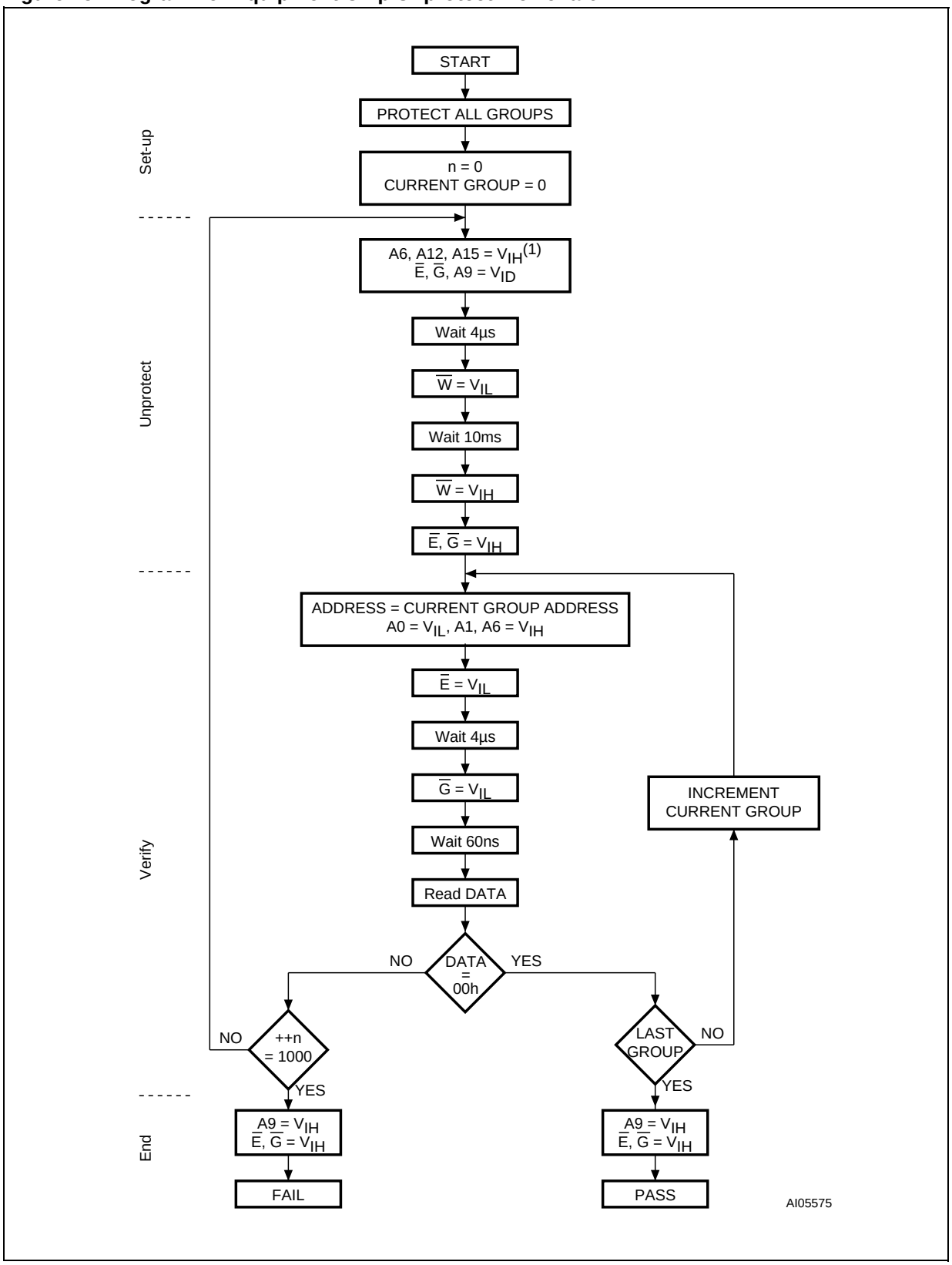
Note: 1. Block Protection Groups are shown in Appendix A, Table 16.

Figure 14. Programmer Equipment Group Protect Flowchart



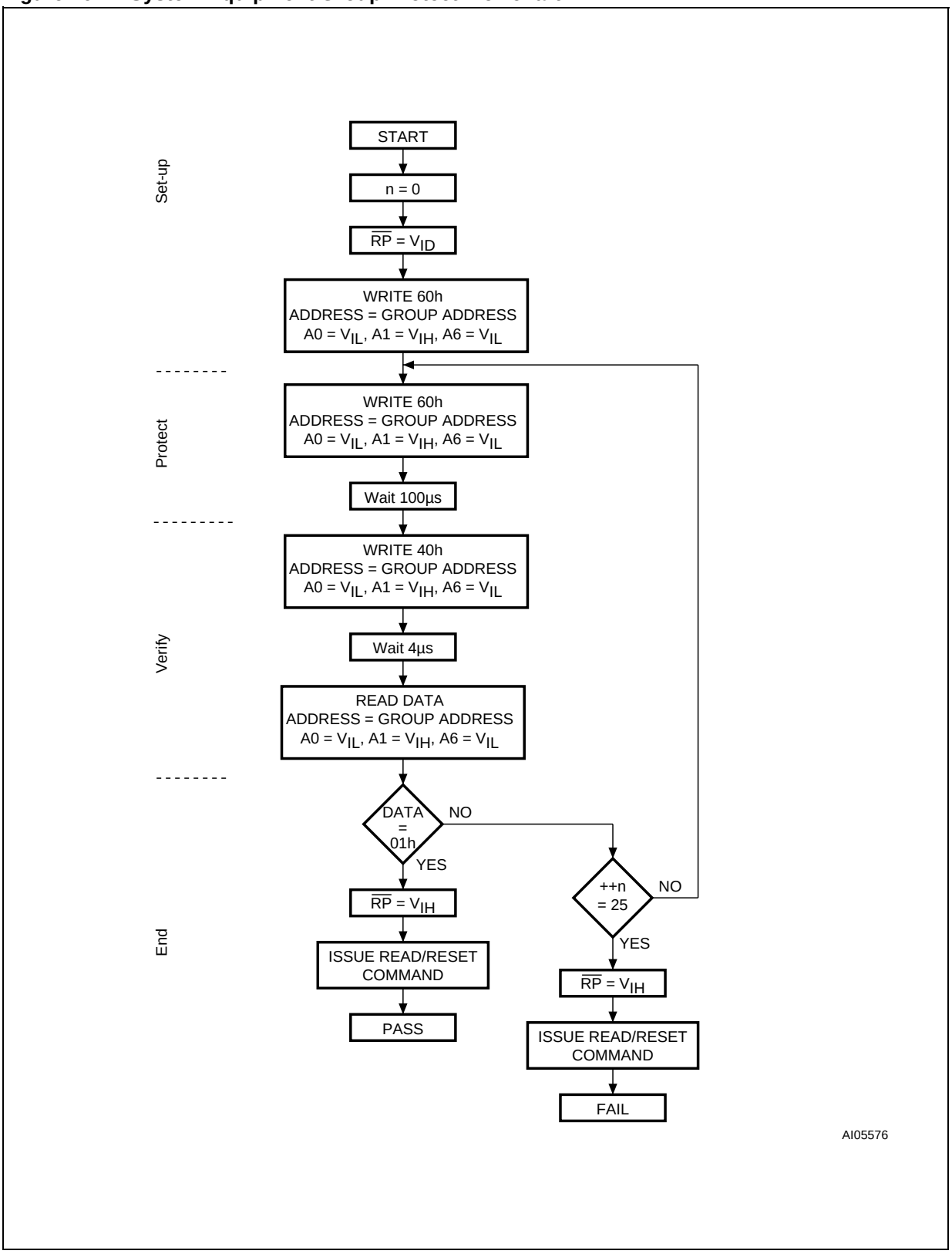
Note: Block Protection Groups are shown in Appendix A, Table 16.

Figure 15. Programmer Equipment Chip Unprotect Flowchart



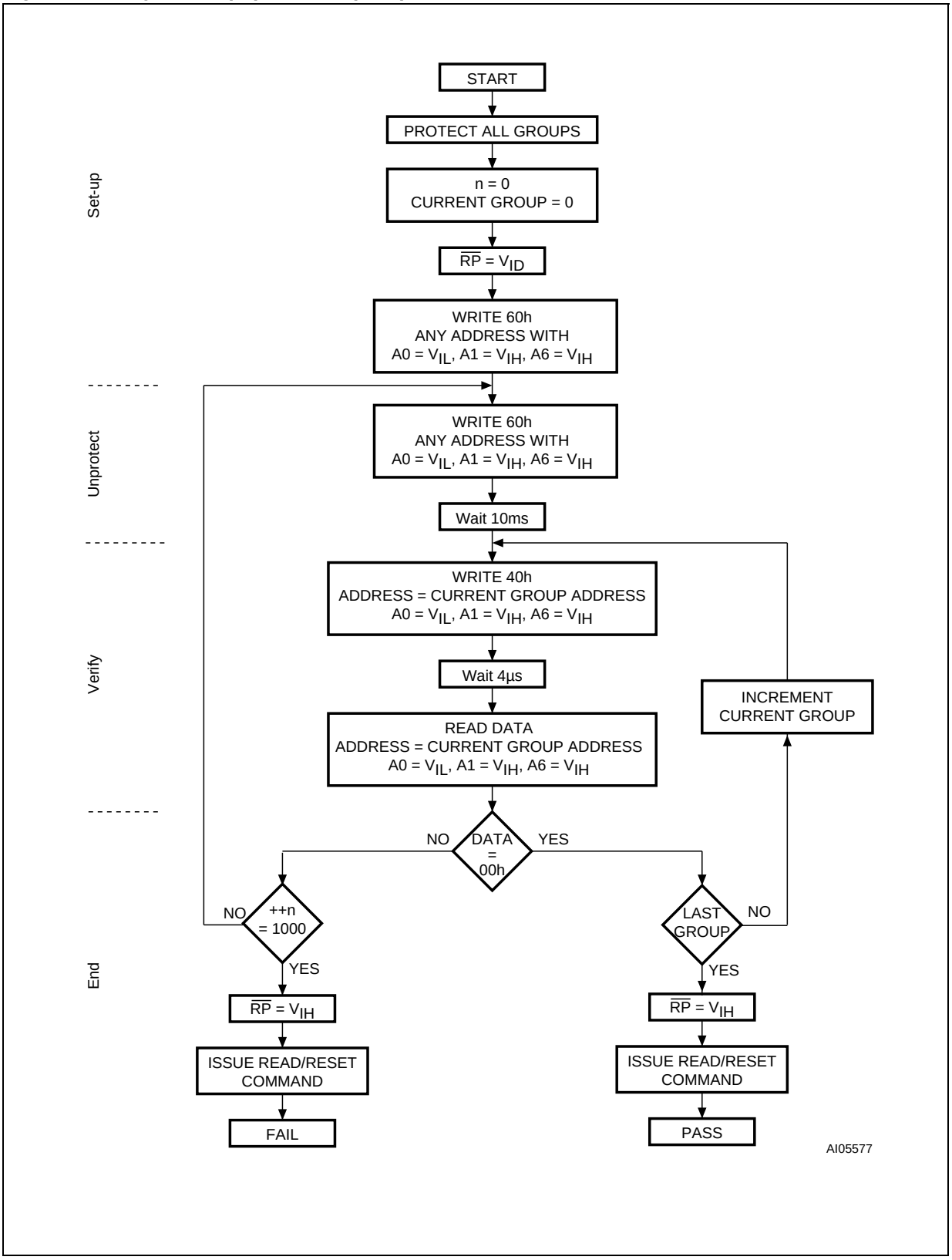
Note: Block Protection Groups are shown in Appendix A, Table 16.

Figure 16. In-System Equipment Group Protect Flowchart



Note: Block Protection Groups are shown in Appendix A, Table 16.

Figure 17. In-System Equipment Chip Unprotect Flowchart



Note: Block Protection Groups are shown in Appendix A, Table 16.