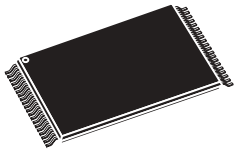
M29W008ET
M29W008EB

8 Mbit (1Mb x 8, Boot Block)
3V Supply Flash Memory

FEATURES SUMMARY

- ACCESS TIMES: 70ns, 90ns
- PROGRAMMING TIME: 10µs per Byte typical
- PROGRAM/ERASE CONTROLLER (P/E.C.)
  - Embedded Byte Program Algorithm
  - Status Register bits and Ready/Busy Output
- 19 MEMORY BLOCKS
  - 1 Boot Block (Top or Bottom location)
  - 2 Parameter and 16 Main Blocks
- BLOCK, MULTI-BLOCK and CHIP ERASE
- MULTIPLE BLOCK PROTECTION/ TEMPORARY UNPROTECTION MODE
- ERASE SUSPEND and RESUME MODES
- LOW POWER CONSUMPTION
  - Standby and Automatic Standby modes
- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- 20 YEARS DATA RETENTION
  - Defectivity below 1ppm/year
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - M29W008ET Device Code: D2h
  - M29W008EB Device Code: DCh
- ECOPACK® TSOP40 PACKAGE

Figure 1. Package



TSOP40 (N)
10 x 20mm

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1 Summary description

The M29W008E is a 8 Mbit (1Mb x 8) non-volatile Flash memory that can be read, erased at block, multi-block or chip level and programmed at Byte level. These operations are performed using a single 2.7V to 3.6V V_{CC} supply voltage. For Program and Erase operations the necessary high voltages are generated internally. The device can also be programmed using standard programming equipment.

The memory is divided into blocks that are asymmetrically arranged. Both M29W008ET and M29W008EB devices have an array of 19 blocks composed of one Boot Block of 16 KBytes, two Parameter Blocks of 8 KBytes, one Main Block of 32 KBytes and fifteen Main Blocks of 64 KBytes. In the M29W008ET, the Boot Block is located at the top of the memory address space while in the M29W008EB, it is located at the bottom. The memory maps are showed in *Figure 4: Block Addresses (Top Boot Block)* and *Figure 5: Block Addresses (Bottom Boot Block)*. Each block can be erased and reprogrammed independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the Command Interface of the memory. An on-chip Program/Erase Controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. Erase operations in one block can be temporarily suspended in order to read from or program in blocks that are not being erased. Each block can be programmed and erased over 100,000 cycles.

Each block can be protected independently to prevent accidental Program or Erase commands from modifying the memory. All previously protected blocks can be temporarily unprotected.

In order to meet environmental requirements, ST offers this device in a TSOP40 (10 x 20mm) ECOPACK® package. ECOPACK® packages are Lead-free and RoHS compliant. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

The device is offered in package and supplied with all the bits erased (set to '1').

Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ7	Data Input/Outputs, Command Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset/Block Temporary Unprotect
$R\overline{B}$	Ready/Busy Output
V_{CC}	Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally

Figure 2. Logic diagram

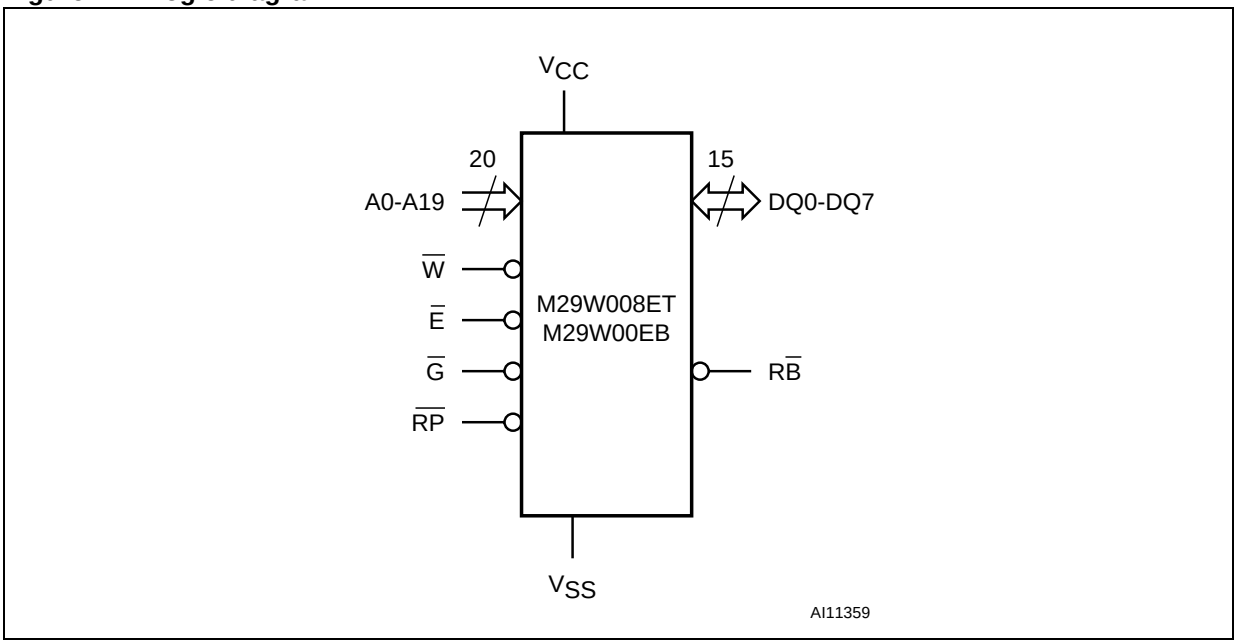


Figure 3. TSOP Connections

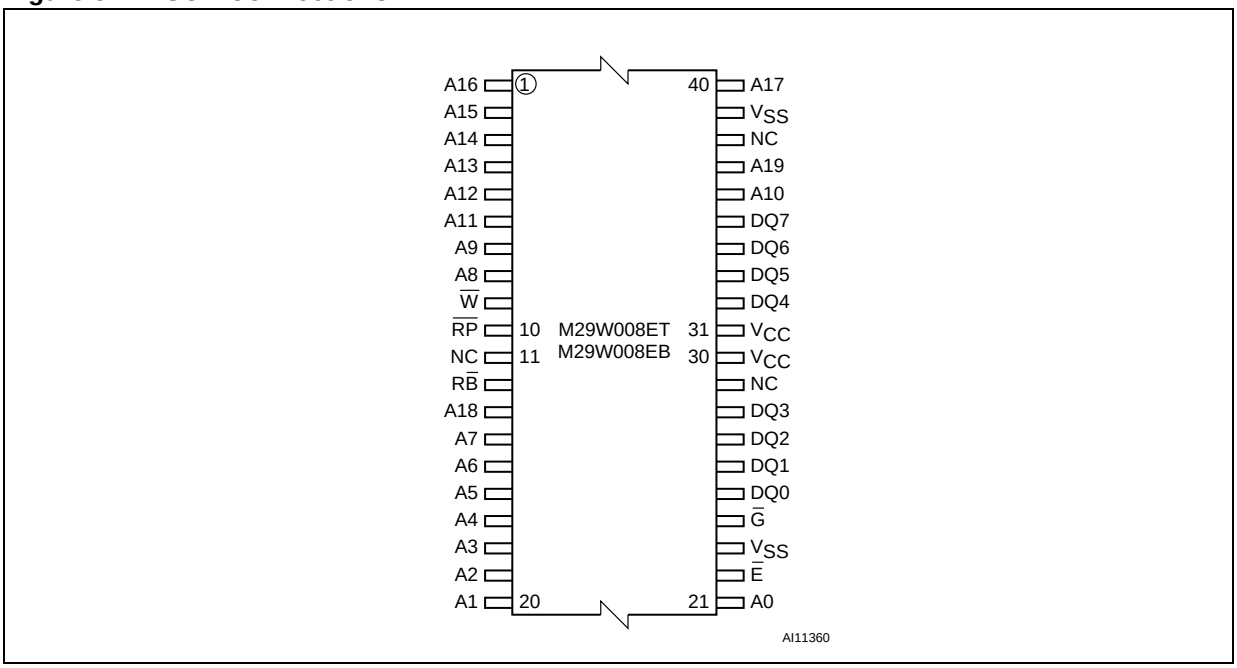


Figure 4. Block Addresses (Top Boot Block)

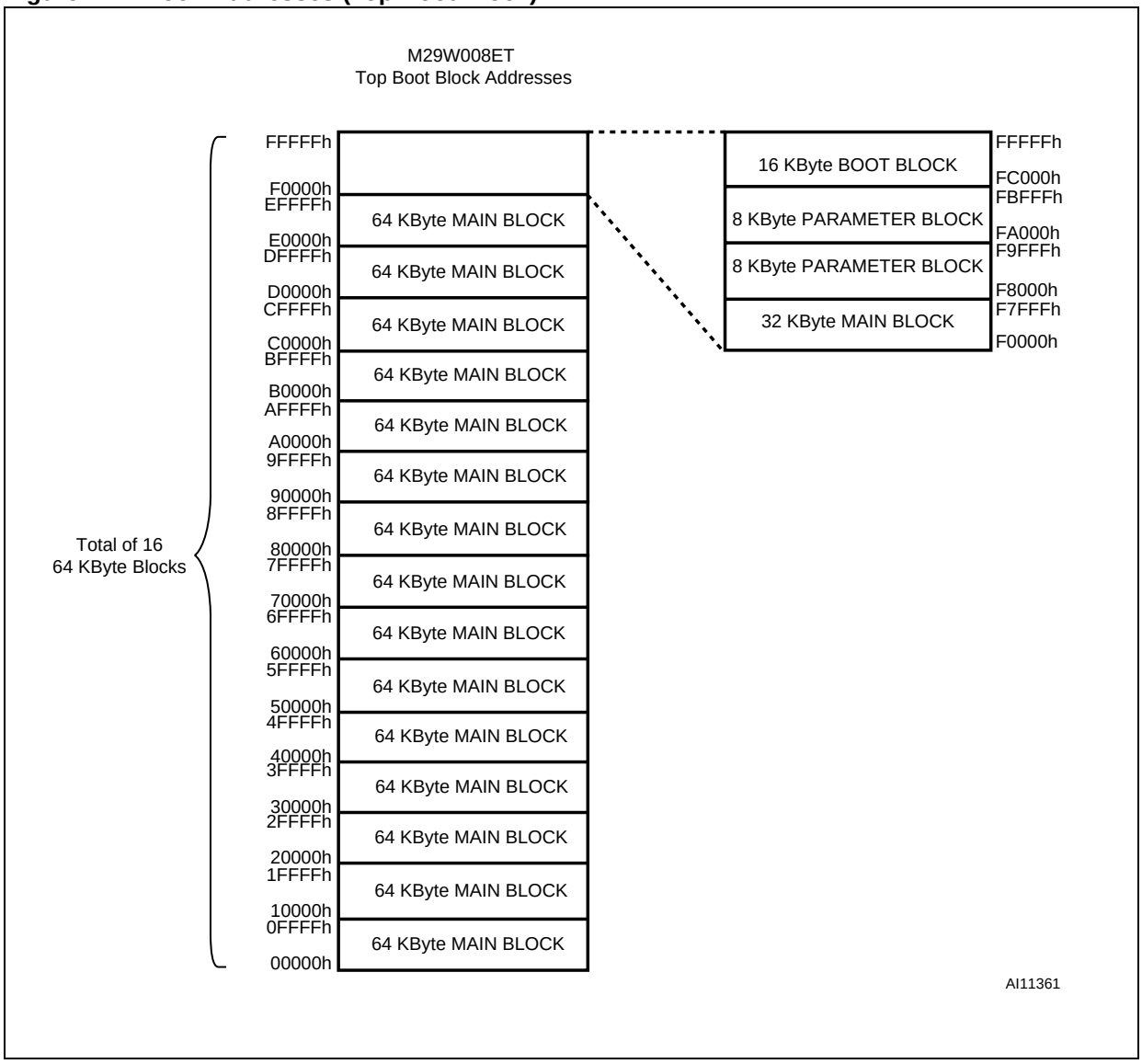
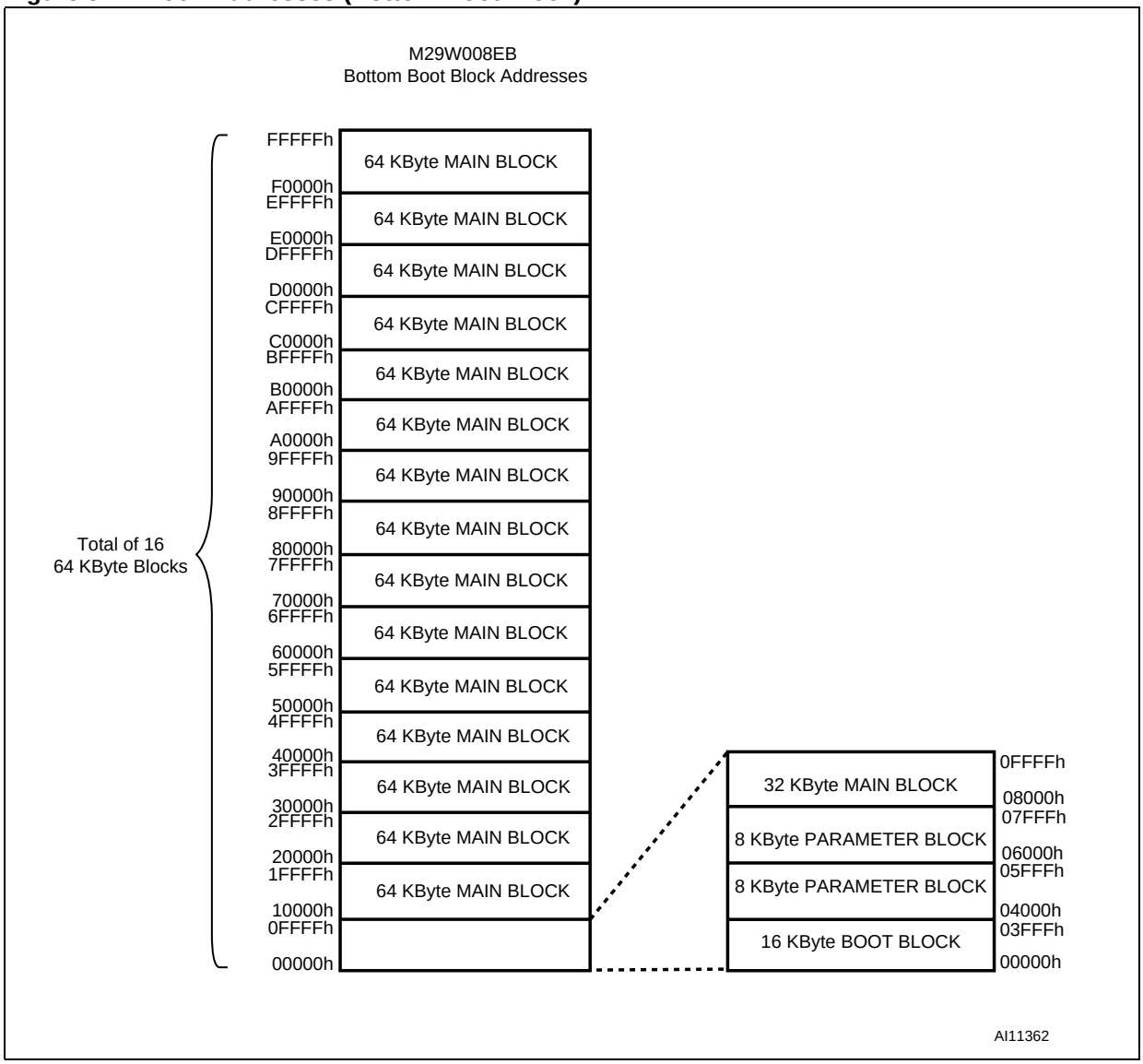


Figure 5. Block Addresses (Bottom Boot Block)



2 Signal descriptions

See *Figure 2: Logic diagram* and *Table 1: Signal Names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A19)

The address inputs for the memory array are latched during a Bus Write operation on the falling edge of Chip Enable, $\overline{E}$ or Write Enable, $\overline{W}$. When A9 is raised to V_{ID}, either a Read Electronic Signature Manufacturer or Device Code, Block Protection Status or a Write Block Protection or Block Unprotection is enabled depending on the combination of levels on A0, A1 A6, A12 and A15.

2.2 Data Input/Outputs (DQ0-DQ7)

During Bus Write operations, the Data Inputs/Outputs input the data to be programmed in the memory array or a command to be written to the Command Interface. Both are latched on the rising edge of Chip Enable, $\overline{E}$ or Write Enable, $\overline{W}$. The Data Inputs/Outputs output the data stored at the selected address during a Bus Read operation, the Electronic Signature (Manufacturer or Device codes), the Block Protection Status or the Data Polling bit (DQ7), Toggle Bits (DQ6) and DQ2), Error bit (DQ5) or Erase Timer bit (DQ3) of the Status Register. Outputs are valid when Chip Enable, $\overline{E}$ and Output Enable, $\overline{G}$ are active. The output is high impedance when the chip is deselected or the outputs are disabled and when $\overline{RP}$ is Low.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable, $\overline{E}$, activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is High, V_{IH}, the memory is deselected and the power consumption is reduced to the Standby level. The Chip Enable, $\overline{E}$, can also be used to control Write operations to the command register and to the memory array, while $\overline{W}$ remains Low. The Chip Enable must be forced to V_{ID} during Block Unprotection operations.

2.4 Output Enable ($\overline{G}$)

The Output Enable, $\overline{G}$, gates the outputs through the data buffers during a Bus Read operation. When $\overline{G}$ is High, V_{IH}, the outputs are high impedance. $\overline{G}$ must be forced to V_{ID} during Block Protection and Unprotection operations.

2.5 Write Enable ($\overline{W}$)

This Write Enable, $\overline{W}$, controls write operations of the memory's Command Interface.

2.6 Ready/Busy Output ($\overline{RB}$)

The Ready/Busy pin is an open-drain output that can be used to identify when the memory array can be read. Ready/Busy is high impedance during Read mode, Auto Select mode and Erase Suspend mode.

After a Hardware Reset, Bus Read and Bus Write operations cannot begin until Ready/Busy becomes high impedance. See *Table 13: Reset/Block Temporary Unprotect AC Characteristics* and *Figure 13: Reset/Block Temporary Unprotect AC Waveforms*.

During Program or Erase operations Ready/Busy is Low, V_{OL}. Ready/Busy will remain Low during Read/Reset commands or Hardware Resets until the memory is ready to enter Read mode.

2.7 Reset/Block Temporary Unprotect Input ($\overline{RP}$)

The Reset/Block Temporary Unprotect input, $\overline{RP}$, can be used to apply a Hardware Reset to the memory or to temporarily unprotect all blocks that have been previously protected.

A Hardware Reset is achieved by holding $\overline{RP}$ Low, V_{IL} for at least t_{PLPX}. After Reset/Block Temporary Unprotect goes High, V_{IH}, if the device is in Read or Standby mode, it will be ready for new operations t_{PHEL} after the rising edge of $\overline{RP}$. If the device is in Erase, Erase Suspend or Program mode, the Hardware Reset will last t_{PLYH} during which the $\overline{RB}$ signal will be held at V_{IL}. The end of the memory Hardware Reset will be indicated by the rising edge of $\overline{RB}$. A Hardware Reset during an Erase or Program operation will corrupt the data being programmed or the blocks being erased. See *Table 13: Reset/Block Temporary Unprotect AC Characteristics* and *Figure 13: Reset/Block Temporary Unprotect AC Waveforms*.

Holding $\overline{RP}$ at V_{ID} will temporarily unprotect the previously protected blocks in the memory. Program and Erase operations on all blocks will be possible. The transition of $\overline{RP}$ from V_{IH} to V_{ID} must slower than t_{PHPHH}.

When $\overline{RP}$ is returned from V_{ID} to V_{IH} all blocks temporarily unprotected will be again protected.

2.8 V_{CC} Supply Voltage

The power supply for all operations (Read, Program and Erase).

A 0.1µF capacitor should be connected between the V_{CC} Supply Voltage pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations, I_{CC3}

2.9 V_{SS} Ground

V_{SS} is the reference for all voltage measurements.

3 Bus Operations

There are 5 standard bus operations that control the device. These are Bus Read, us Write, Output Disable, Standby and Automatic Standby. See *Table 2: Bus Operations*, for a summary. Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect the bus operations.

3.1 Standard bus operations

3.1.1 Bus Read

Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register or the Block Protection Status. Both Chip Enable $\overline{E}$ and Output Enable $\overline{G}$ must be Low in order to read the output of the memory. A new Bus Read operation is initiated either on the falling edge of Chip Enable, $\overline{E}$, or on any address transition with $\overline{E}$ at V_{IL}.

See *Figure 10: Read Mode AC Waveforms*, and *Table 10: Read AC Characteristics* for details of the timing requirements.

3.1.2 Bus Write

Bus Write operations are used to write to the Command Interface or to latch input data to be programmed. A valid Bus Write operation begins by setting the desired address on the Address Inputs. The Address Inputs are latched by the Command Interface on the falling edge of Chip Enable or Write Enable, whichever occurs last. The Data Inputs/Outputs are latched by the Command Interface on the rising edge of Chip Enable or Write Enable, whichever occurs first. Output Enable must remain High, V_{IH}, during the whole Bus Write operation.

See Figures *11* and *12*, Write AC Waveforms and Tables *11* and *12*, Write AC Characteristics, for details of the timing requirements.

3.1.3 Output Disable

The data outputs are high impedance when the Output Enable $\overline{G}$ is High with Write Enable $\overline{W}$ High.

3.1.4 Standby

The memory is in Standby mode when Chip Enable, $\overline{E}$, is High and the Program/Erase Controller is idle. The Supply Current is reduced to the Standby Supply Current, I_{CC2}, and the outputs are high impedance, independent of the Output Enable $\overline{G}$ or Write Enable $\overline{W}$ inputs.

3.1.5 Automatic Standby

If CMOS levels ($V_{CC} \pm 0.2V$) are used to drive the bus and if the bus is inactive (no address transition, $\overline{E} = V_{IL}$) during 150ns or more, the memory automatically enters a Automatic Standby mode where the Supply Current is reduced to the Standby Supply Current, I_{CC2}. The Inputs/Outputs will still output data if a Bus Read operation is in progress.

3.2 Special bus operations

Additional bus operations can be performed to read the Electronic Signature and also to apply and remove Block Protection. These bus operations are intended for use by programming equipment and are not usually used in applications. They require V_{ID} to be applied to some pins.

3.2.1 Read Electronic Signature

The memory has two codes, the Manufacturer code and the Device code, that can be read to identify the memory.

These codes allow programming equipment or applications to automatically match their interface to the characteristics of the M29W008E.

The electronic Signature is output either by applying the signals listed in *Table 2: Bus Operations* or by issuing an Auto Select command (see *Section 4.2: Auto Select command*).

3.2.2 Block Protection and Unprotection

Each block can be individually protected against accidental Program or Erase using programming equipment. Protected blocks can be unprotected to allow data to be changed.

There are two methods available for protecting and unprotecting the blocks, one for use on programming equipment (Programmer Technique) and the other for in-system use (In-System Technique). Block Protect and Chip Unprotect operations are described in *Appendix B: Block protection*.

Table 2. Bus Operations

Operation			$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	Address Inputs A0-A19	DQ0-DQ7
Byte Read			V_{IL}	V_{IL}	V_{IH}	V_{IH}	Cell Address	Data Output
Byte Write			V_{IL}	V_{IH}	V_{IL}	V_{IH}	Command Address	Data Input
Output Disable			V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	Hi-Z
Standby			V_{IH}	X(1)	X(1)	V_{IH}	X	Hi-Z
Read Electronic signature	Manufacturer Code		V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0= V_{IL}, A1= V_{IL}, A9=V_{ID}, others address bits are 'Don't Care'	20h
	Device Code	M29W008ET	V_{IL}	V_{IL}	V_{IH}	V_{IH}	A0= V_{IH}, A1= V_{IL}, A9=V_{ID}, others address bits are 'Don't Care'	D2h
		M29W008EB						DCh

1. X = V_{IL} or V_{IH}.

4 Command interface

All Bus Write operations to the memory are interpreted by the Command Interface.

Commands consist of one or more sequential Bus Write operations. Failure to observe a valid sequence of Bus Write operations will result in the memory returning to Read mode. The long command sequences are imposed to maximize data security. All commands start with two coded cycles which unlock the Command Interface.

Seven commands are available: Read/Reset, Auto Select (to read the Electronic Signature and the Block Protection Status), Program, Block Erase, Chip Erase, Erase Suspend and Erase Resume (see *Table 3: Commands*).

4.1 Read/Reset command

The Read/Reset command returns the memory to its Read mode where it behaves like a ROM or EPROM, unless otherwise stated. It also resets the errors in the Status Register. Either one or three Bus Write operations can be used to issue the Read/Reset command.

The Read/Reset Command can be issued, between Bus Write cycles before the start of a program or erase operation, to return the device to read mode. Once the program or erase operation has started the Read/Reset command is no longer accepted. The Read/Reset command will not abort an Erase operation when issued while in Erase Suspend.

4.2 Auto Select command

The Auto Select command is used to read the Manufacturer Code, the Device Code and the Block Protection Status. Three consecutive Bus Write operations are required to issue the Auto Select command. Once the Auto Select command is issued the memory remains in Auto Select mode until another command is issued.

From the Auto Select mode the Manufacturer Code can be read using a Bus Read operation with A0 = VIL and A1 = VIL. The other address bits may be set to either VIL or VIH.

The Device Code can be read using a Bus Read operation with A0 = VIH and A1 = VIL. The other address bits may be set to either VIL or VIH.

The Block Protection Status of each block can be read using a Bus Read operation with A0 = VIL, A1 = VIH, and A13-A19 specifying the address of the block. The other address bits may be set to either VIL or VIH. If the addressed block is protected then 01h is output on Data Inputs/ Outputs DQ0-DQ7, otherwise 00h is output.

4.3 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four Bus Write operations, the final write operation latches the address and data and starts the Program/Erase Controller.

If the address falls in a protected block then the Program command is ignored, the data remains unchanged. The Status Register is never read and no error condition is given.

During the program operation the memory will ignore all commands. It is not possible to issue any command to abort or pause the operation. Typical program times are given in *Table 4: Program, Erase Times and Program, Erase Endurance Cycles*. Bus Read operations during the program operation will output the Status Register on the Data Inputs/Outputs. See *Section 5: Status register* for more details.

After the program operation has completed the memory will return to the Read mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

Note that the Program command cannot change a bit set at '0' back to '1'. One of the Erase Commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

4.4 Unlock Bypass command

The Unlock Bypass command is used in conjunction with the Unlock Bypass Program command to program the memory. When the access time to the device is long (as with some EPROM programmers) considerable time saving can be made by using these commands. Three Bus Write operations are required to issue the Unlock Bypass command.

Once the Unlock Bypass command has been issued the memory will only accept the Unlock Bypass Program command and the Unlock Bypass Reset command. The memory can be read as if in Read mode.

4.5 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in memory at a time. The command requires two Bus Write operations, the final write operation latches the address and data and starts the Program/Erase Controller.

The Program operation using the Unlock Bypass Program command behaves identically to the Program operation using the Program command. A protected block cannot be programmed; the operation cannot be aborted and the Status Register is read. Errors must be reset using the Read/Reset command, which leaves the device in Unlock Bypass Mode. See the Program command for details on the behavior.

4.6 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to Read/Reset mode from Unlock Bypass Mode. Two Bus Write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from Unlock Bypass Mode.

4.7 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. Six Bus Write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth Bus Write operation using the address of the additional block. The Block Erase operation starts the Program/Erase Controller about 50µs after the last Bus Write operation. Once the Program/Erase Controller starts it is not possible to select any more

blocks. Each additional block must therefore be selected within 50µs of the last block. The 50µs timer restarts when an additional block is selected. The Status Register can be read after the sixth Bus Write operation. See the Status Register for details on how to identify if the Program/Erase Controller has started the Block Erase operation.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the Block Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the Block Erase operation the memory will ignore all commands except the Erase Suspend command. Typical program times are given in *Table 4: Program, Erase Times and Program, Erase Endurance Cycles*. All Bus Read operations during the Block Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Block Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read mode.

The Block Erase Command sets all of the bits in the unprotected selected blocks to ’1’. All previous data in the selected blocks is lost.

4.8 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six Bus Write operations are required to issue the Chip Erase Command and start the Program/Erase Controller.

If any blocks are protected then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands. It is not possible to issue any command to abort the operation. Typical program times are given in *Table 4: Program, Erase Times and Program, Erase Endurance Cycles*. All Bus Read operations during the Chip Erase operation will output the Status Register on the Data Inputs/Outputs. See the section on the Status Register for more details.

After the Chip Erase operation has completed the memory will return to the Read Mode, unless an error has occurred. When an error occurs the memory will continue to output the Status Register. A Read/Reset command must be issued to reset the error condition and return to Read Mode.

The Chip Erase Command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

4.9 Erase Suspend command

The Erase Suspend Command may be used to temporarily suspend a Block Erase operation and return the memory to Read mode. The command requires one Bus Write operation.

The Program/Erase Controller will suspend within the Erase Suspend Latency Time after the Erase Suspend Command is issued (see *Table 4: Program, Erase Times and Program, Erase*

Endurance Cycles). Once the Program/Erase Controller has stopped the memory will be set to Read mode and the Erase will be suspended. If the Erase Suspend command is issued during the period when the memory is waiting for an additional block (before the Program/Erase Controller starts) then the Erase is suspended immediately and will start immediately when the Erase Resume Command is issued. It is not possible to select any further blocks to erase after the Erase Resume.

During Erase Suspend it is possible to Read and Program cells in blocks that are not being erased; both Read and Program operations behave as normal on these blocks. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. The Status Register is not read and no error condition is given. Reading from blocks that are being erased will output the Status Register.

It is also possible to issue the Auto Select, during an Erase Suspend. The Read/Reset command must be issued to return the device to Read Array mode before the Resume command will be accepted.

4.10 Erase Resume Command

The Erase Resume command must be used to restart the Program/Erase Controller from Erase Suspend. An erase can be suspended and resumed more than once.

Table 3. Commands

Command[1]	Length	Bus Write Operations[2][3]													
		1st		2nd		3rd		4th		5th		6th		7th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset[4][5]	1+	X	F0h	Read Memory Array until a new write cycle is initiated.											
	3+	555h	AAh	2AAh	55h	555h	F0h	Read Memory Array until a new write cycle is initiated.							
Auto Select[5]	3+	555h	AAh	2AAh	55h	555h	90h	Read Electronic Signature or Block Protection Status until a new write cycle is initiated. [6][7]							
Program	4	555h	AAh	2AAh	55h	555h	A0h	PA	PD	Read Data Polling or Toggle Bit until Program completes.					
Unlock Bypass	3	555h	AAh	2AAh	55h	555h	20h								
Unlock Bypass Program	2	X	A0h	PA	PD										
Unlock Bypass Reset	2	X	90h	X	00h										
Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h	[8]	
Block Erase	6+	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA	30h	AB [9]	30h
Erase Suspend[10]	1	X	B0h	Read until Toggle stops, then read all the data needed from any Block(s) not being erased then Resume Erase.											
Erase Resume	1	X	30h	Read Data Polling or Toggle Bits until Erase completes or Erase is suspended another time.											

1. Commands not interpreted in this table will default to read array mode.
2. X = Don't Care. PA = Program Address, PD = Program Data, BA = Block Address, AB = Additional Block.
3. For Coded cycles address inputs A15-A19 are don't care.
4. A wait of t_{PLYH} is necessary after a Read/Reset command if the memory was in an Erase or Program mode before starting any new operation (see *Table 10: Read AC Characteristics*).
5. The first cycles of the Read/Reset and Auto Select commands are followed by read operations. Any number of read cycles can occur after the command cycles.
6. Signature Address bits A0, A1, at V_{IL} will output the Manufacturer Code (20h). Address bits A0 at V_{IH} and A1, at V_{IL} will output the Device Code.
7. Block Protection Address: A0, at V_{IL}, A1 at V_{IH} and A13-A19 within the Block will output the Block Protection status.
8. Read Data Polling, Toggle bits or $R\overline{B}$ until Erase completes.
9. Optional, Additional Block (AB) addresses must be entered within the erase time-out delay after last write entry, time-out status can be verified through DQ3 value (see Erase Timer Bit DQ3 description). When full command is entered, read Data Polling or Toggle bit until Erase has completed or is suspended.
10. During Erase Suspend, Read and Data Program functions are allowed in blocks not being erased.

Table 4. Program, Erase Times and Program, Erase Endurance Cycles

Parameter	Min	Typ(1)(2)	Max(2)	Unit
Chip Erase		12	60(3)	s
Block Erase (64 KBytes)		0.8	6(4)	s
Erase Suspend Latency Time		15	25(3)	µs
Program (Byte)		10	200(3)	µs
Chip Program (Byte by Byte)		12	60(3)	s
Program/Erase Cycles (per Block)	100,000			cycles
Data Retention	20			years

1. Typical values measured at room temperature and nominal voltages.
2. Sampled, but not 100% tested.
3. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,00 program/erase cycles.
4. Maximum value measured at worst case conditions for both temperature and V_{CC}.

5 Status register

The status of the Program/Erase Controller during command execution is indicated by bit DQ7 (Data Polling bit), Toggle bits DQ6 and DQ2 and Error bits DQ3 and DQ5. Any attempt to read the memory array during Program or Erase command execution will automatically output these five Status Register bits. The Program/Erase Controller automatically sets bits DQ2, DQ3, DQ5, DQ6 and DQ7. Other bits (DQ0, DQ1 and DQ4) are reserved for future use and should be masked (see *Table 5: Status Register Bits*).

5.1 Data Polling Bit (DQ7)

The Data Polling Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Data Polling Bit is output on DQ7 when the Status Register is read.

During Program operations the Data Polling Bit outputs the complement of the bit being programmed to DQ7. After successful completion of the Program operation the memory returns to Read mode and Bus Read operations from the address just programmed output DQ7, not its complement.

During Erase operations the Data Polling Bit outputs ’0’, the complement of the erased state of DQ7. After successful completion of the Erase operation the memory returns to Read Mode.

In Erase Suspend mode the Data Polling Bit will output a ’1’ during a Bus Read operation within a block being erased. The Data Polling Bit will change from a ’0’ to a ’1’ when the Program/Erase Controller has suspended the Erase operation.

Figure 6: Data Polling Flowchart gives an example of how to use the Data Polling Bit. A Valid Address is the address being programmed or an address within the block being erased.

5.2 Toggle Bit (DQ6)

The Toggle Bit can be used to identify whether the Program/Erase Controller has successfully completed its operation or if it has responded to an Erase Suspend. The Toggle Bit is output on DQ6 when the Status Register is read.

During Program and Erase operations the Toggle Bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations at any address. After successful completion of the operation the memory returns to Read mode.

During Erase Suspend mode the Toggle Bit will output when addressing a cell within a block being erased. The Toggle Bit will stop toggling when the Program/Erase Controller has suspended the Erase operation.

If any attempt is made to erase a protected block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 100µs. If any attempt is made to program a protected block or a suspended block, the operation is aborted, no error is signalled and DQ6 toggles for approximately 1µs.

Figure 7: Data Toggle Flowchart gives an example of how to use the Data Toggle bit.

5.3 Error Bit (DQ5)

The Error Bit can be used to identify errors detected by the Program/Erase Controller. The Error Bit is set to ’1’ when a Program, Block Erase or Chip Erase operation fails to write the correct data to the memory. If the Error Bit is set a Read/Reset command must be issued before other commands are issued. The Error bit is output on DQ5 when the Status Register is read.

Note that the Program command cannot change a bit set to ’0’ back to ’1’ and attempting to do so will set DQ5 to ‘1’. A Bus Read operation to that address will show the bit is still ‘0’. One of the Erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’

5.4 Erase Timer Bit (DQ3)

The Erase Timer Bit can be used to identify the start of Program/Erase Controller operation during a Block Erase command. Once the Program/Erase Controller starts erasing the Erase Timer Bit is set to ’1’. Before the Program/Erase Controller starts the Erase Timer Bit is set to ’0’ and additional blocks to be erased may be written to the Command Interface. The Erase Timer Bit is output on DQ3 when the Status Register is read.

5.5 Alternative Toggle Bit (DQ2)

The Alternative Toggle Bit can be used to monitor the Program/Erase controller during Erase operations. The Alternative Toggle Bit is output on DQ2 when the Status Register is read.

During Chip Erase and Block Erase operations the Toggle Bit changes from ’0’ to ’1’ to ’0’, etc., with successive Bus Read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to Read mode.

During Erase Suspend the Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read operations from addresses within the blocks being erased. Bus Read operations to addresses within blocks not being erased will output the memory cell data as if in Read mode.

After an Erase operation that causes the Error Bit to be set the Alternative Toggle Bit can be used to identify which block or blocks have caused the error. The Alternative Toggle Bit changes from ’0’ to ’1’ to ’0’, etc. with successive Bus Read Operations from addresses within blocks that have not erased correctly. The Alternative Toggle Bit does not change if the addressed block has erased correctly.

Table 5. Status Register Bits

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	$\overline{RB}$
Program	Any Address	DQ7	Toggle	0	–	–	0
Program During Erase Suspend	Any Address	DQ7	Toggle	0	–	–	0
Program Error	Any Address	DQ7	Toggle	1	–	–	0
Chip Erase	Any Address	0	Toggle	0	1	Toggle	0
Block Erase before timeout	Erasing Block	0	Toggle	0	0	Toggle	0
	Non-Erasing Block	0	Toggle	0	0	No Toggle	0
Block Erase	Erasing Block	0	Toggle	0	1	Toggle	0
	Non-Erasing Block	0	Toggle	0	1	No Toggle	0
Erase Suspend	Erasing Block	1	No Toggle	0	–	Toggle	1
	Non-Erasing Block	Data read as normal					1
Erase Error	Good Block Address	0	Toggle	1	1	No Toggle	0
	Faulty Block Address	0	Toggle	1	1	Toggle	0

Note: Unspecified data bits should be ignored.

Figure 6. Data Polling Flowchart

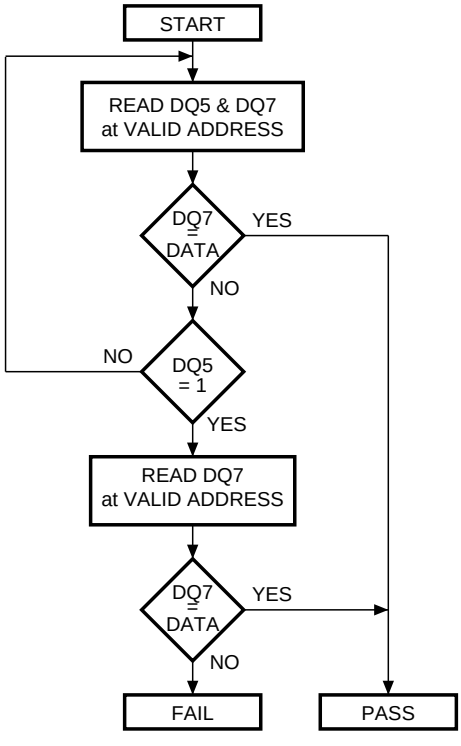
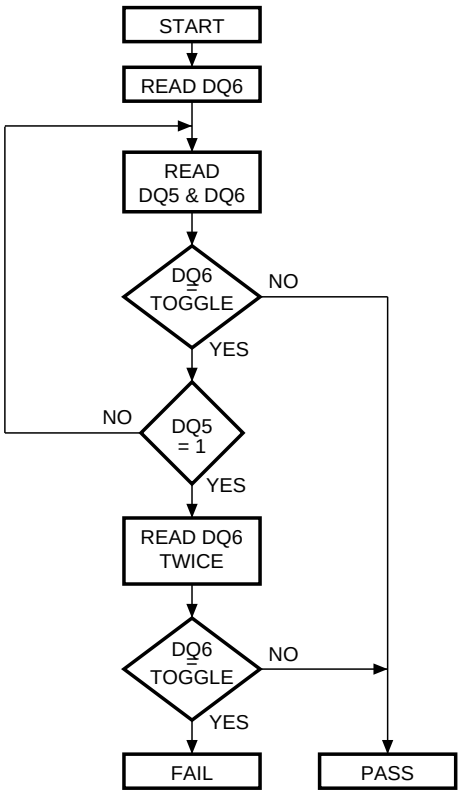


Figure 7. Data Toggle Flowchart



6 Maximum rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
T_{BIAS}	Temperature Under Bias	–50 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
T_{LEAD}	Lead Temperature during Soldering(1)	260(2)	°C
V_{IO}(3)	Input or Output Voltage	–0.6 to 5	V
V_{CC}	Supply Voltage	–0.6 to 5	V
V_{ID}(3)	Identification Voltage	–0.6 to 13.5	V

1. Compliant with the ST 7191395 specification for Lead-free soldering processes.
2. Not exceeding 250°C for more than 30s, and peaking at 260°C.
3. V_{ID} and V_{IO} may undershoot to –2V during transition and for less than 20ns during transitions.

7 DC and AC characteristics

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 7: Operating and AC Measurement Conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 7. Operating and AC Measurement Conditions

Parameter	M29W008E				Unit
	70		90		
	Min	Max	Min	Max	
V_{CC} Supply Voltage	2.7	3.6	2.7	3.6	V
Ambient Operating Temperature (range 6)	–40	85	–40	85	°C
Ambient Operating Temperature (range 1)	0	70	0	70	
Load Capacitance (C_L)	30		100		pF
Input Rise and Fall Times		10		10	ns
Input Pulse Voltages	0 to V_{CC}		0 to V_{CC}		V
Input and Output Timing Ref. Voltages	$V_{CC}/2$		$V_{CC}/2$		V

Figure 8. AC Testing Input Output Waveform

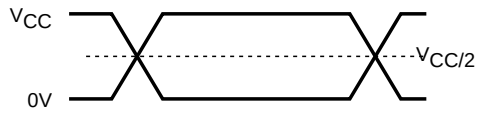


Figure 9. AC Testing Load Circuit

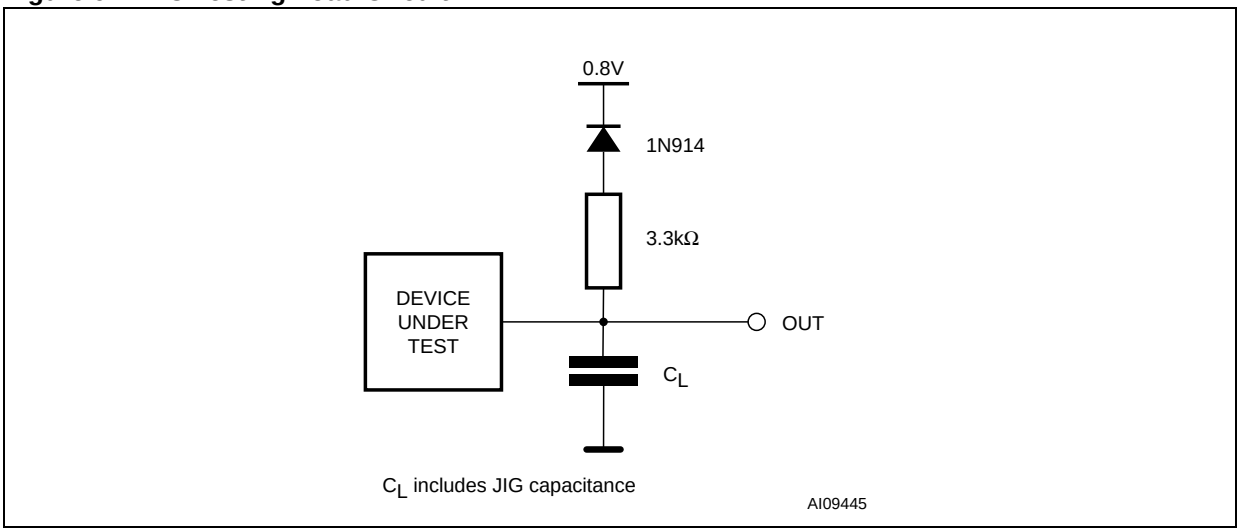


Table 8. Device Capacitance

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V		12	pF

Note: Sampled only, not 100% tested.

Table 9. DC Characteristics

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{CC}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{CC}$		±1	µA
I_{CC1}	Supply Current (Read)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$, f = 6MHz		10	mA
I_{CC2}	Supply Current (Standby)	$\overline{E} = V_{CC}$ ±0.2V $\overline{RP} = V_{CC}$ ±0.2V		100	µA
I_{CC3}(1)	Supply Current (Program or Erase)	Program,/ Erase Controller active		20	mA
V_{IL}	Input Low Voltage		–0.5	0.8	V
V_{IH}	Input High Voltage		0.7 V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 1.8mA		0.45	V
V_{OH}	Output High Voltage CMOS	I_{OH} = –100µA	V_{CC} –0.4V		V
V_{ID}	A9 Voltage (Electronic Signature)		11.5	12.5	V
I_{ID}	A9 Current (Electronic Signature)	A9 = V_{ID}		100	µA
V_{LKO}(1)	Supply Voltage (Erase and Program lock-out)		1.8	2.3	V

1. Sampled only, not 100% tested.

Figure 10. Read Mode AC Waveforms

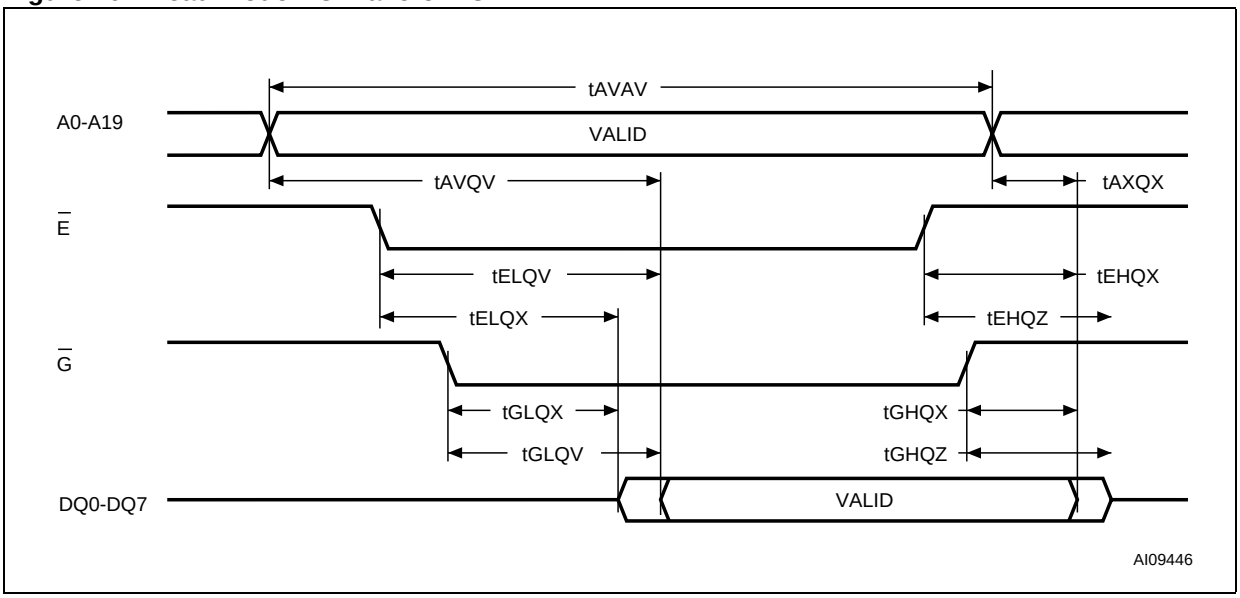


Table 10. Read AC Characteristics

Symbol	Alt	Parameter	Test Condition		M29W008E		Unit
					70	90	
t_{AVAV}(1)	t_{RC}	Address Valid to Next Address Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Min	70	90	ns
t_{AVQV}(1)	t_{ACC}	Address Valid to Output Valid	$\overline{E} = V_{IL}$, $\overline{G} = V_{IL}$	Max	70	90	ns
t_{ELQX}(2)	t_{LZ}	Chip Enable Low to Output Transition	$\overline{G} = V_{IL}$	Min	0	0	ns
t_{ELQV}(1)	t_{CE}	Chip Enable Low to Output Valid	$\overline{G} = V_{IL}$	Max	70	90	ns
t_{GLQX}(2)	t_{OLZ}	Output Enable Low to Output Transition	$\overline{E} = V_{IL}$	Min	0	0	ns
t_{GLQV}(1)	t_{OE}	Output Enable Low to Output Valid	$\overline{E} = V_{IL}$	Max	30	35	ns
t_{EHQZ}(2)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G} = V_{IL}$	Max	25	30	ns
t_{GHQZ}(2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E} = V_{IL}$	Max	25	30	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address Transition to Output Transition		Min	0	0	ns

1. Address are latched on the falling edge of $\overline{W}$, Data is latched on the rising edge of $\overline{W}$.
2. Sampled only, not 100% tested.

Figure 11. Write AC Waveforms, $\overline{W}$ Controlled

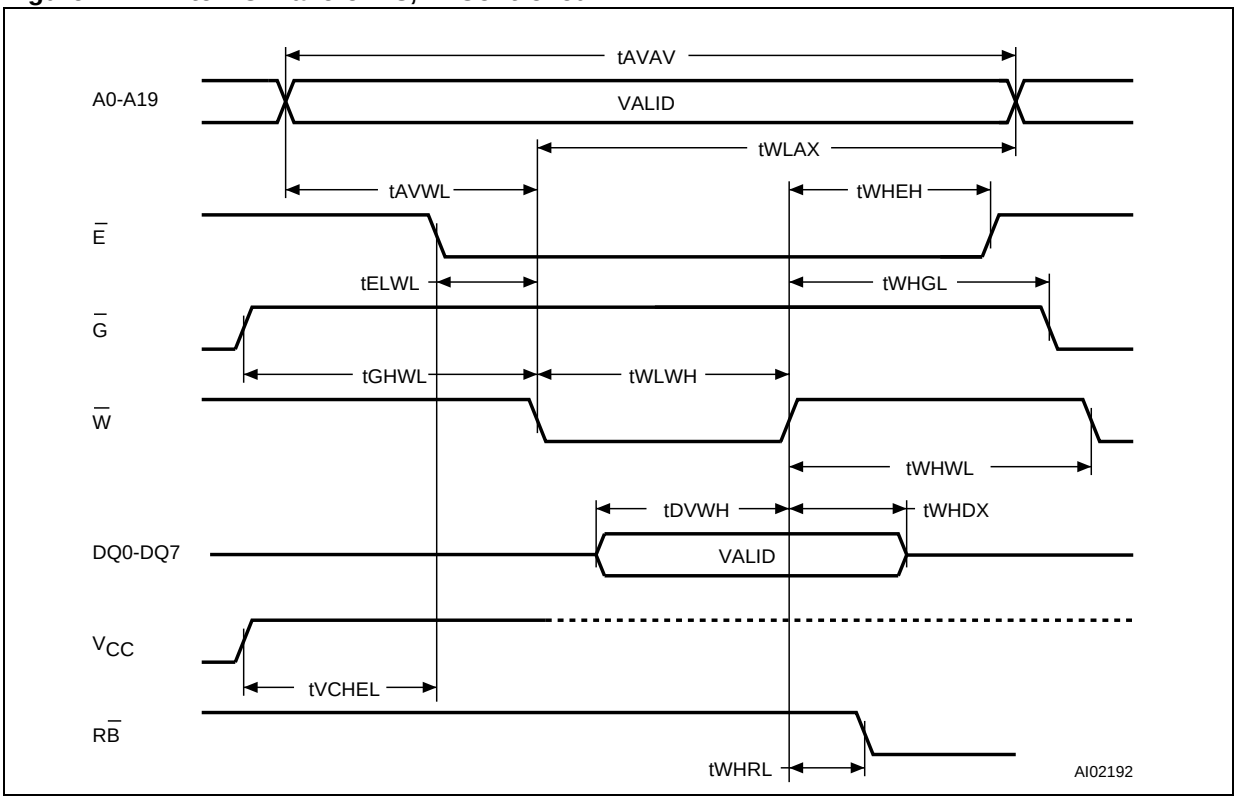
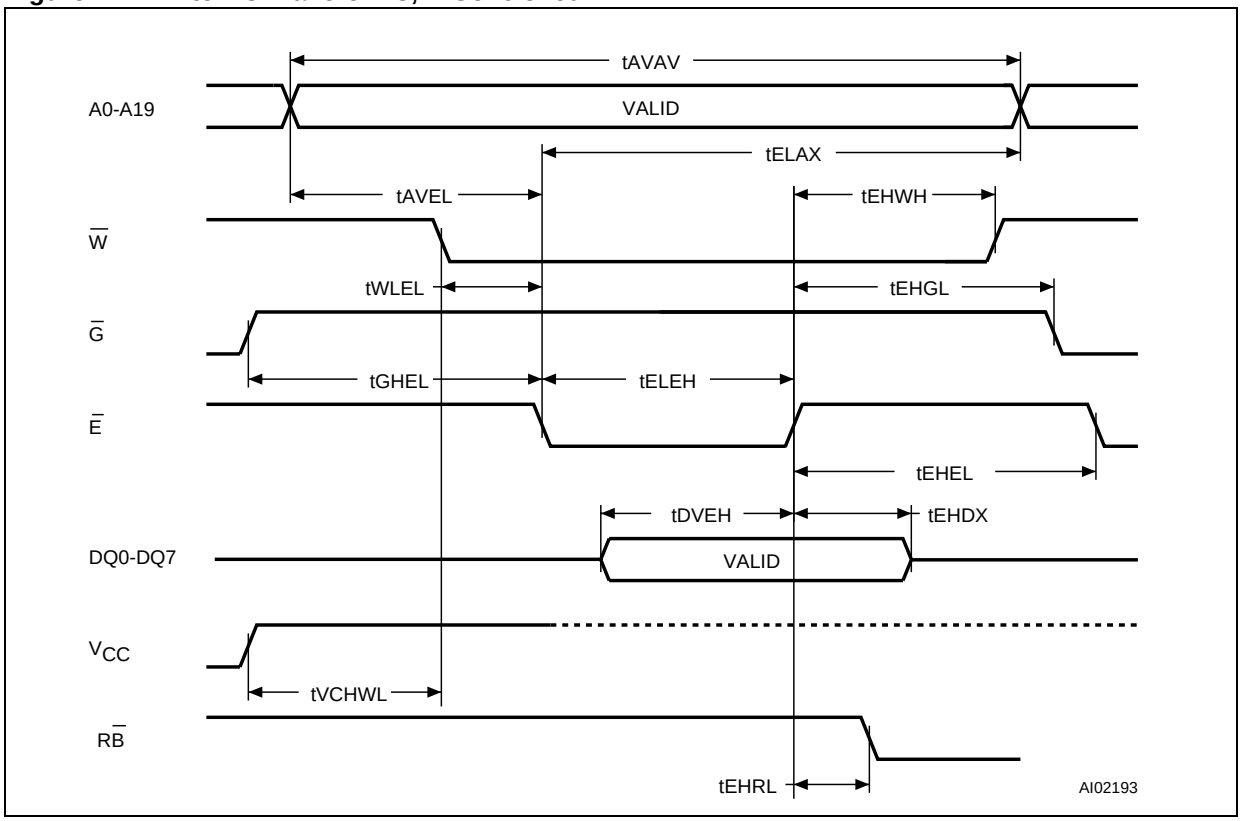


Table 11. Write AC Characteristics, $\overline{W}$ Controlled

Symbol	Alt	Parameter		M29W008E		Unit
				70	90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	90	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	45	50	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	50	ns
t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address Transition	Min	45	50	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	ns
t_{WHRL} (1)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	35	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	µs

1. Sampled only, not 100% tested.

Figure 12. Write AC Waveforms, $\overline{E}$ Controlled



Note: Address are latched on the falling edge of $\overline{E}$, Data is latched on the rising edge of $\overline{E}$.

Table 12. Write AC Characteristics, $\overline{E}$ Controlled

Symbol	Alt	Parameter		M29W008E		Unit
				70	90	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	70	90	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	45	50	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	50	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address Transition	Min	45	50	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	ns
t_{EHGL}	t_{OEH}	Chip Enable High to Output Enable Low	Min	0	0	ns
t_{EHRL} (1)	t_{BUSY}	Program/Erase Valid to $R\overline{B}$ Low	Max	30	35	ns
t_{VCHWL}	t_{VCS}	V_{CC} High to Write Enable Low	Min	50	50	µs

1. Sampled only, not 100% tested.

Figure 13. Reset/Block Temporary Unprotect AC Waveforms

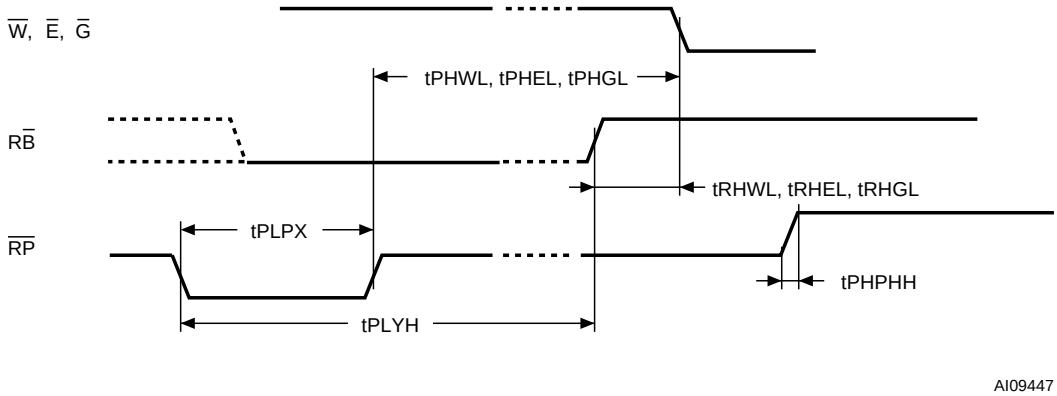


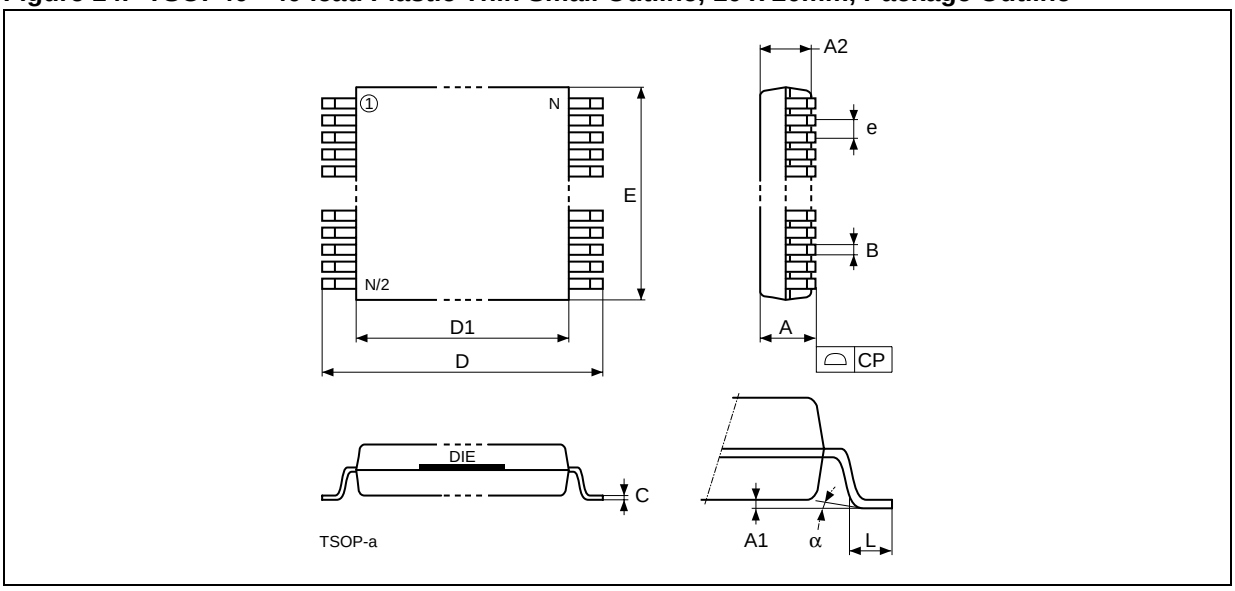
Table 13. Reset/Block Temporary Unprotect AC Characteristics

Symbol	Alt	Parameter		M29W008E		Unit
				70	90	
t_{PHWL}(1) t_{PHEL} t_{PHGL}(1)	t_{RH}	RP High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	50	50	ns
t_{RHWL}(1) t_{RHEL}(1) t_{RHGL}(1)	t_{RB}	RB High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	ns
t_{PLPX}	t_{RP}	RP Pulse Width	Min	500	500	ns
t_{PLYH}(1)	t_{READY}	RP Low to Read Mode	Max	10	10	µs
t_{PHPHH}(1)	t_{VIDR}	RP Rise Time to V_{ID}	Min	500	500	ns

1. Sampled only, not 100% tested.

8 Package mechanical

Figure 14. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm, Package Outline



Note: Drawing is not to scale.

Table 14. TSOP40 - 40 lead Plastic Thin Small Outline, 10 x 20mm, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0
A1		0.050	0.150		0	0
A2		0.950	1.050		0	0
B		0.170	0.270		0	0
C		0.100	0.210		0	0
CP			0.100			0
D		19.800	20.200		1	1
D1		18.300	18.500		1	1
e	0.500	–	–	0	–	–
E		9.900	10.100		0	0
L		0.500	0.700		0	0
α		0	5		0	5
N	40			40		

9 Part numbering

Table 15. Ordering Information Scheme

Example: M29W008ET 70 N 1 E

Device Type
M29

Operating Voltage
W = 2.7 to 3.6V

Device Function
008E = 8 Mbit (1Mb x8), Boot Block

Array Matrix
T = Top Boot
B = Bottom Boot

Speed
70 = 70ns
90 = 90ns

Package
N = TSOP40: 10 x 20 mm

Temperature Range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
E = ECOPACK Package, Standard Packing
F = ECOPACK Package, Tape & Reel 24mm Packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Appendix A Block address table

Table 16. Top Boot Block Addresses, M29W008ET

#	Size (Kbytes)	Address Range (x8)
18	16	FC000h-FFFFFh
17	8	FA000h-FBFFFh
16	8	F8000h-F9FFFh
15	32	F0000h-F7FFFh
14	64	E0000h-EFFFFh
13	64	D0000h-DFFFFh
12	64	C0000h-CFFFFh
11	64	B0000h-BFFFFh
10	64	A0000h-AFFFFh
9	64	90000h-9FFFFh
8	64	80000h-8FFFFh
7	64	70000h-7FFFFh
6	64	60000h-6FFFFh
5	64	50000h-5FFFFh
4	64	40000h-4FFFFh
3	64	30000h-3FFFFh
2	64	20000h-2FFFFh
1	64	10000h-1FFFFh
0	64	00000h-0FFFFh

Table 17. Bottom Boot Block Addresses, M29W008EB

#	Size (Kbytes)	Address Range (x8)
18	64	F0000h-FFFFFh
17	64	E0000h-EFFFFh
16	64	D0000h-DFFFFh
15	64	C0000h-CFFFFh
14	64	B0000h-BFFFFh
13	64	A0000h-AFFFFh
12	64	90000h-9FFFFh
11	64	80000h-8FFFFh
10	64	70000h-7FFFFh

9	64	60000h-6FFFFh
8	64	50000h-5FFFFh
7	64	40000h-4FFFFh
6	64	30000h-3FFFFh
5	64	20000h-2FFFFh
4	64	10000h-1FFFFh
3	32	08000h-0FFFFh
2	8	06000h-07FFFh
1	8	04000h-05FFFh
0	16	00000h-03FFFh

Appendix B Block protection

Block protection can be used to prevent any operation from modifying the data stored in the Flash. Each Block can be protected individually. Once protected, Program and Erase operations on the block fail to change the data.

There are three techniques that can be used to control Block Protection, these are the Programmer technique, the In-System technique and Temporary Unprotection. Temporary Unprotection is controlled by the Reset/Block Temporary Unprotection pin, $\overline{RP}$; this is described in the Signal Descriptions section.

Unlike the Command Interface of the Program/Erase Controller, the techniques for protecting and unprotecting blocks change between different Flash memory suppliers. For example, the techniques for AMD parts will not work on STMicroelectronics parts. Care should be taken when changing drivers for one part to work on another.

9.1 Programmer technique

The Programmer technique uses high (V_{ID}) voltage levels on some of the bus pins. These cannot be achieved using a standard microprocessor bus, therefore the technique is recommended only for use in Programming Equipment.

To protect a block follow the flowchart in *Figure 15: Programmer Equipment Block Protect Flowchart*. To unprotect the whole chip it is necessary to protect all of the blocks first, then all blocks can be unprotected at the same time. To unprotect the chip follow *Figure 16: Programmer Equipment Chip Unprotect Flowchart*. *Table 18: Programmer Technique Bus Operations*, gives a summary of each operation.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

9.2 In-System technique

The In-System technique requires a high voltage level on the Reset/Blocks Temporary Unprotect pin, $\overline{RP}$. This can be achieved without violating the maximum ratings of the components on the microprocessor bus, therefore this technique is suitable for use after the Flash has been fitted to the system.

To protect a block follow the flowchart in *Figure 17: In-System Equipment Block Protect Flowchart*. To unprotect the whole chip it is necessary to protect all of the blocks first, then all the blocks can be unprotected at the same time. To unprotect the chip follow *Figure 18: In-System Equipment Chip Unprotect Flowchart*.

The timing on these flowcharts is critical. Care should be taken to ensure that, where a pause is specified, it is followed as closely as possible. Do not allow the microprocessor to service interrupts that will upset the timing and do not abort the procedure before reaching the end. Chip Unprotect can take several seconds and a user message should be provided to show that the operation is progressing.

Table 18. Programmer Technique Bus Operations

Operation	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address Inputs A0-A18	Data Inputs/Outputs DQ7-DQ0
Block Protect	V_{IL}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A13-A19= Block Address Others = X	X
Chip Unprotect	V_{ID}	V_{ID}	V_{IL} Pulse	A9 = V_{ID}, A13 = V_{IH}, A16 = V_{IH} Others = X	X
Block Protection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IL}, A9 = V_{ID}, A13-A19= Block Address Others = X	Pass = 01h Retry = 00h
Block Unprotection Verify	V_{IL}	V_{IL}	V_{IH}	A0 = V_{IL}, A1 = V_{IH}, A6 = V_{IH}, A9 = V_{ID}, A13-A19= Block Address Others = X	Retry = 01h Pass = 00h

Figure 15. Programmer Equipment Block Protect Flowchart

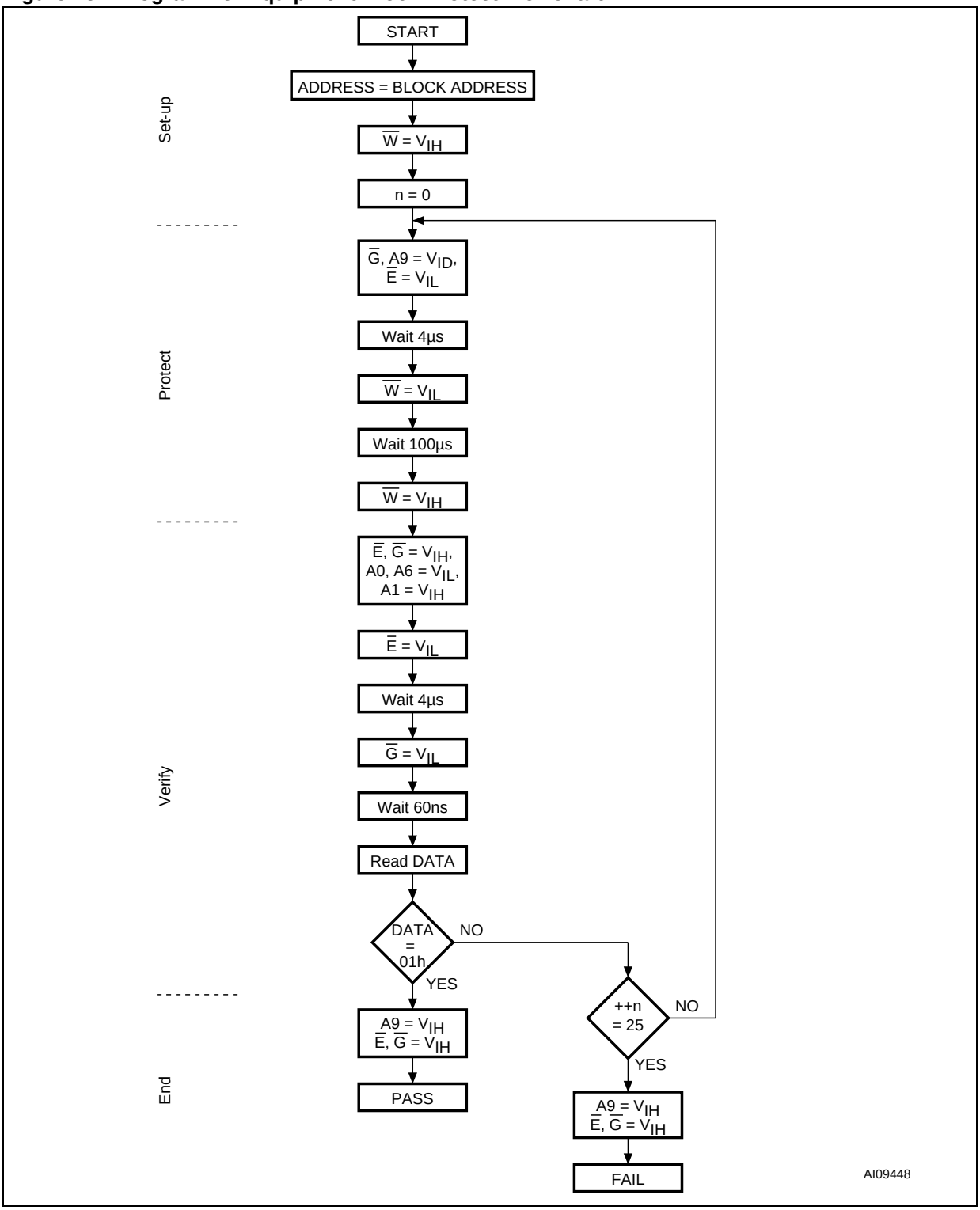


Figure 16. Programmer Equipment Chip Unprotect Flowchart

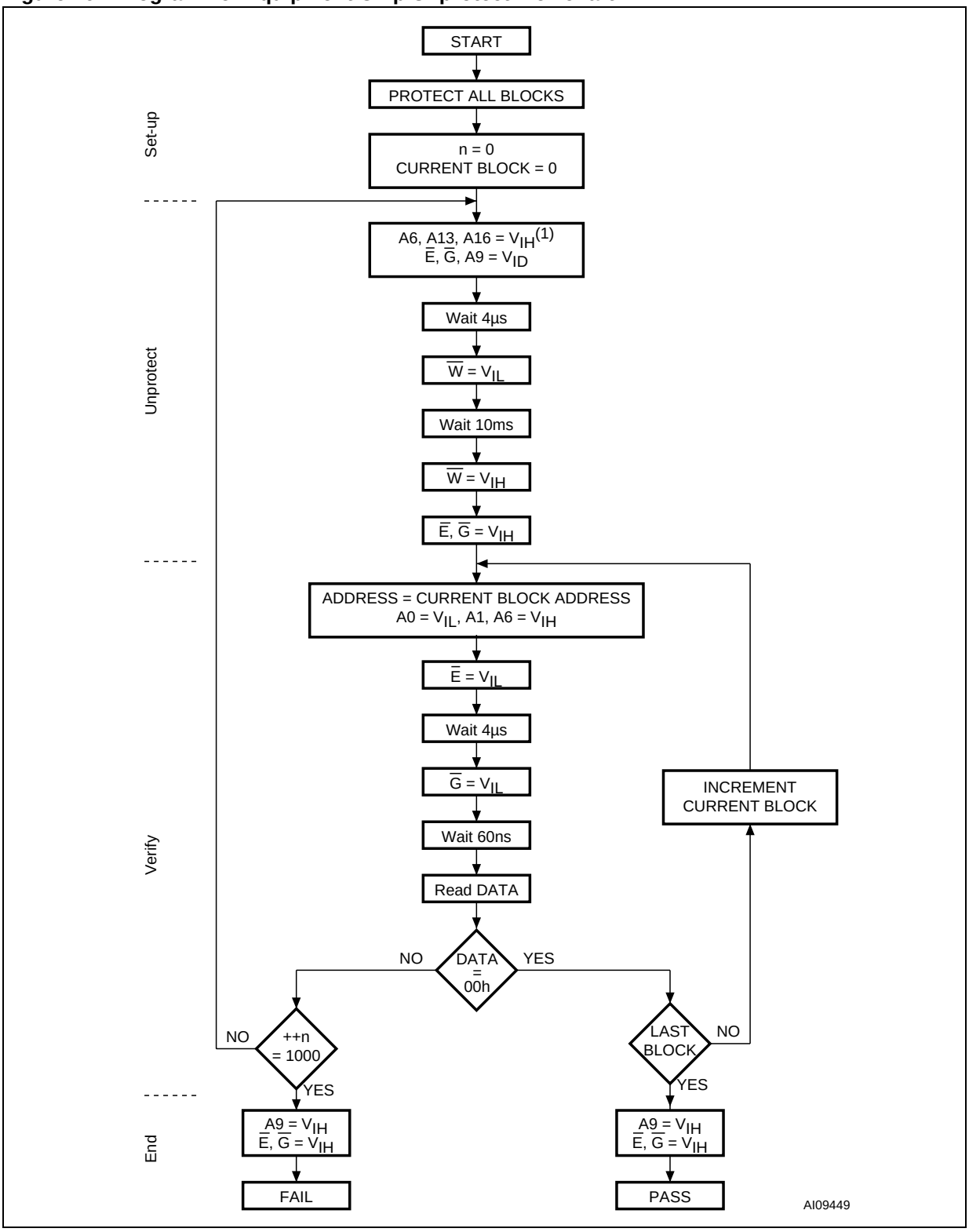


Figure 17. In-System Equipment Block Protect Flowchart

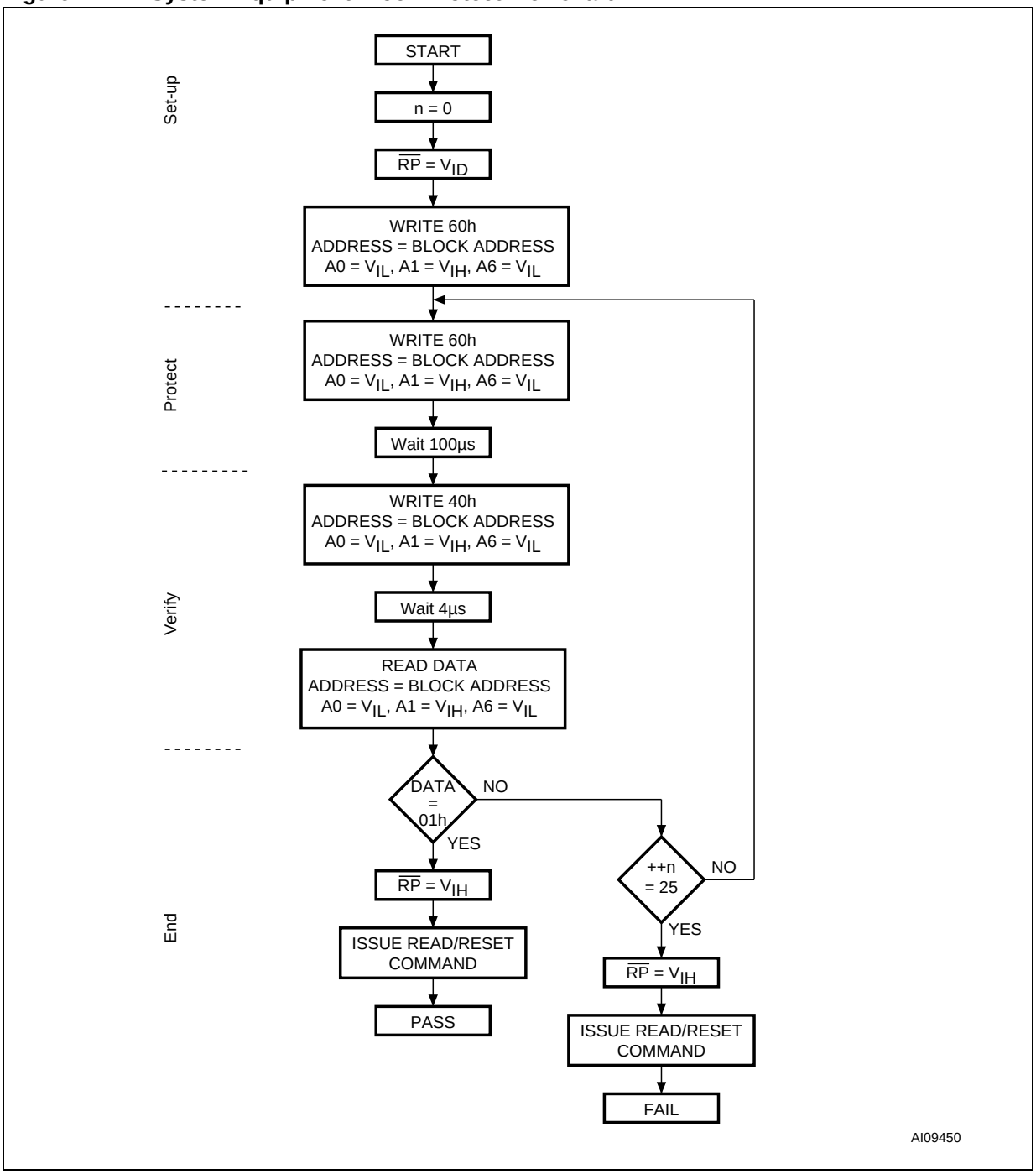
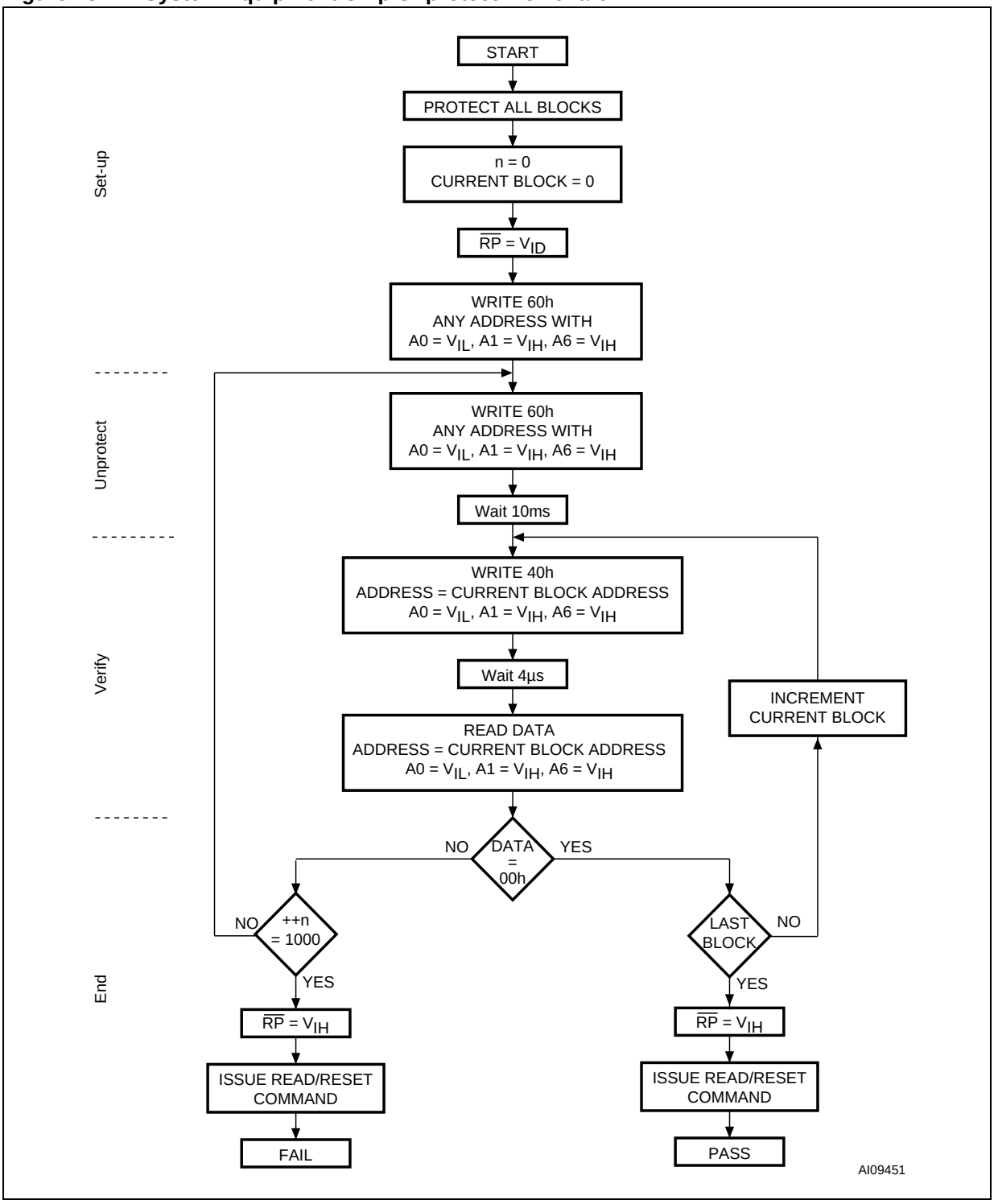


Figure 18. In-System Equipment Chip Unprotect Flowchart



10 Revision history

Table 19. Document Revision History

Date	Version	Revision Details
21-Jun-2005	0.1	First Issue.