M310x Series

5x7 mm, 3.3/2.5/1.8 Volt, PECL/LVDS/CML, VCXO

- Featuring *QiK Chip™* Technology
- Superior Jitter Performance (comparable to SAW based)
- APR of ±50 or ±100ppm over industrial temperature range
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

Phase Lock Loop Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

Ordering Information

M310 0 6 A G P N 00.0000 MHz

Product Series

Supply Voltage
- **0:** 3.3 V **1:** 2.5 V
- **2:** 1.8 V

Temperature Range
- **2:** -40°C to +85°C (see note 1)
- **6:** -20°C to +70°C

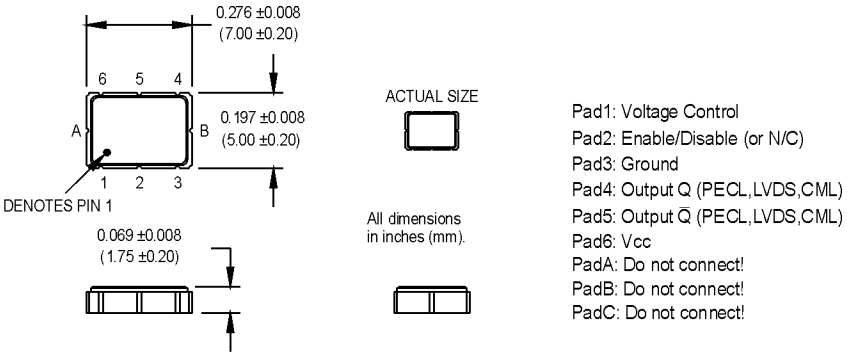
Absolute Pull Range (APR)
- **A:** ±50 ppm **B:** ±100 ppm

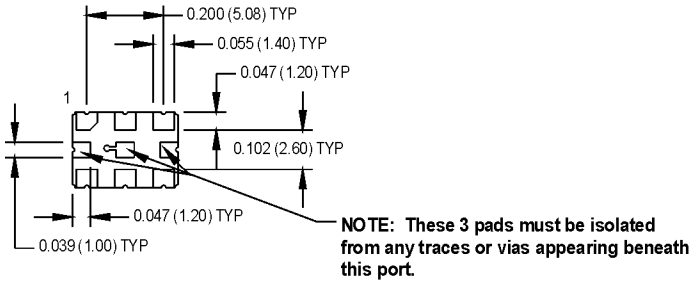
Enable/Disable
- **G:** Complementary Enable High (Pad 2)
- **M:** Complementary Enable Low (Pad 2)
- **U:** Complementary Output

Logic Type
- **P:** PECL **L:** LVDS
- **M:** CML

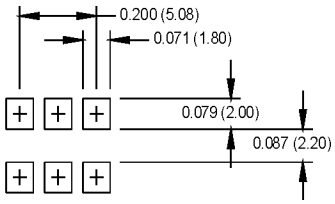
Package/Lead Configuration
- **N:** 5x7 mm Leadless

Frequency (customer specified)





SUGGESTED SOLDER PAD LAYOUT



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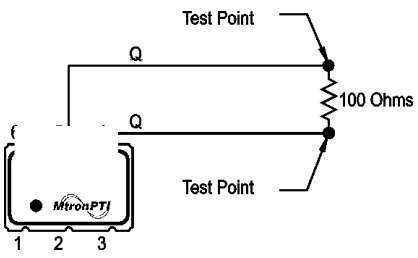
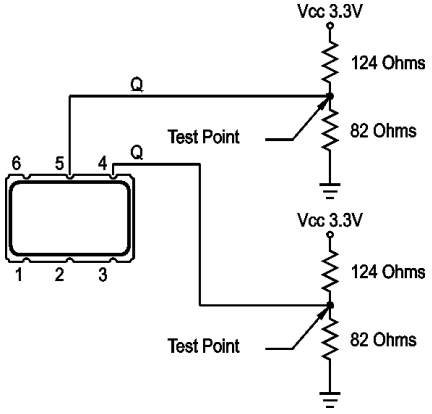
Electrical Specifications	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
	Frequency Range	F	150		1400	MHz	See Note 2
	Operating Temperature	TA	(See ordering information)				See Note 1
	Storage Temperature	TS	-55		+125	°C	
	Frequency Stability	ΔF/F		±25		ppm	
	Aging 1st Year Thereafter (per year)		 -3 -1		 +3 +1	 ppm ppm	
	Pullability/APR		(See ordering information)				See Note 3
	Control Voltage	Vc	0.18 0.25 0.30	0.90 1.25 1.65	1.62 2.25 3.0	V V V	@ 1.8V Vcc @ 2.5V Vcc @ 3.3V Vcc
	Linearity			1	5	%	Positive Monotonic
	Modulation Bandwidth	fm	20			KHz	-3 dB bandwidth
	Input Impedance	Zin	500k	1M		Ohms	@ DC
	Supply Voltage	Vcc	1.71	1.8	1.89	V	
			2.375	2.5	2.625	V	
			3.135	3.3	3.465	V	
	Input Current	Icc			125	mA	PECL/LVDS/CML
	Load		50 Ohms to (Vcc –2) Vdc 100 Ohm differential load				See Note 4 PECL Waveform LVDS/CML Waveform
	Symmetry (Duty Cycle)		45		55	%	@ 50% of waveform
	Output Skew			TBD			
	Differential Voltage		350	425 TBD	500	mVppd	LVDS CML
	Common Mode Output Voltage	Vcm		1.2		V	LVDS
	Logic "1" Level	Voh	Vcc -1.02			V	LVPECL
	Logic "0" Level	Vol			Vcc -1.63	V	LVPECL
	Rise/Fall Time	Tr/Tf		0.23	0.50	ns	@ 20/80% LVPECL
	Enable Function		80% Vcc min. or N/C: output active 20% Vcc max: output disables to high-Z				Output Option G
			20% Vcc max: output active 80% Vcc min: output disables to high-Z				Output Option M
	Start up Time			10		ms	
	Phase Jitter @ 622.08 MHz	 ϕJ		 0.50		 ps RMS	 Integrated 12 kHz – 20 MHz

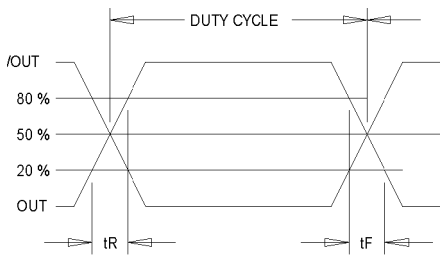
Note 1: If the device is powered up below -20°C and then the ambient temperature rises 105°C during normal operation, the output will be interrupted for approximately 2-3 ms. A correction is in process an will be available Q1 2007
Note 2: Contact factory for exact frequency availability over 945 MHz.
Note 3: APR specification is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.
Note 4: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.



LVDS Load Circuit



3.3V LVPECL Load Circuit



Output Waveform: LVDS/CML/PECL