

# 3806 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

## DESCRIPTION

The 3806 group is 8-bit microcomputer based on the 740 family core technology.

The 3806 group is designed for controlling systems that require analog signal processing and include two serial I/O functions, A-D converters, and D-A converters.

The various microcomputers in the 3806 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3806 group, refer to the section on group expansion.

## FEATURES

- Basic machine-language instructions ..... 71
- Memory size
  - ROM ..... 12 K to 48 K bytes
  - RAM ..... 384 to 1024 bytes
- Programmable input/output ports ..... 72
- Interrupts ..... 16 sources, 16 vectors
- Timers ..... 8 bit X 4
- Serial I/O1 ..... 8-bit X 1 (UART or Clock-synchronized)
- Serial I/O2 ..... 8-bit X 1 (Clock-synchronized)
- A-D converter ..... 8-bit X 8 channels
- D-A converter ..... 8-bit X 2 channels

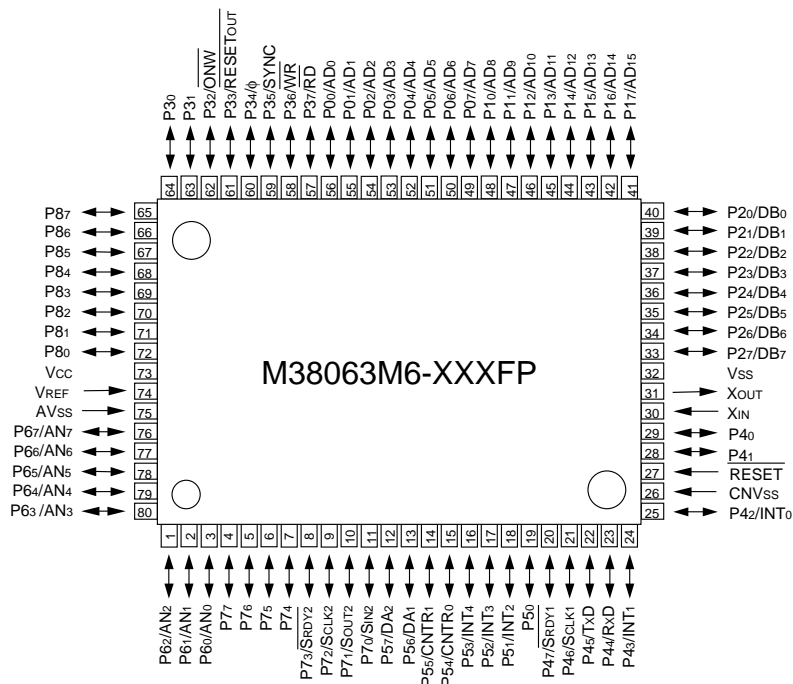
- Clock generating circuit ..... Internal feedback resistor (connect to external ceramic resonator or quartz-crystal)
- Memory expansion possible

Specification (unit)	Standard	Extended operating temperature version	High-speed version
Minimum instruction execution time (μs)	0.5	0.5	0.4
Oscillation frequency (MHz)	8	8	10
Power source voltage (V)	3.0 to 5.5	4.0 to 5.5	2.7 to 5.5
Power dissipation (mW)	32	32	40
Operating temperature range (°C)	-20 to 85	-40 to 85	-20 to 85

## APPLICATIONS

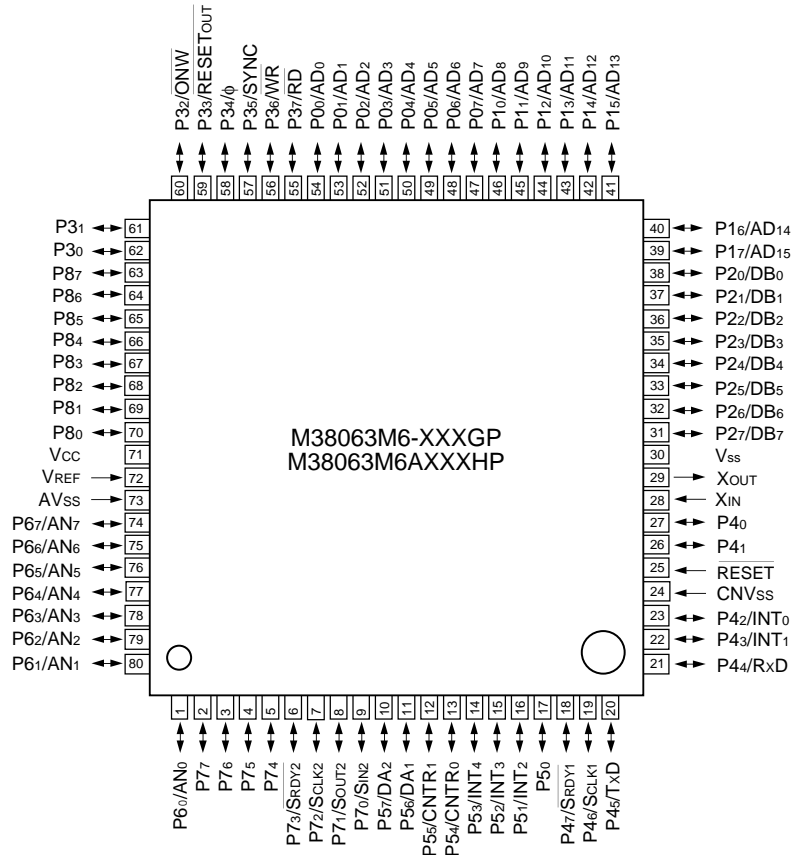
Office automation, VCRs, tuners, musical instruments, cameras, air conditioners, etc.

## PIN CONFIGURATION (TOP VIEW)



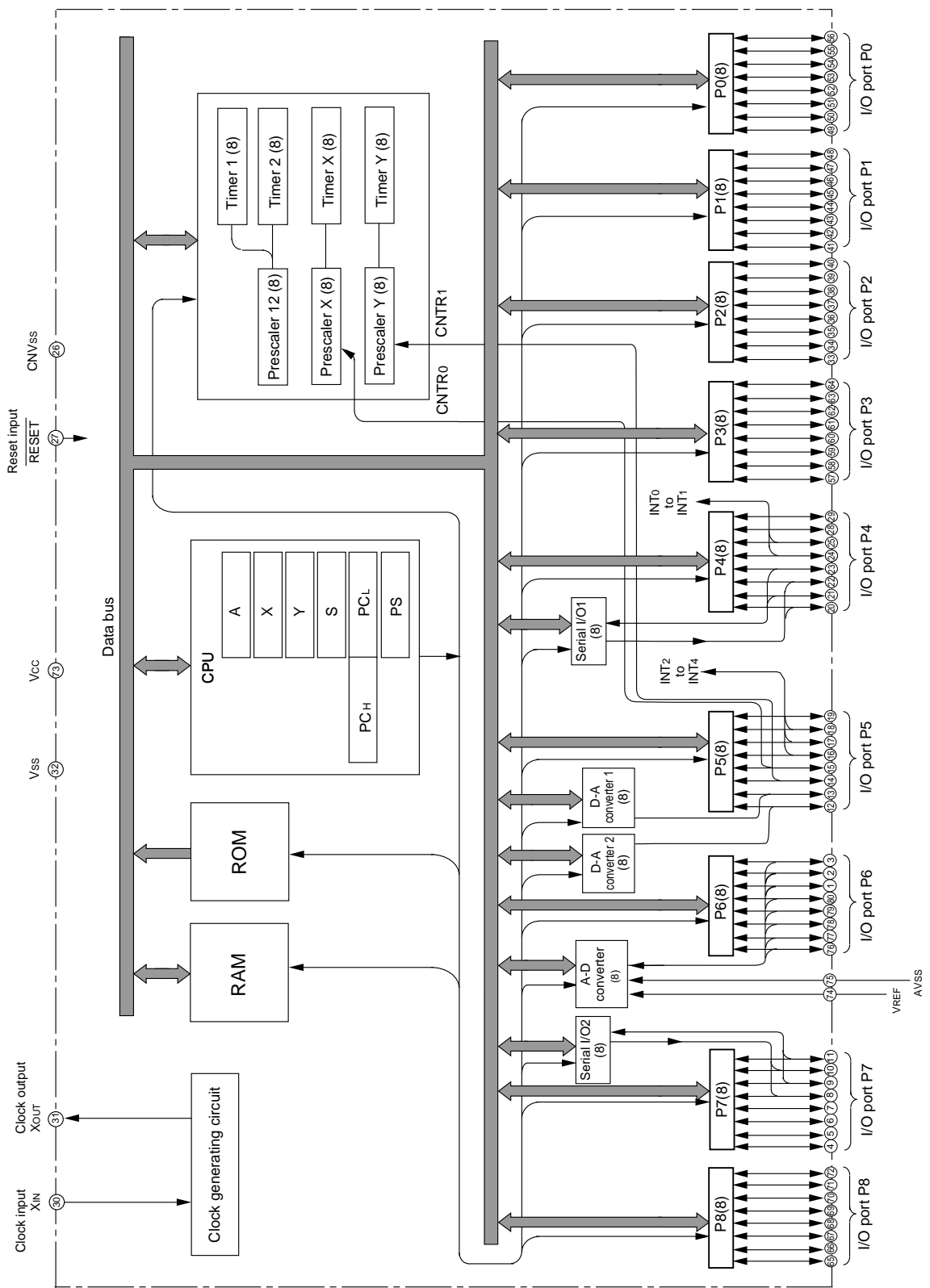
Package type : 80P6N-A  
80-pin plastic-molded QFP

**PIN CONFIGURATION (TOP VIEW)**



**Package type : 80P6S-A/80P6D-A  
80-pin plastic-molded QFP**

FUNCTIONAL BLOCK DIAGRAM (Package : 80P6N)



**PIN DESCRIPTION**

Pin	Name	Function	Function except a port function
Vcc	Power source	<ul style="list-style-type: none"> <li>Apply voltage of 3.0 V to 5.5 V to Vcc, and 0 V to Vss. (Extended operating temperature version : 4.0 V to 5.5 V) (High-speed version : 2.7 V to 5.5 V)</li> </ul>	
Vss			
CNVss	CNVss	<ul style="list-style-type: none"> <li>This pin controls the operation mode of the chip.</li> <li>Normally connected to Vss.</li> <li>If this pin is connected to Vcc, the internal ROM is inhibited and external memory is accessed.</li> </ul>	
VREF	Analog reference voltage	<ul style="list-style-type: none"> <li>Reference voltage input pin for A-D and D-A converters</li> </ul>	
AVss	Analog power source	<ul style="list-style-type: none"> <li>GND input pin for A-D and D-A converters</li> <li>Connect to Vss.</li> </ul>	
RESET	Reset input	<ul style="list-style-type: none"> <li>Reset input pin for active "L"</li> </ul>	
XIN	Clock input	<ul style="list-style-type: none"> <li>Input and output signals for the internal clock generating circuit.</li> <li>Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency.</li> <li>If an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.</li> <li>The clock is used as the oscillating source of system clock.</li> </ul>	
XOUT	Clock output		
P00 – P07	I/O port P0	<ul style="list-style-type: none"> <li>8 bit CMOS I/O port</li> <li>I/O direction register allows each pin to be individually programmed as either input or output.</li> <li>At reset this port is set to input mode.</li> <li>In modes other than single-chip, these pins are used as address, data, and control bus I/O pins.</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>	
P10 – P17	I/O port P1		
P20 – P27	I/O port P2		
P30 – P37	I/O port P3		
P40, P41	I/O port P4	<ul style="list-style-type: none"> <li>8-bit CMOS I/O port with the same function as port P0</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>	<ul style="list-style-type: none"> <li>External interrupt input pin</li> </ul>
P42/INT0, P43/INT1			
P44/RxD, P45/TxD, P46/SCLK1, P47/SRDY1			<ul style="list-style-type: none"> <li>Serial I/O1 I/O pins</li> </ul>
P50	I/O port P5	<ul style="list-style-type: none"> <li>8-bit CMOS I/O port with the same function as port P0</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>	<ul style="list-style-type: none"> <li>External interrupt input pin</li> </ul>
P51/INT2 – P53/INT4			
P54/CNTR0, P55/CNTR1			<ul style="list-style-type: none"> <li>Timer X and Timer Y I/O pins</li> </ul>
P56/DA1, P57/DA2			<ul style="list-style-type: none"> <li>D-A conversion output pins</li> </ul>
P60/AN0 – P67/AN7	I/O port P6	<ul style="list-style-type: none"> <li>8-bit CMOS I/O port with the same function as port P0</li> <li>CMOS compatible input level</li> <li>CMOS 3-state output structure</li> </ul>	<ul style="list-style-type: none"> <li>A-D conversion input pins</li> </ul>

**PIN DESCRIPTION (Continued)**

Pin	Name	Function	Function except a port function
P70/SIN2, P71/SOUT2, P72/SCLK2, P73/SRDY2	I/O port P7	<ul style="list-style-type: none"> <li>• 8-bit I/O port with the same function as port P0</li> <li>• CMOS compatible input level</li> <li>• N-channel open-drain output structure</li> </ul>	<ul style="list-style-type: none"> <li>• Serial I/O2 I/O pins</li> </ul>
P74 – P77			
P80 – P87	I/O port P8	<ul style="list-style-type: none"> <li>• 8-bit CMOS I/O port with the same function as port P0</li> <li>• CMOS compatible input level</li> <li>• CMOS 3-state output structure</li> </ul>	

**PART NUMBERING**

Product M3806 **3** **M** **6** - **XXX** **FP**

**Package type**  
 FP : 80P6N-A package  
 GP : 80P6S-A package  
 FS : 80D0 package

**ROM number**  
 Omitted in some types.

**Normally, using hyphen**  
 When electrical characteristic, or division of quality identification code using alphanumeric character  
 - : standard  
 D : Extended operating temperature version  
 A : High-speed version

**ROM/PROM size**  
 1 : 4096 bytes  
 2 : 8192 bytes  
 3 : 12288 bytes  
 4 : 16384 bytes  
 5 : 20480 bytes  
 6 : 24576 bytes  
 7 : 28672 bytes  
 8 : 32768 bytes  
 9 : 36864 bytes  
 A : 40960 bytes  
 B : 45056 bytes  
 C : 49152 bytes  
 D : 53248 bytes  
 E : 57344 bytes  
 F : 61440 bytes

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

**Memory type**  
 M : Mask ROM version  
 E : EPROM or One Time PROM version

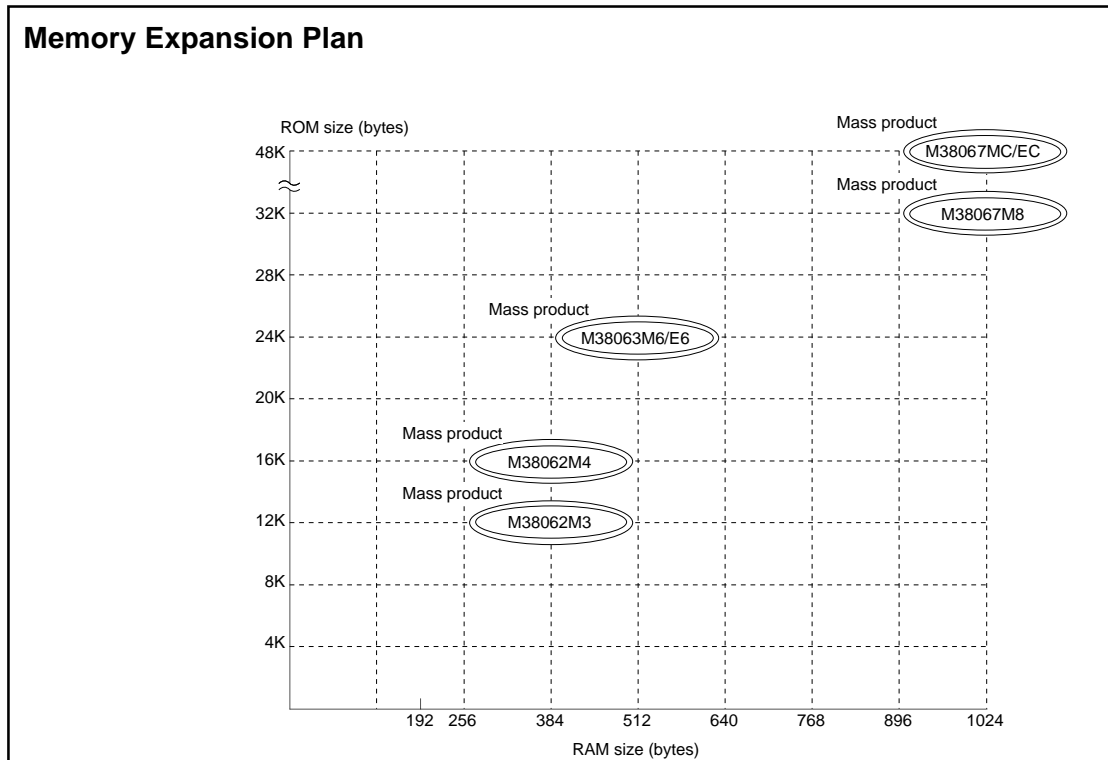
**RAM size**  
 0 : 192 bytes  
 1 : 256 bytes  
 2 : 384 bytes  
 3 : 512 bytes  
 4 : 640 bytes  
 5 : 768 bytes  
 6 : 896 bytes  
 7 : 1024 bytes

**GROUP EXPANSION**

Mitsubishi plans to expand the 3806 group as follows:

- (1) Support for mask ROM, One Time PROM, and EPROM versions
  - ROM/PROM capacity ..... 12 K to 48 K bytes
  - RAM capacity ..... 384 to 1024 bytes

- (2) Packages
  - 80P6N-A ..... 0.8 mm-pitch plastic molded QFP
  - 80P6S-A ..... 0.65 mm-pitch plastic molded QFP
  - 80D0 ..... 0.8 mm-pitch ceramic LCC (EPROM version)



Products under development : the development schedule and specification may be revised without notice.

Currently supported products are listed below

As of May 1996

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks		
M38062M3-XXXFP	12288	384	80P6N-A	Mask ROM version		
M38062M3-XXXGP	(12158)		80P6S-A	Mask ROM version		
M38062M4-XXXFP	16384	384	80P6N-A	Mask ROM version		
M38062M4-XXXGP	(16254)		80P6S-A	Mask ROM version		
M38063M6-XXXFP	24576 (24446)	512	80P6N-A	Mask ROM version		
M38063E6-XXXFP				One Time PROM version		
M38063E6FP				One Time PROM version (blank)		
M38063M6-XXXGP			80P6S-A	Mask ROM version		
M38063E6-XXXGP				One Time PROM version		
M38063E6GP				One Time PROM version (blank)		
M38063E6FS				80D0	EPROM version	
M38067M8-XXXFP			32768	1024	80P6N-A	Mask ROM version
M38067M8-XXXGP			(32638)		80P6S-A	Mask ROM version
M38067MC-XXXFP			49152 (49022)	1024	80P6N-A	Mask ROM version
M38067EC-XXXFP	One Time PROM version					
M38067ECFP	One Time PROM version (blank)					
M38067MC-XXXGP	80P6S-A	Mask ROM version				
M38067EC-XXXGP		One Time PROM version				
M38067ECGP		One Time PROM version (blank)				

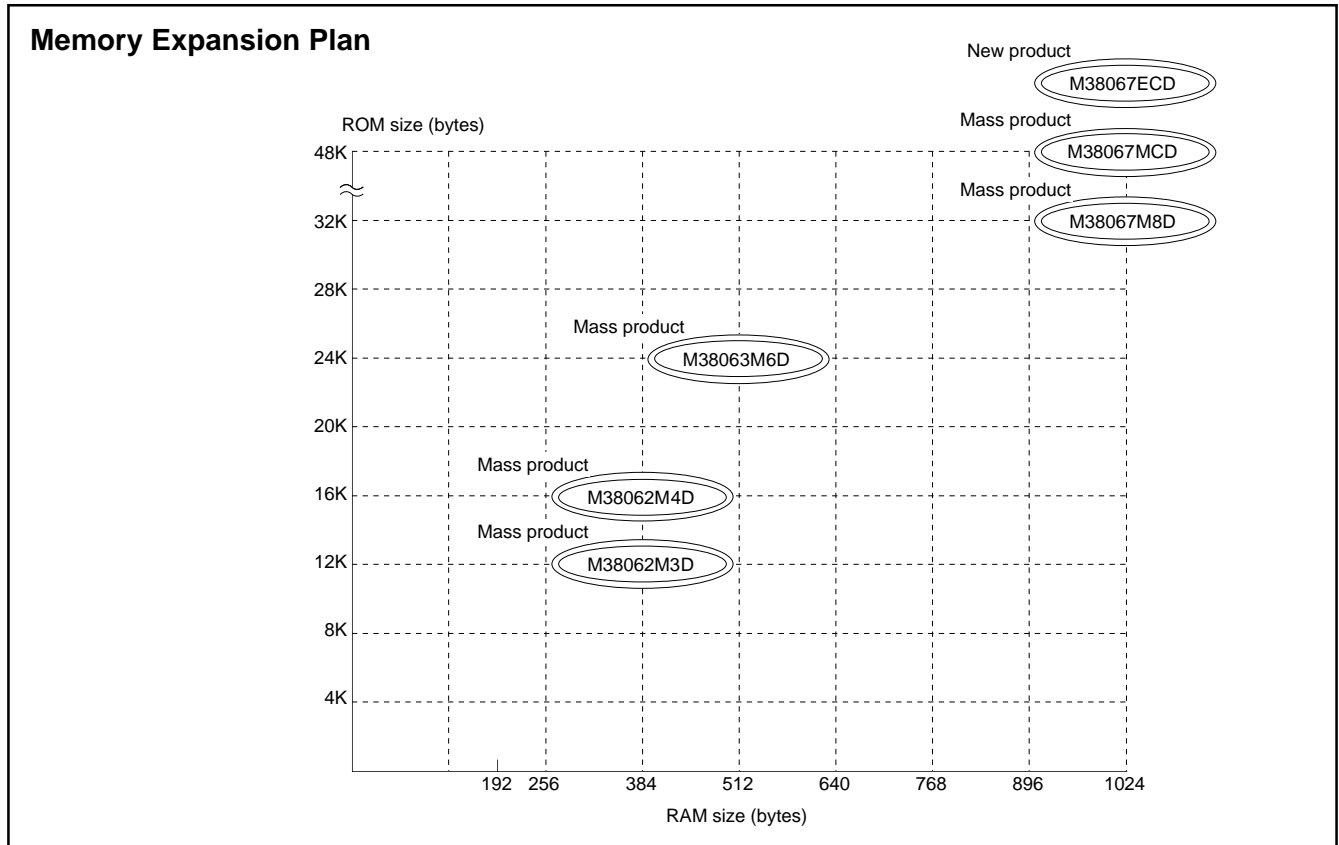
**GROUP EXPANSION**

**(EXTENDED OPERATING TEMPERATURE VERSION)**

Mitsubishi plans to expand the 3806 group (extended operating temperature version) as follows:

- (1) Support for mask ROM version
  - ROM/PROM capacity ..... 12 K to 48 K bytes
  - RAM capacity ..... 384 to 1024 bytes

- (2) Packages
  - 80P6N-A ..... 0.8 mm-pitch plastic molded QFP



Currently supported products are listed below.

As of May 1996

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38062M3DXXXFP	12288(12158)	384	80P6N-A	Mask ROM version
M38062M4DXXXFP	16384(16254)	384		Mask ROM version
M38063M6DXXXFP	24576(24446)	512		Mask ROM version
M38067M8DXXXFP	32768(32638)	1024		Mask ROM version
M38067MCDXXXFP	49152(49022)	1024		Mask ROM version
M38067ECDXXXFP				One Time PROM version
M38067ECDFP				One Time PROM version (blank)

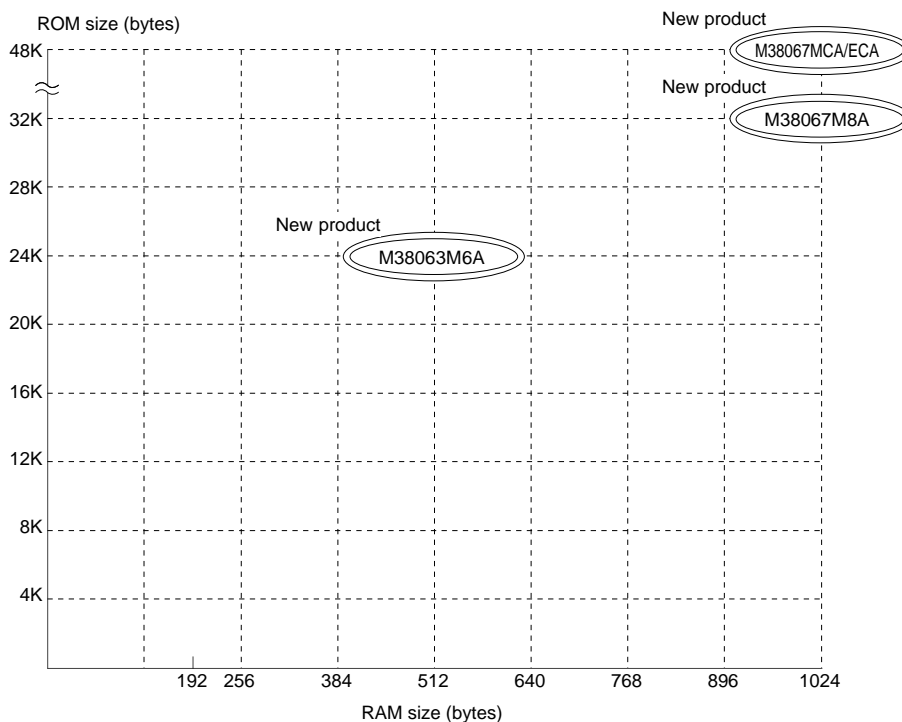
**GROUP EXPANSION  
(HIGH-SPEED VERSION)**

Mitsubishi plans to expand the 3806 group (high-speed version) as follows:

- (1) Support for mask ROM, One Time PROM, and EPROM versions
  - ROM/PROM capacity ..... 24 K to 48 K bytes
  - RAM capacity ..... 512 to 1024 bytes

- (2) Packages
  - 80P6N-A ..... 0.8 mm-pitch plastic molded QFP
  - 80P6S-A ..... 0.65 mm-pitch plastic molded QFP
  - 80P6D-A ..... 0.5 mm-pitch plastic molded QFP
  - 80D0 ..... 0.8 mm-pitch ceramic LCC (EPROM version)

**Memory Expansion Plan**



Products under development: the development schedule and specification may be revised without notice.

Currently supported products are listed below.

As of May 1996

Product name	(P) ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks	
M38063M6AXXFP	24576 (24446)	512	80P6N-A	Mask ROM version	
M38063M6AXXGP			80P6S-A	Mask ROM version	
M38063M6AXXHP			80P6D-A	Mask ROM version	
M38067M8AXXFP	32768 (32638)	1024	80P6N-A	Mask ROM version	
M38067M8AXXGP			80P6S-A	Mask ROM version	
M38067MCAAXXFP	49152 (49022)	1024	80P6N-A	Mask ROM version	
M38067ECAAXXFP				One Time PROM version	
M38067ECAFP				One Time PROM version (blank)	
M38067MCAAXXGP			80P6S-A	Mask ROM version	
M38067ECAAXXGP				One Time PROM version	
M38067ECAGP				One Time PROM version (blank)	
M38067ECAF5				80D0	EPROM version



**FUNCTIONAL DESCRIPTION**  
**Central Processing Unit (CPU)**

The 3806 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

- The FST and SLW instruction cannot be used.
- The STP, WIT, MUL, and DIV instruction can be used.

**CPU mode register**

The CPU mode register is allocated at address 003B16.  
 The CPU mode register contains the stack page selection bit.

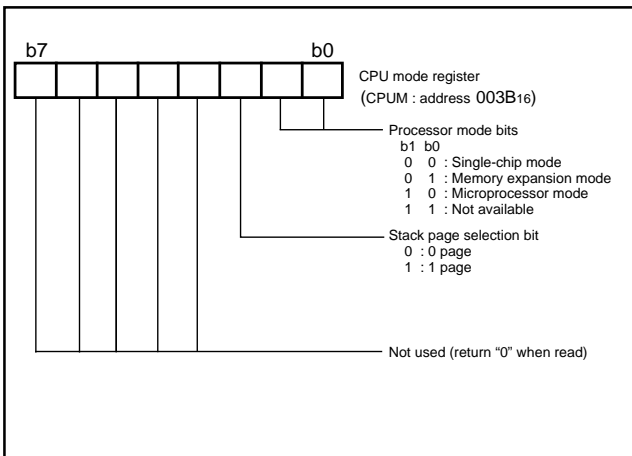


Fig. 1 Structure of CPU mode register

**Memory**

**Special function register (SFR) area**

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

**RAM**

RAM is used for data storage and for stack area of subroutine calls and interrupts.

**ROM**

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

**Interrupt vector area**

The interrupt vector area contains reset and interrupt vectors.

**Zero page**

The 256 bytes from addresses 0000<sub>16</sub> to 00FF<sub>16</sub> are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

**Special page**

The 256 bytes from addresses FF00<sub>16</sub> to FFFF<sub>16</sub> are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

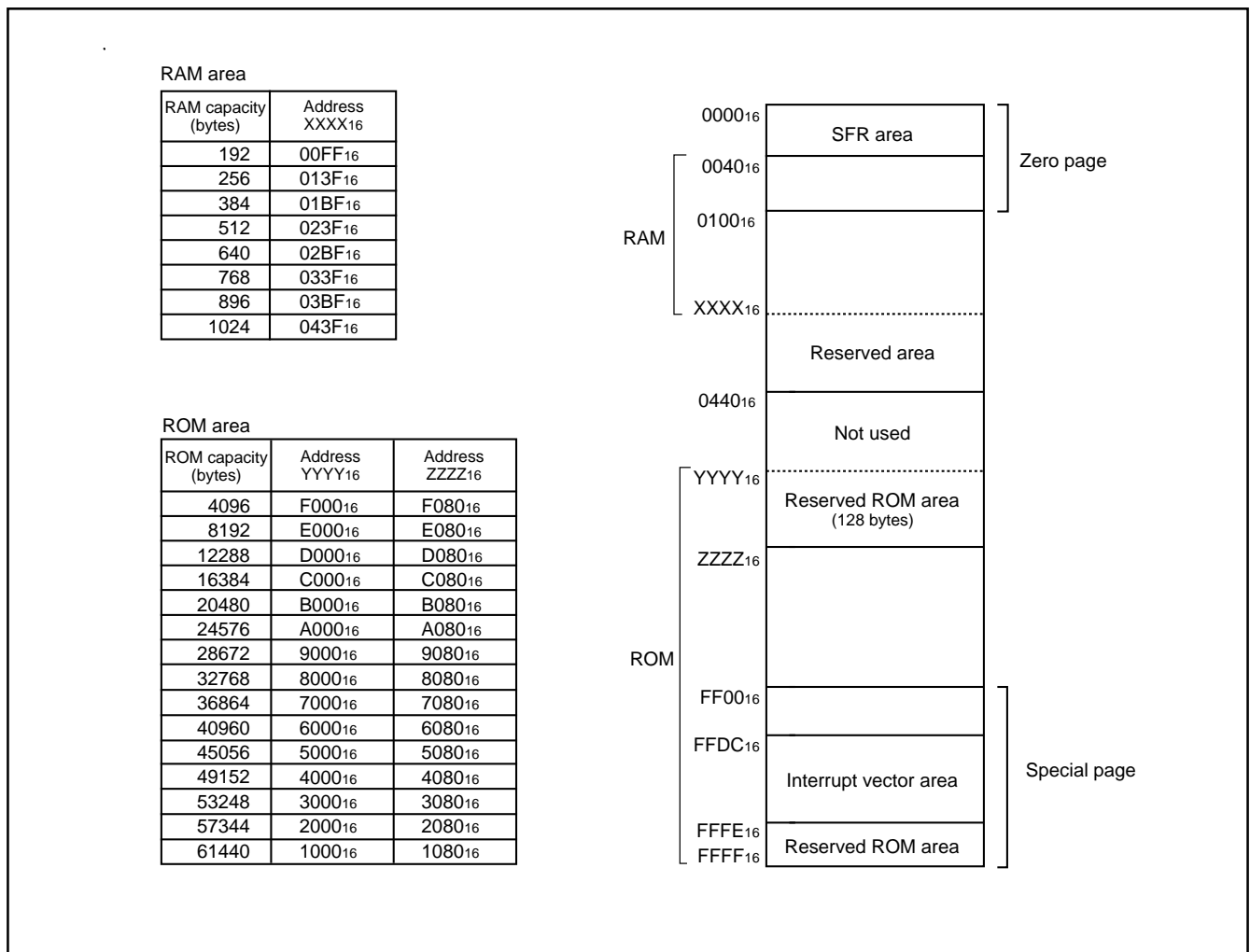


Fig. 2 Memory map diagram

0000 <sub>16</sub>	Port P0 (P0)	0020 <sub>16</sub>	Prescaler 12 (PRE12)
0001 <sub>16</sub>	Port P0 direction register (P0D)	0021 <sub>16</sub>	Timer 1 (T1)
0002 <sub>16</sub>	Port P1 (P1)	0022 <sub>16</sub>	Timer 2 (T2)
0003 <sub>16</sub>	Port P1 direction register (P1D)	0023 <sub>16</sub>	Timer XY mode register (TM)
0004 <sub>16</sub>	Port P2 (P2)	0024 <sub>16</sub>	Prescaler X (PREX)
0005 <sub>16</sub>	Port P2 direction register (P2D)	0025 <sub>16</sub>	Timer X (TX)
0006 <sub>16</sub>	Port P3 (P3)	0026 <sub>16</sub>	Prescaler Y (PREY)
0007 <sub>16</sub>	Port P3 direction register (P3D)	0027 <sub>16</sub>	Timer Y (TY)
0008 <sub>16</sub>	Port P4 (P4)	0028 <sub>16</sub>	
0009 <sub>16</sub>	Port P4 direction register (P4D)	0029 <sub>16</sub>	
000A <sub>16</sub>	Port P5 (P5)	002A <sub>16</sub>	
000B <sub>16</sub>	Port P5 direction register (P5D)	002B <sub>16</sub>	
000C <sub>16</sub>	Port P6 (P6)	002C <sub>16</sub>	
000D <sub>16</sub>	Port P6 direction register (P6D)	002D <sub>16</sub>	
000E <sub>16</sub>	Port P7 (P7)	002E <sub>16</sub>	
000F <sub>16</sub>	Port P7 direction register (P7D)	002F <sub>16</sub>	
0010 <sub>16</sub>	Port P8 (P8)	0030 <sub>16</sub>	
0011 <sub>16</sub>	Port P8 direction register (P8D)	0031 <sub>16</sub>	
0012 <sub>16</sub>		0032 <sub>16</sub>	
0013 <sub>16</sub>		0033 <sub>16</sub>	
0014 <sub>16</sub>		0034 <sub>16</sub>	AD/DA control register (ADCON)
0015 <sub>16</sub>		0035 <sub>16</sub>	A-D conversion register (AD)
0016 <sub>16</sub>		0036 <sub>16</sub>	D-A1 conversion register (DA1)
0017 <sub>16</sub>		0037 <sub>16</sub>	D-A2 conversion register (DA2)
0018 <sub>16</sub>	Transmit/Receive buffer register (TB/RB)	0038 <sub>16</sub>	
0019 <sub>16</sub>	Serial I/O1 status register (SIO1STS)	0039 <sub>16</sub>	
001A <sub>16</sub>	Serial I/O1 control register (SIO1CON)	003A <sub>16</sub>	Interrupt edge selection register (INTEDGE)
001B <sub>16</sub>	UART control register (UARTCON)	003B <sub>16</sub>	CPU mode register (CPUM)
001C <sub>16</sub>	Baud rate generator (BRG)	003C <sub>16</sub>	Interrupt request register 1(IREQ1)
001D <sub>16</sub>	Serial I/O2 control register (SIO2CON)	003D <sub>16</sub>	Interrupt request register 2(IREQ2)
001E <sub>16</sub>		003E <sub>16</sub>	Interrupt control register 1(ICON1)
001F <sub>16</sub>	Serial I/O2 register (SIO2)	003F <sub>16</sub>	Interrupt control register 2(ICON2)

Fig. 3 Memory map of special function register (SFR)

**I/O Ports**  
**Direction registers**

The 3806 group has 72 programmable I/O pins arranged in nine I/O ports (ports P0 to P8). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P00 – P07	Port P0	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Address low-order byte output	CPU mode register	(1)
P10 – P17	Port P1	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Address high-order byte output	CPU mode register	
P20 – P27	Port P2	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Data bus I/O	CPU mode register	
P30 – P37	Port P3	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	Control signal I/O	CPU mode register	
P40,P41	Port P4	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	External interrupt input	Interrupt edge selection register	(2)
P42/INT0, P43/INT1				Serial I/O1 function I/O	Serial I/O1 control register UART control register	(3)
P44/RxD, P45/TxD, P46/SCLK1, P47/SRDY1						(4)
						(5)
						(6)
P50	Port P5	Input/output, individual bits	CMOS 3-state output CMOS compatible input level			(1)
P51/INT2, P52/INT3, P53/INT4				External interrupt input	Interrupt edge selection register	(2)
P54/CNTR0, P55/CNTR1				Timer X and Timer Y function I/O	Timer XY mode register	(7)
P56/DA1, P57/DA2				D-A conversion output	AD/DA control register	(8)
P60/AN0 – P67/AN7	Port P6	Input/output, individual bits	CMOS 3-state output CMOS compatible input level	A-D conversion input		(9)
P70/SIN2, P71/SOUT2, P72/SCLK2, P73/SRDY2	Port P7	Input/output, individual bits	N-channel open-drain output CMOS compatible input level	Serial I/O2 function I/O	Serial I/O2 control register	(10)
P74 – P77						(11)
						(12)
						(13)
						(14)
P80 – P87	Port P8	Input/output, individual bits	CMOS 3-state output CMOS compatible input level			(1)

**Note 1:** For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, refer to the applicable sections.

**2:** Make sure that the input level at each pin is either 0 V or V<sub>CC</sub> during execution of the STP instruction.  
When an input level is at an intermediate potential, a current will flow from V<sub>CC</sub> to V<sub>SS</sub> through the input-stage gate.

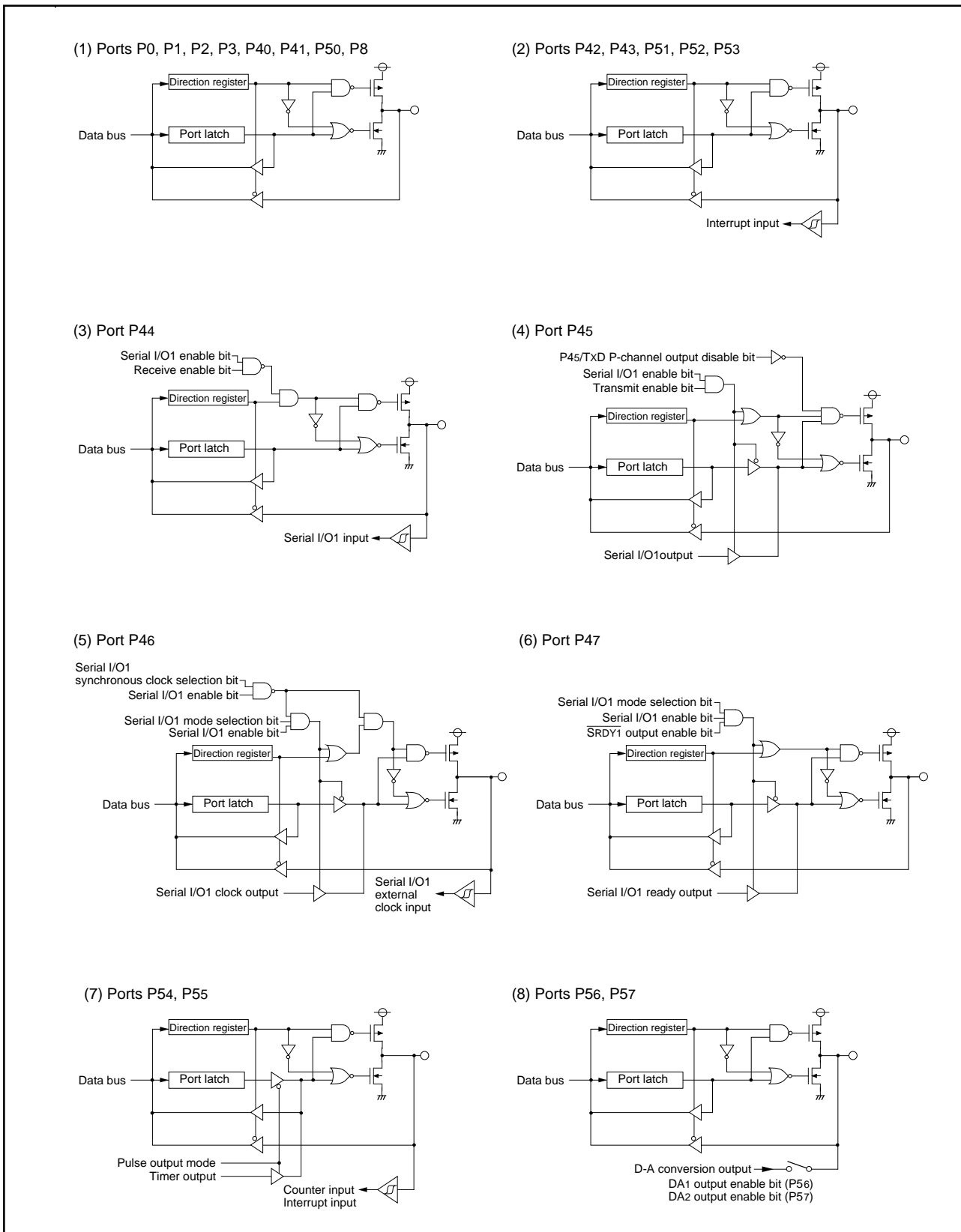


Fig. 4 Port block diagram (single-chip mode) (1)

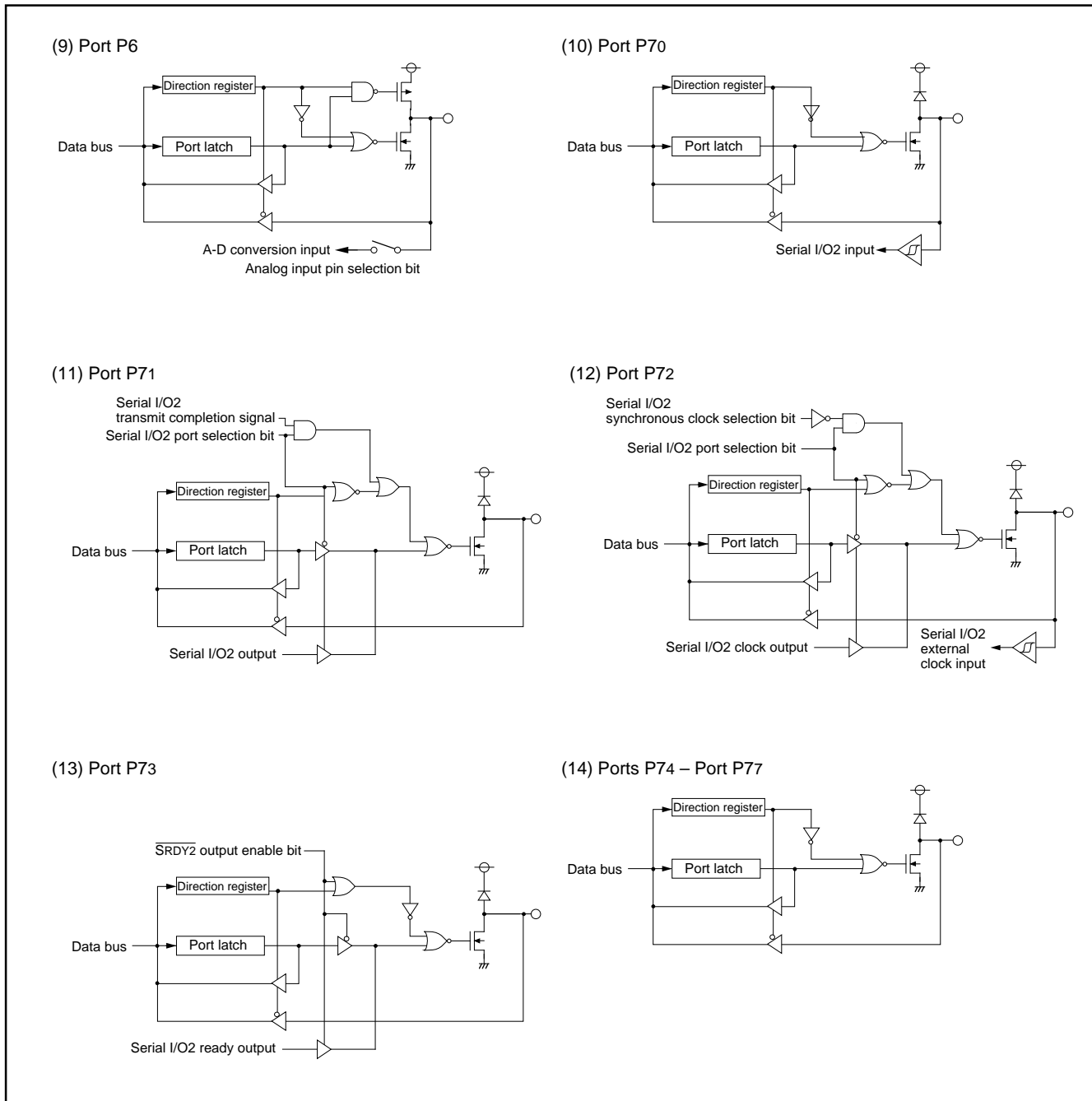


Fig. 5 Port block diagram (single-chip mode) (2)

## INTERRUPTS

Interrupts occur by sixteen sources: seven external, eight internal, and one software.

### Interrupt control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

### Interrupt operation

When an interrupt is received, the contents of the program counter and processor status register are automatically stored into the stack. The interrupt disable flag is set to inhibit other interrupts from interfering. The corresponding interrupt request bit is cleared and the interrupt jump destination address is read from the vector table into the program counter.

### Notes on use

When the active edge of an external interrupt (INT0 to INT4, CNTR0, or CNTR1) is changed, the corresponding interrupt request bit may also be set. Therefore, please take following sequence;

- (1) Disable the external interrupt which is selected.
- (2) Change the active edge selection.
- (3) Clear the interrupt request bit which is selected to "0".
- (4) Enable the external interrupt which is selected.

Table 1. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD <sub>16</sub>	FFFC <sub>16</sub>	At reset	Non-maskable
INT <sub>0</sub>	2	FFFB <sub>16</sub>	FFFA <sub>16</sub>	At detection of either rising or falling edge of INT <sub>0</sub> input	External interrupt (active edge selectable)
INT <sub>1</sub>	3	FFF9 <sub>16</sub>	FFF8 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>1</sub> input	External interrupt (active edge selectable)
Serial I/O1 reception	4	FFF7 <sub>16</sub>	FFF6 <sub>16</sub>	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	FFF5 <sub>16</sub>	FFF4 <sub>16</sub>	At completion of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	FFF3 <sub>16</sub>	FFF2 <sub>16</sub>	At timer X underflow	
Timer Y	7	FFF1 <sub>16</sub>	FFF0 <sub>16</sub>	At timer Y underflow	
Timer 1	8	FFEF <sub>16</sub>	FFEE <sub>16</sub>	At timer 1 underflow	STP release timer underflow
Timer 2	9	FFED <sub>16</sub>	FFEC <sub>16</sub>	At timer 2 underflow	
CNTR <sub>0</sub>	10	FFEB <sub>16</sub>	FFEA <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>0</sub> input	External interrupt (active edge selectable)
CNTR <sub>1</sub>	11	FFE9 <sub>16</sub>	FFE8 <sub>16</sub>	At detection of either rising or falling edge of CNTR <sub>1</sub> input	External interrupt (active edge selectable)
Serial I/O2	12	FFE7 <sub>16</sub>	FFE6 <sub>16</sub>	At completion of serial I/O2 data transfer	Valid when serial I/O2 is selected
INT <sub>2</sub>	13	FFE5 <sub>16</sub>	FFE4 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>2</sub> input	External interrupt (active edge selectable)
INT <sub>3</sub>	14	FFE3 <sub>16</sub>	FFE2 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>3</sub> input	External interrupt (active edge selectable)
INT <sub>4</sub>	15	FFE1 <sub>16</sub>	FFE0 <sub>16</sub>	At detection of either rising or falling edge of INT <sub>4</sub> input	External interrupt (active edge selectable)
A-D converter	16	FFDF <sub>16</sub>	FFDE <sub>16</sub>	At completion of A-D conversion	
BRK instruction	17	FFDD <sub>16</sub>	FFDC <sub>16</sub>	At BRK instruction execution	Non-maskable software interrupt

Note 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

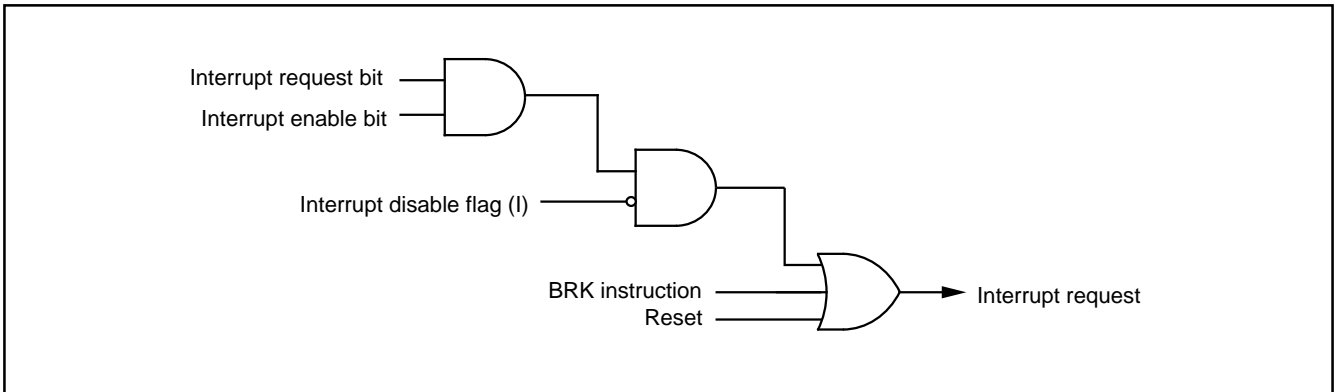


Fig. 6 Interrupt control

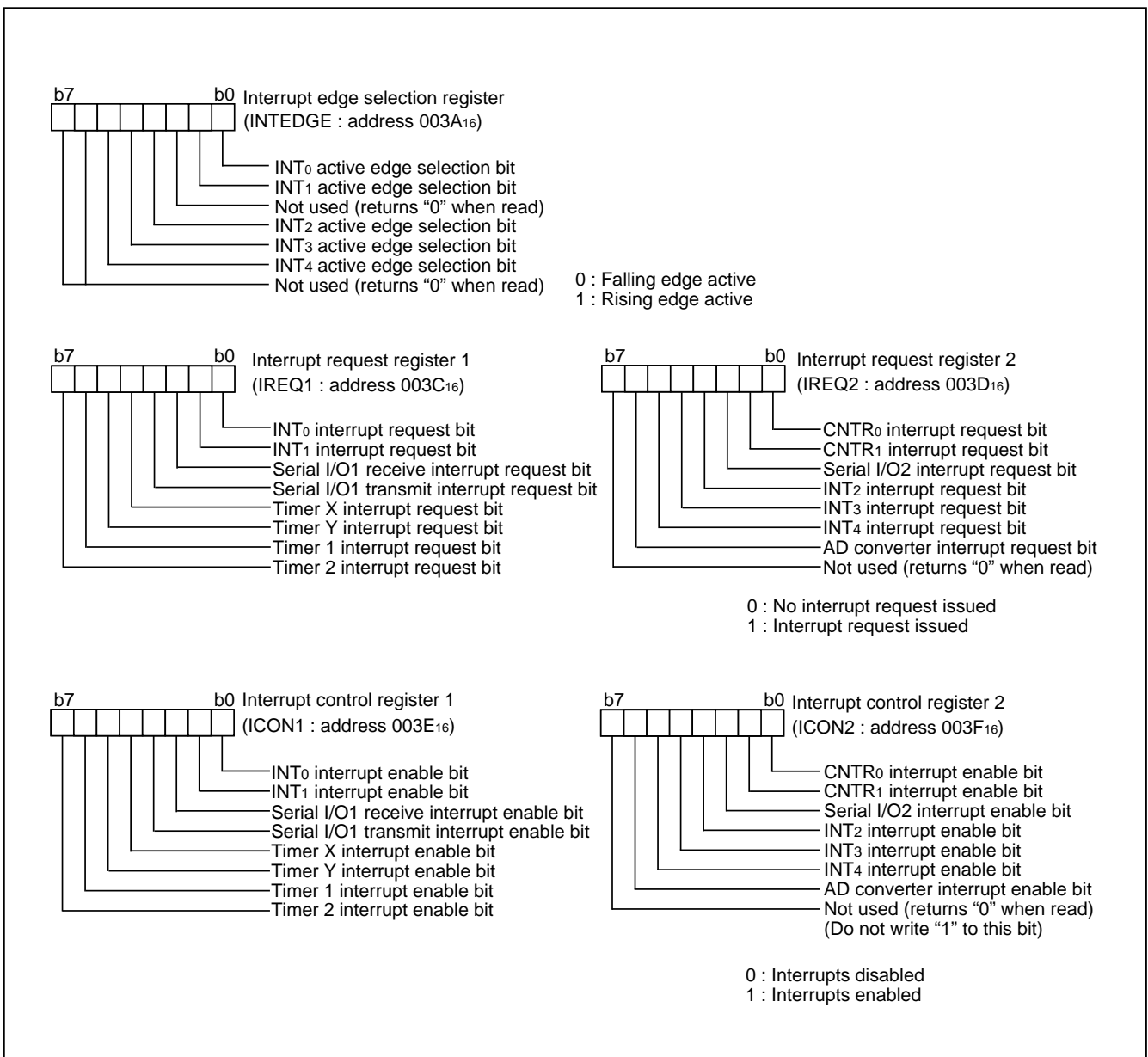


Fig. 7 Structure of interrupt-related registers



**Timers**

The 3806 group has four timers: timer X, timer Y, timer 1, and timer 2.

All timers are count down. When the timer reaches "0016", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

The division ratio of each timer or prescaler is given by  $1/(n + 1)$ , where n is the value in the corresponding timer or prescaler latch.

**Timer 1 and Timer 2**

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

**Timer X and Timer Y**

Timer X and Timer Y can each be selected in one of four operating modes by setting the timer XY mode register.

**Timer Mode**

The timer counts  $f(XIN)/16$  in timer mode.

**Pulse Output Mode**

Timer X (or timer Y) counts  $f(XIN)/16$ . Whenever the contents of the timer reach "0016", the signal output from the CNTR0 (or CNTR1) pin is inverted. If the CNTR0 (or CNTR1) active edge switch bit is "0", output begins at "H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port P54 ( or port P55) direction register to output mode.

**Event Counter Mode**

Operation in event counter mode is the same as in timer mode, except the timer counts signals input through the CNTR0 or CNTR1 pin.

**Pulse Width Measurement Mode**

If the CNTR0 (or CNTR1) active edge selection bit is "0", the timer counts at the oscillation frequency divided by 16 while the CNTR0 (or CNTR1) pin is at "H". If the CNTR0 (or CNTR1) active edge switch bit is "1", the count continues during the time that the CNTR0 (or CNTR1) pin is at "L".

In all of these modes, the count can be stopped by setting the timer X (timer Y) count stop bit to "1". Every time a timer underflows, the corresponding interrupt request bit is set.

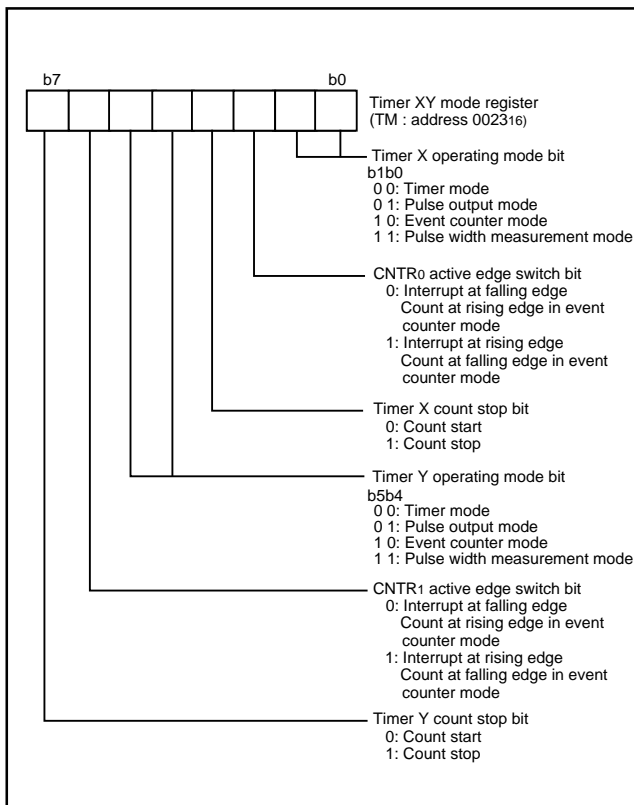


Fig. 8 Structure of timer XY register

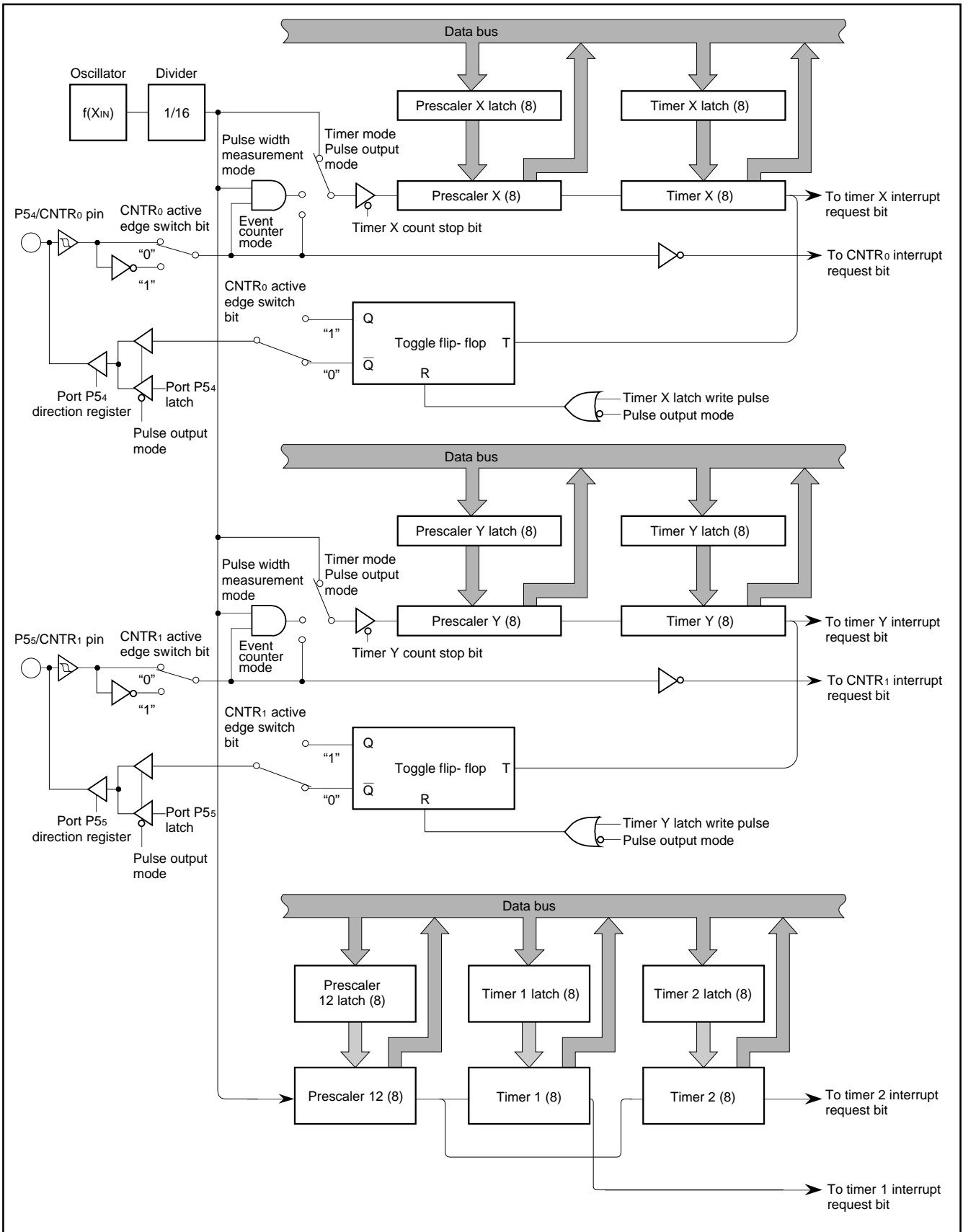


Fig. 9 Block diagram of timer X, timer Y, timer 1, and timer 2

**Serial I/O1**

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

**Clock synchronous serial I/O mode**

Clock synchronous serial I/O1 mode can be selected by setting the mode selection bit of the serial I/O1 control register to "1". For clock synchronous serial I/O1, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB (address 0018<sub>16</sub>).

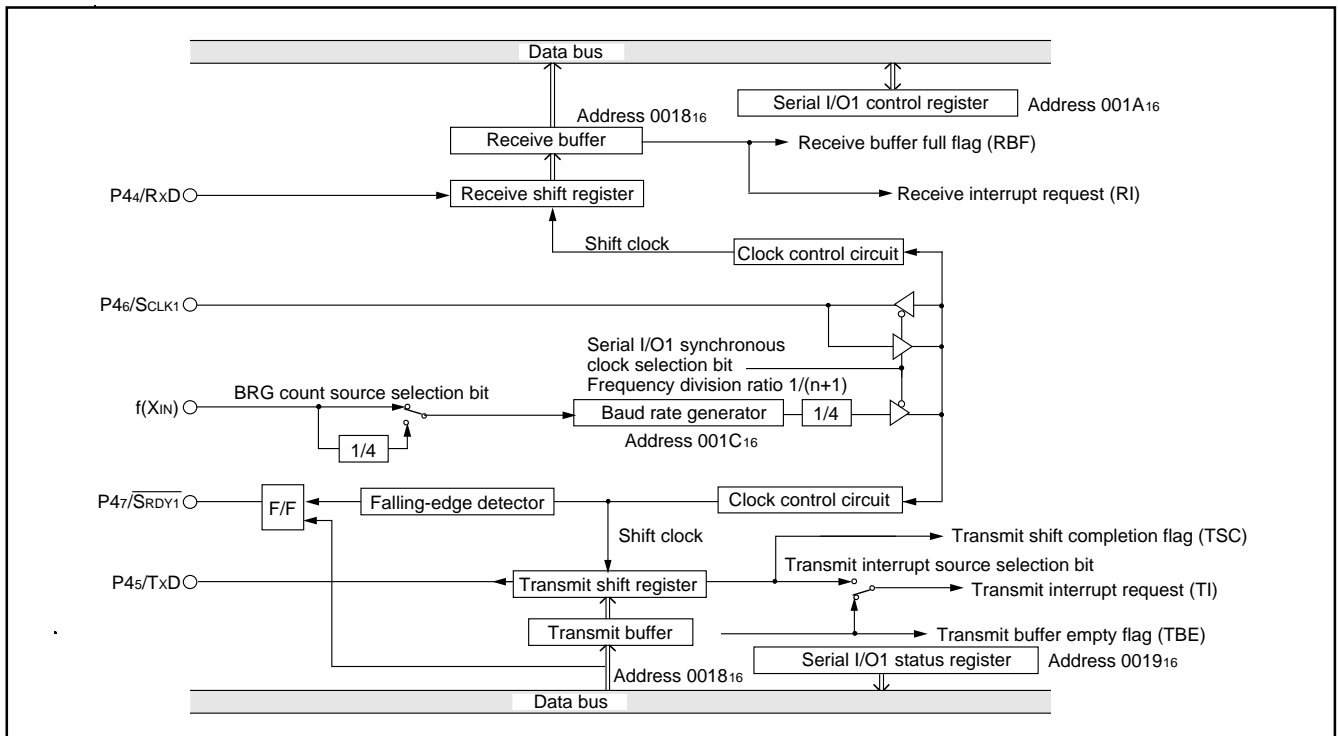


Fig. 10 Block diagram of clock synchronous serial I/O1

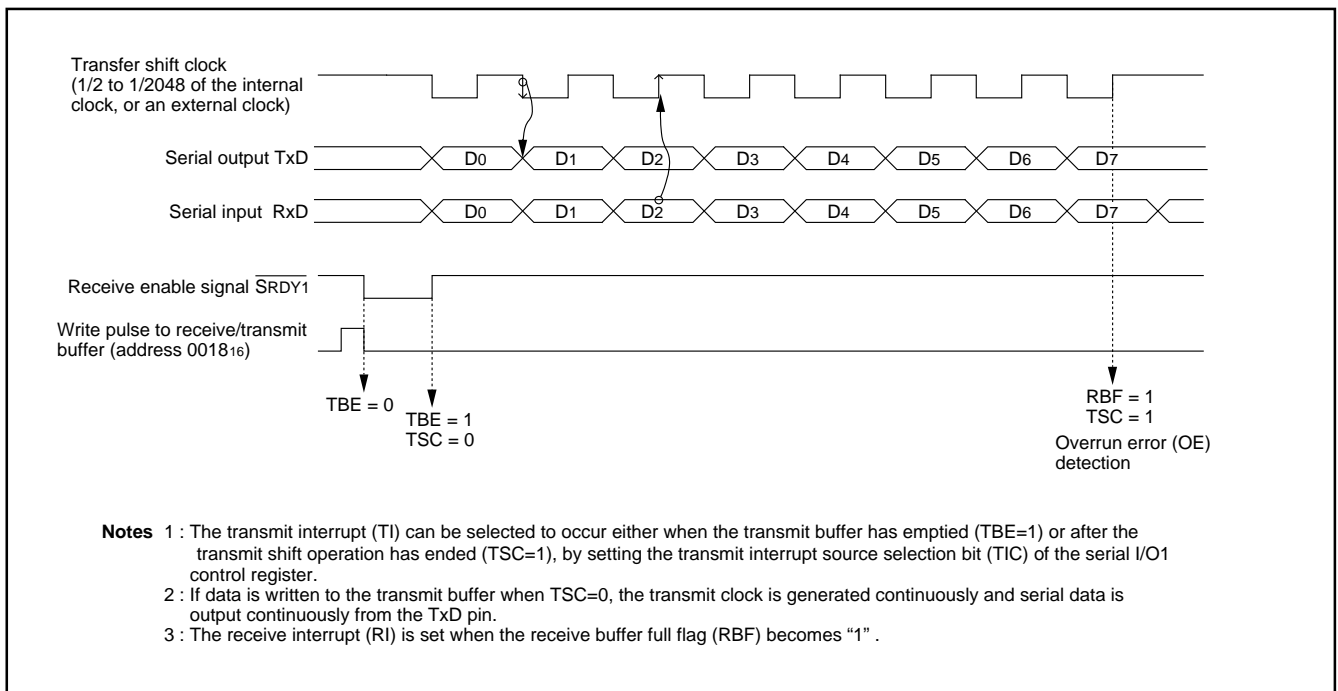


Fig. 11 Operation of clock synchronous serial I/O1 function

### Asynchronous serial I/O (UART) mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O mode selection bit of the serial I/O control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

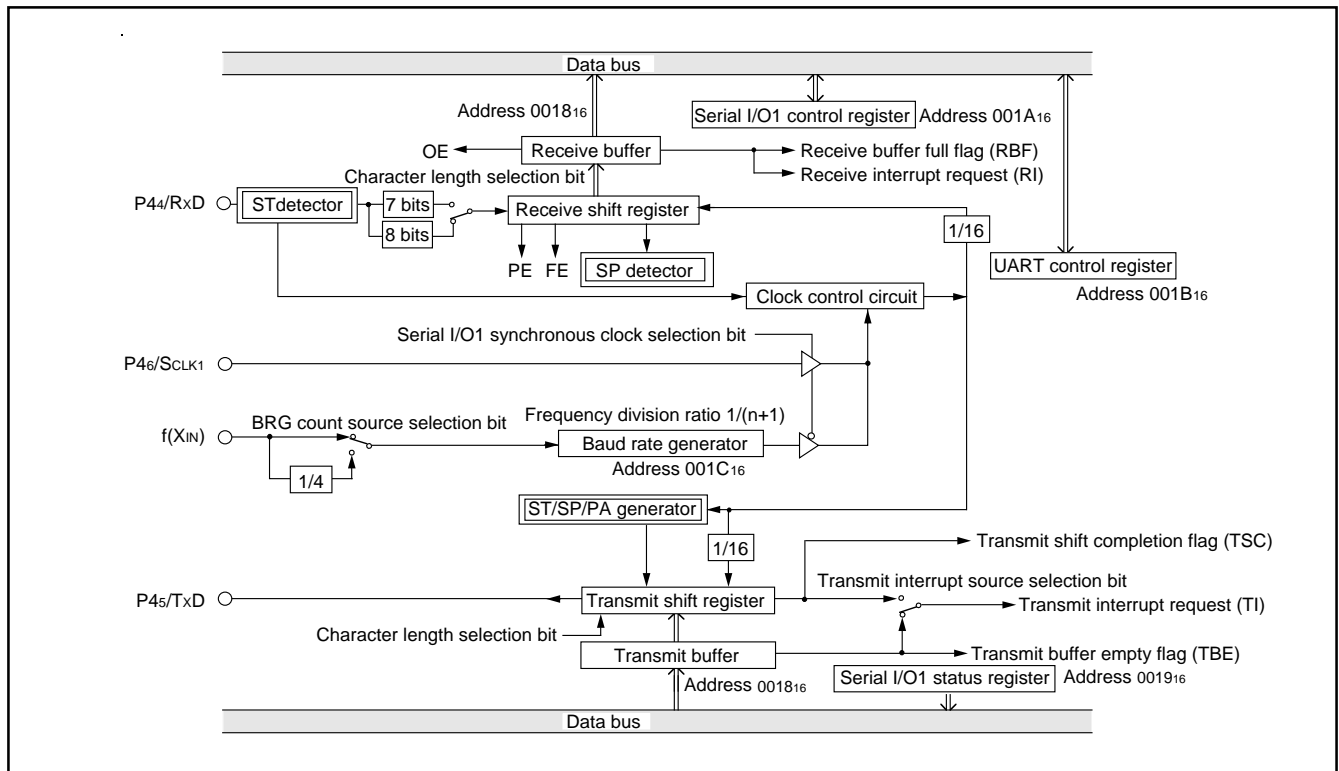


Fig. 12 Block diagram of UART serial I/O

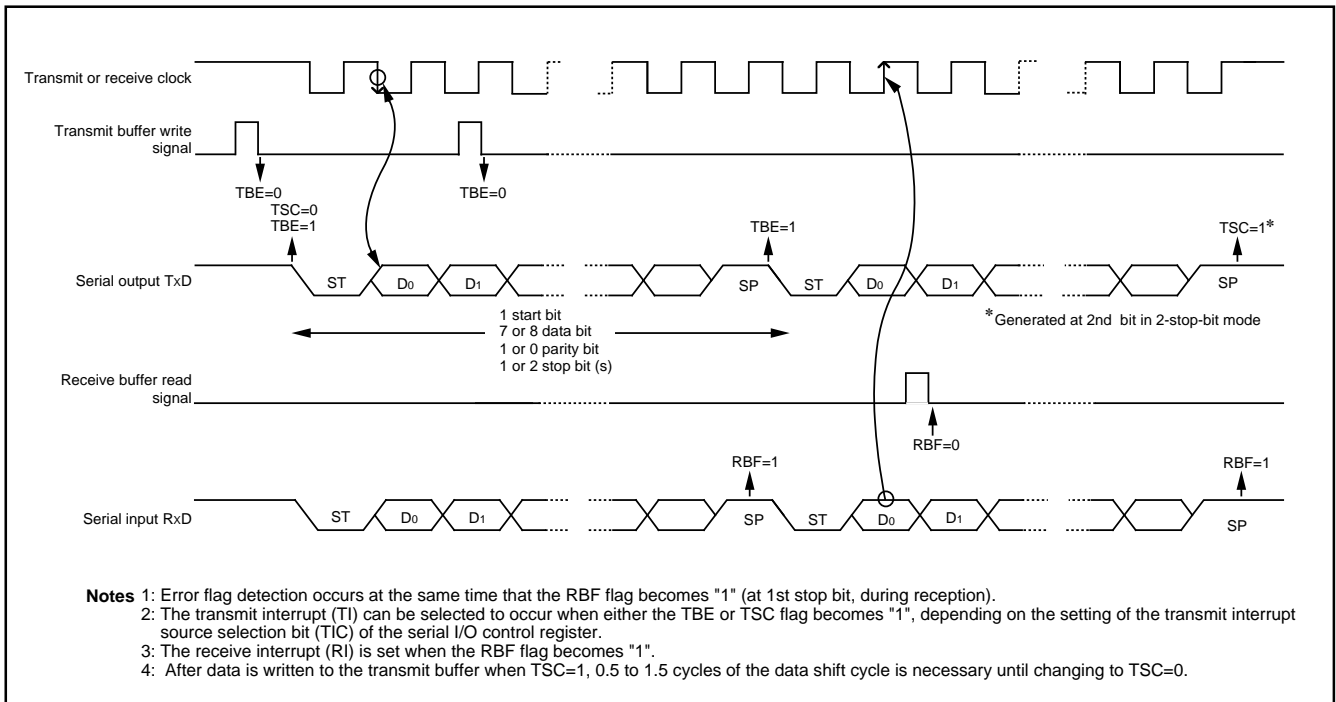


Fig. 13 Operation of UART serial I/O function

**Serial I/O1 control register (SIO1CON) 001A16**

The serial I/O control register consists of eight control bits for the serial I/O function.

**UART control register (UARTCON) 001B16**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (bit 4) is always valid and sets the output structure of the P45/TxD pin.

**Serial I/O1 status register (SIO1STS) 001916**

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer, and the receive buffer full flag is set. A write to the serial I/O status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, re-

spectively). Writing "0" to the serial I/O enable bit SIOE (bit 7 of the Serial I/O Control Register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

**Transmit buffer/Receive buffer register (TB/RB) 001816**

The transmit buffer and the receive buffer are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

**Baud rate generator (BRG) 001C16**

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by  $1/(n + 1)$ , where n is the value written to the baud rate generator.

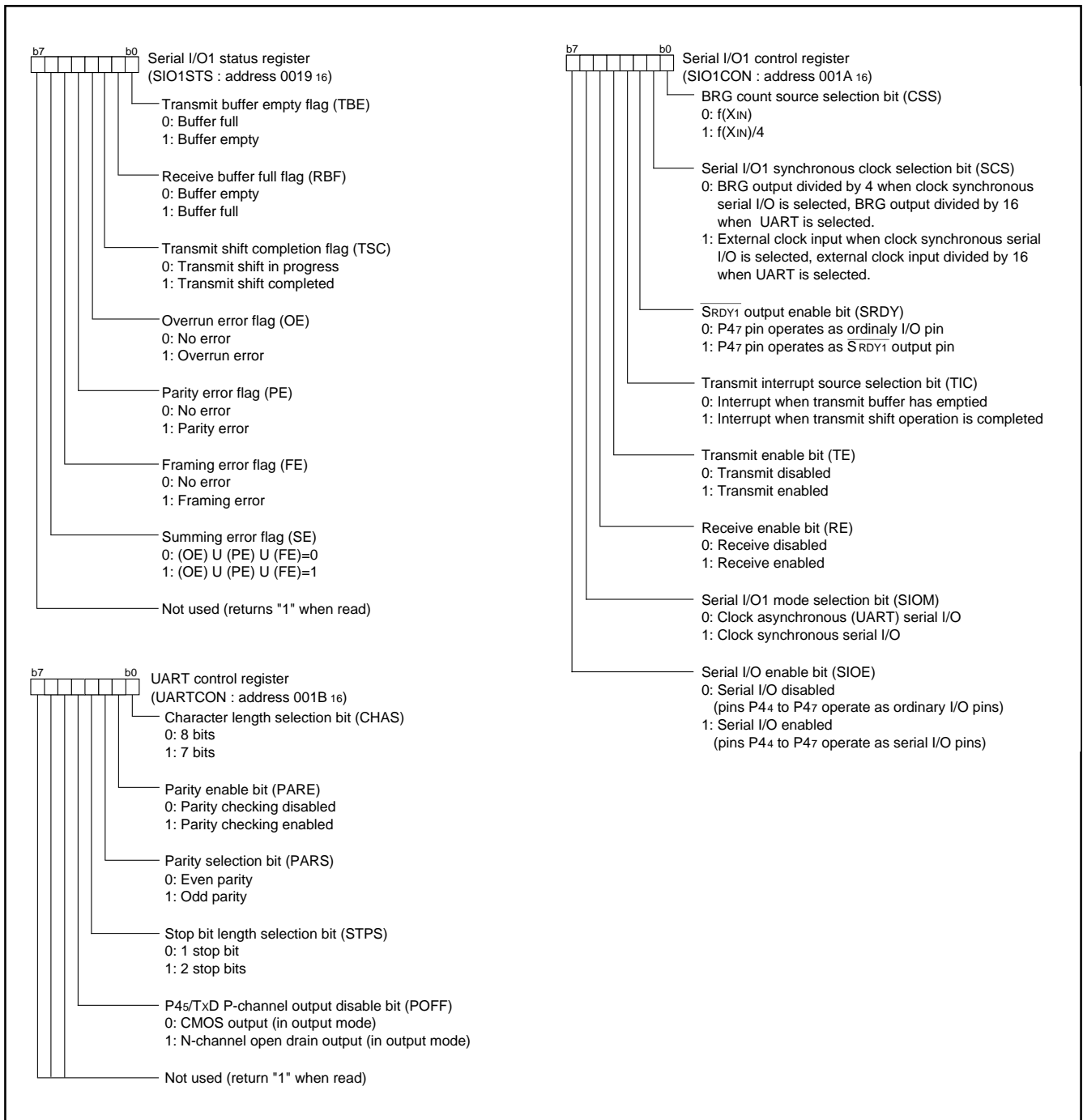


Fig. 14 Structure of serial I/O control registers

**Serial I/O2**

The serial I/O2 function can be used only for clock synchronous serial I/O.

For clock synchronous serial I/O the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

**Serial I/O2 control register (SIO2CON) 001D16**

The serial I/O2 control register contains seven bits which control various serial I/O functions.

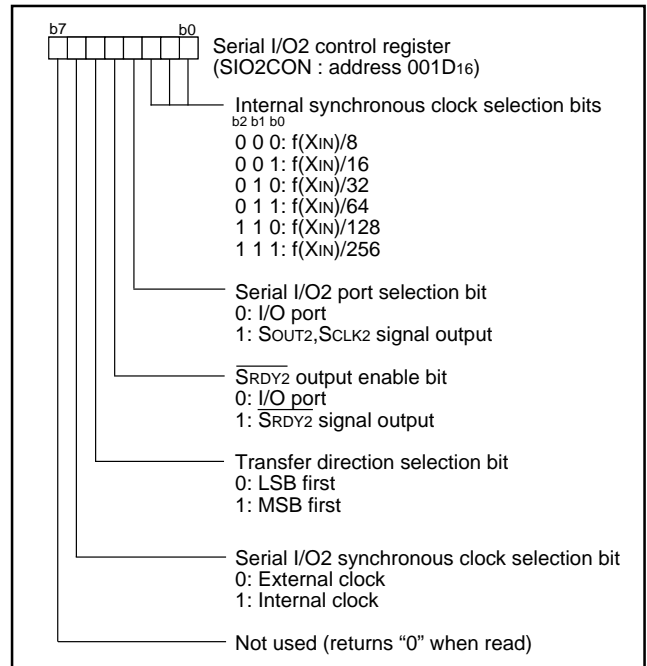


Fig. 15 Structure of serial I/O2 control register

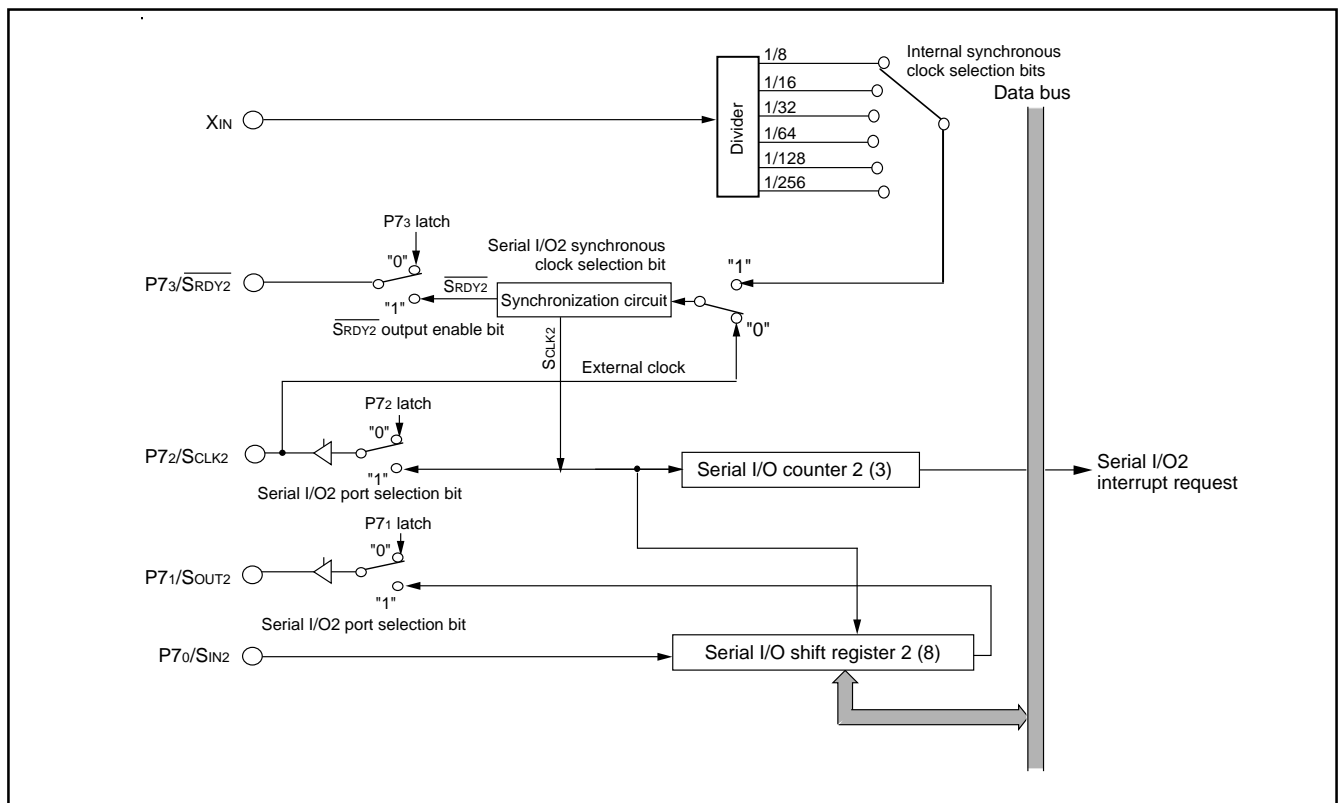


Fig. 16 Block diagram of serial I/O2 function

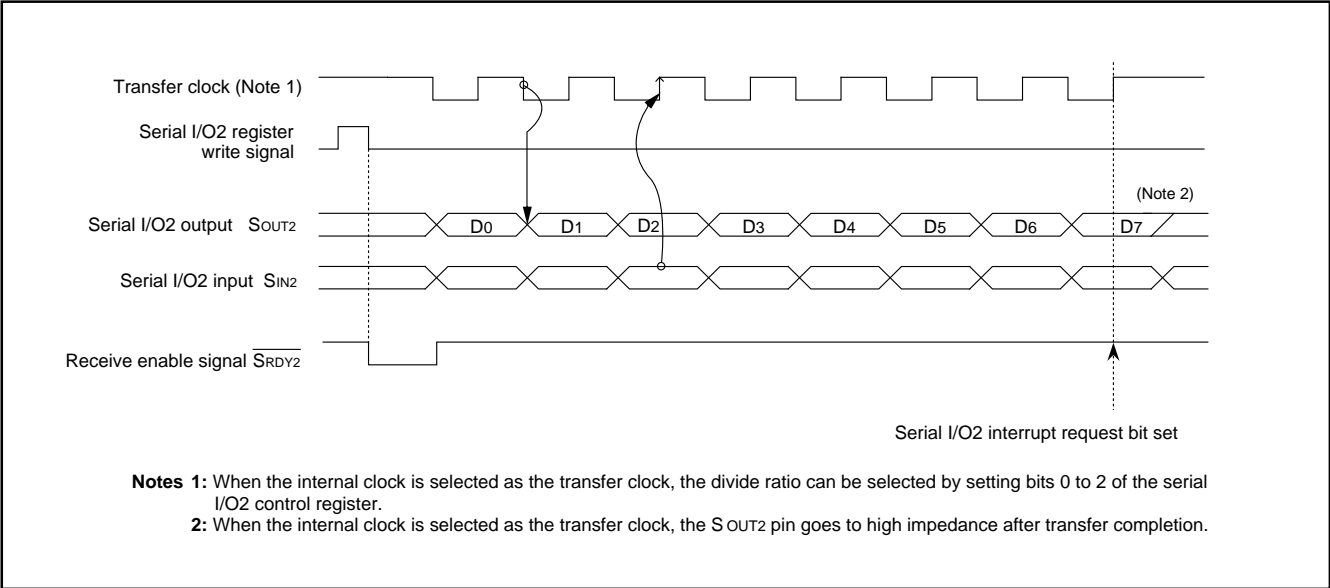


Fig. 17 Timing of serial I/O2 function



**A-D Converter**

The functional blocks of the A-D converter are described below.

**[A-D conversion register]**

The A-D conversion register is a read-only register that stores the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

**[AD/DA control register]**

The AD/DA control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 3 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion. Bits 6 and 7 are used to control the output of the D-A converter.

**[Comparison voltage generator]**

The comparison voltage generator divides the voltage between AVSS and VREF into 256, and outputs the divided voltages.

**[Channel selector]**

The channel selector selects one of the ports P60/AN0 to P67/AN7, and inputs the voltage to the comparator.

**[Comparator and Control circuit]**

The comparator and control circuit compares an analog input voltage with the comparison voltage, then stores the result in the A-D conversion register. When an A-D conversion is complete, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that the comparator is constructed linked to a capacitor, so set f(XIN) to 500 kHz or more during an A-D conversion.

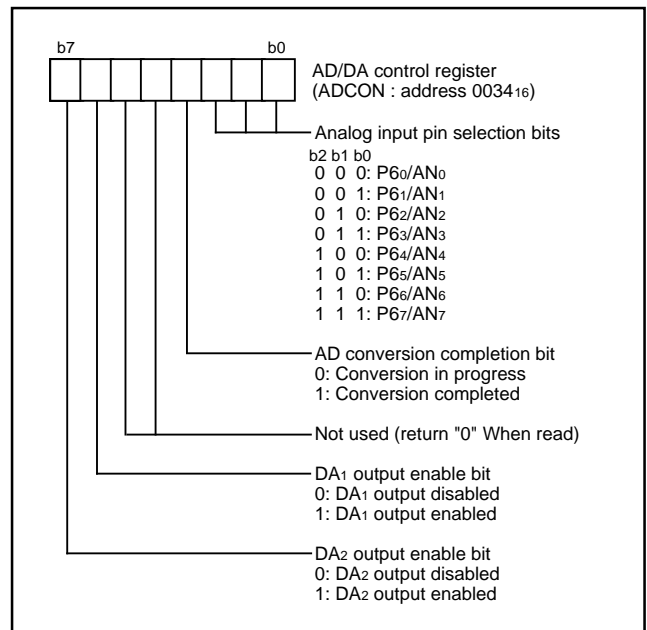


Fig.18 Structure of AD/DA control register

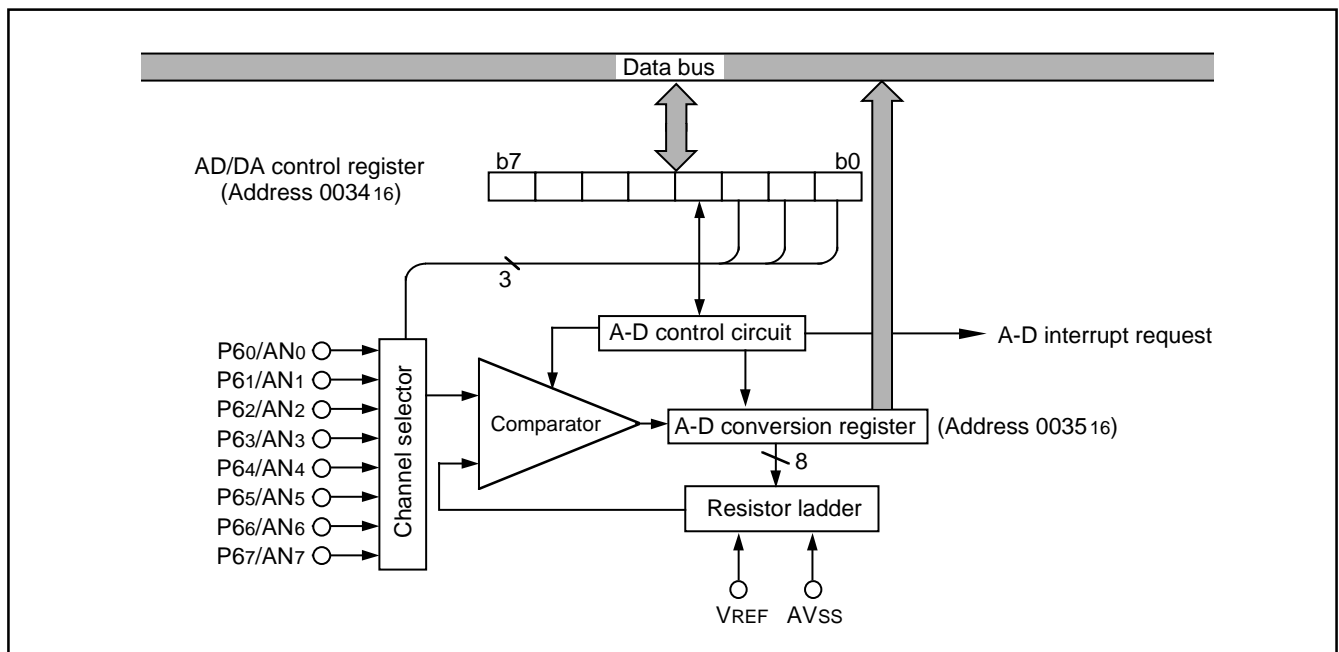


Fig. 19 Block diagram of A-D converter

**D-A Converter**

The 3806 group has two internal D-A converters (DA1 and DA2) with 8-bit resolutions.

The D-A converter is performed by setting the value in the D-A conversion register. The result of D-A converter is output from the DA1 or DA2 pin by setting the DA output enable bit to "1".

When using the D-A converter, the corresponding port direction register bit (DA1/P56 or DA2/P57) should be set to "0" (input status).

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n = 0 \text{ to } 255)$$

Where VREF is the reference voltage.

At reset, the D-A conversion registers are cleared to "0016", the DA output enable bits are cleared to "0", and the P56/DA1 and P57/DA2 pins are set to input (high impedance).

The D-A output is not buffered, so connect an external buffer when driving a low-impedance load.

Set VCC to 4.0 V or more when using the D-A converter.

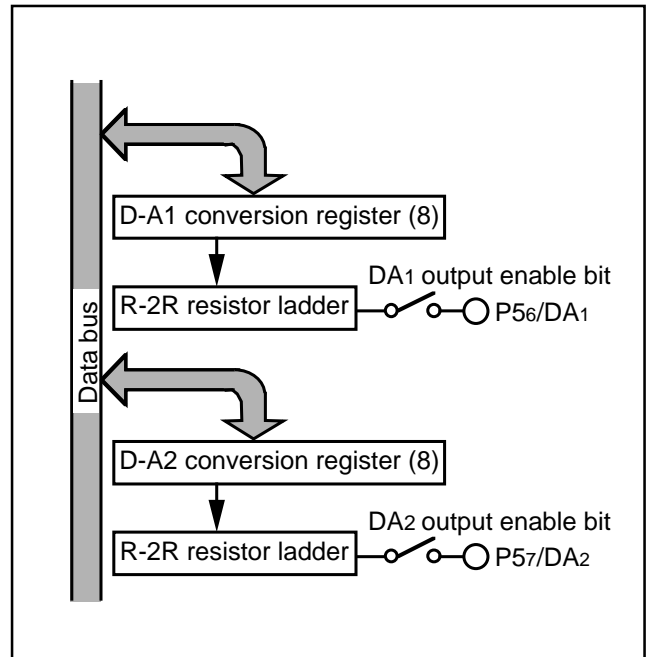


Fig. 20 Block diagram of D-A converter

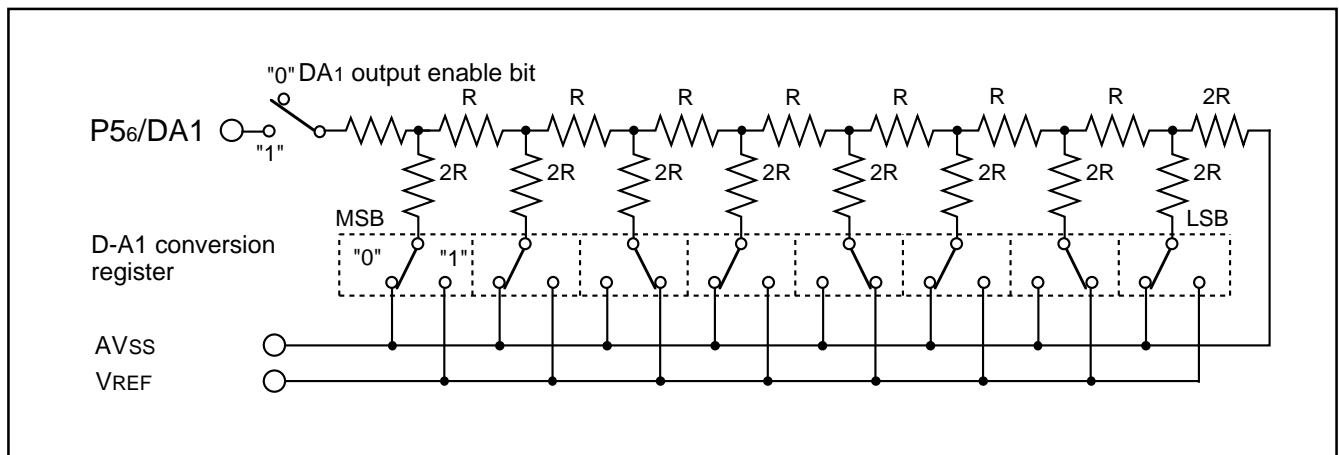


Fig. 21 Equivalent connection circuit of D-A converter

**Reset Circuit**

To reset the microcomputer, the RESET pin should be held at an "L" level for 2 μs or more. Then the RESET pin is returned to an "H" level (Note 1), reset is released. Internal operation does not begin until after 8 to 13 XIN clock cycles are completed. After the reset is completed, the program starts from the address contained in address FFFD<sub>16</sub> (high-order byte) and address FFFC<sub>16</sub> (low-order byte).

Make sure that the reset input voltage is less than 0.8 V for VCC of 4.0 V (Note 2).

**Note 1.** The power source voltage should be between the following voltage.

- Between 3.0 V and 5.5 V for standard version
- Between 4.0 V and 5.5 V for extended operating temperature version
- Between 2.7 V and 5.5 V for high-speed version

**Note 2.** Reset input voltage is less than the following voltage.

- 0.6 V for VCC = 3.0 V
- 0.8 V for VCC = 4.0 V
- 0.54 V for VCC = 2.7 V

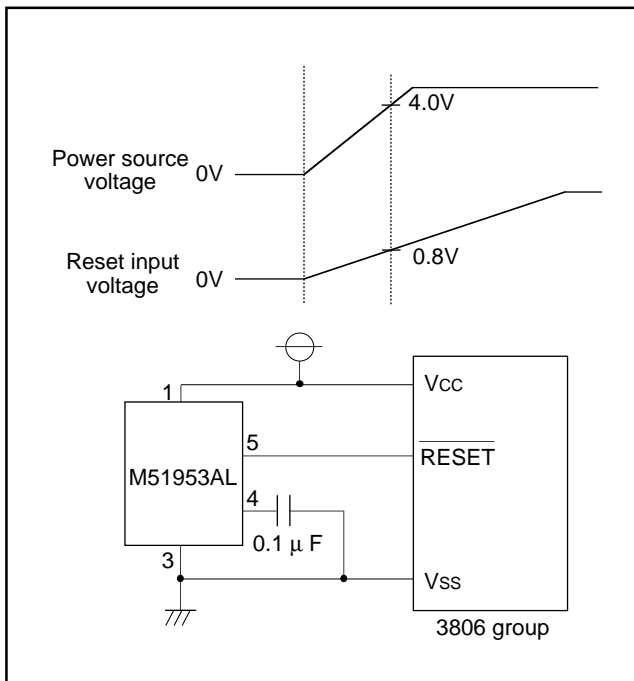


Fig. 22 Example of reset circuit

	Address	Register contents
(1) Port P0 direction register	(0001 <sub>16</sub> ) •••	00 <sub>16</sub>
(2) Port P1 direction register	(0003 <sub>16</sub> ) •••	00 <sub>16</sub>
(3) Port P2 direction register	(0005 <sub>16</sub> ) •••	00 <sub>16</sub>
(4) Port P3 direction register	(0007 <sub>16</sub> ) •••	00 <sub>16</sub>
(5) Port P4 direction register	(0009 <sub>16</sub> ) •••	00 <sub>16</sub>
(6) Port P5 direction register	(000B <sub>16</sub> ) •••	00 <sub>16</sub>
(7) Port P6 direction register	(000D <sub>16</sub> ) •••	00 <sub>16</sub>
(8) Port P7 direction register	(000F <sub>16</sub> ) •••	00 <sub>16</sub>
(9) Port P8 direction register	(0011 <sub>16</sub> ) •••	00 <sub>16</sub>
(10) Serial I/O1 status register	(0019 <sub>16</sub> ) •••	1 0 0 0 0 0 0 0
(11) Serial I/O1 control register	(001A <sub>16</sub> ) •••	00 <sub>16</sub>
(12) UART control register	(001B <sub>16</sub> ) •••	1 1 1 0 0 0 0 0
(13) Serial I/O2 control register	(001D <sub>16</sub> ) •••	00 <sub>16</sub>
(14) Prescaler 12	(0020 <sub>16</sub> ) •••	FF <sub>16</sub>
(15) Timer 1	(0021 <sub>16</sub> ) •••	01 <sub>16</sub>
(16) Timer 2	(0022 <sub>16</sub> ) •••	FF <sub>16</sub>
(17) Timer XY mode register	(0023 <sub>16</sub> ) •••	00 <sub>16</sub>
(18) Prescaler X	(0024 <sub>16</sub> ) •••	FF <sub>16</sub>
(19) Timer X	(0025 <sub>16</sub> ) •••	FF <sub>16</sub>
(20) Prescaler Y	(0026 <sub>16</sub> ) •••	FF <sub>16</sub>
(21) Timer Y	(0027 <sub>16</sub> ) •••	FF <sub>16</sub>
(22) AD/DA control register	(0034 <sub>16</sub> ) •••	0 0 0 0 0 1 0 0
(23) D-A1 conversion register	(0036 <sub>16</sub> ) •••	00 <sub>16</sub>
(24) D-A2 conversion register	(0037 <sub>16</sub> ) •••	00 <sub>16</sub>
(25) Interrupt edge selection register	(003A <sub>16</sub> ) •••	00 <sub>16</sub>
(26) CPU mode register	(003B <sub>16</sub> ) •••	0 0 0 0 0 0 0 *
(27) Interrupt request register 1	(003C <sub>16</sub> ) •••	00 <sub>16</sub>
(28) Interrupt request register 2	(003D <sub>16</sub> ) •••	00 <sub>16</sub>
(29) Interrupt control register 1	(003E <sub>16</sub> ) •••	00 <sub>16</sub>
(30) Interrupt control register 2	(003F <sub>16</sub> ) •••	00 <sub>16</sub>
(31) Processor status register	(PS)	x x x x x 1 x x
(32) Program counter	(PC <sub>H</sub> )	Contents of address FFFD <sub>16</sub>
	(PC <sub>L</sub> )	Contents of address FFFC <sub>16</sub>

Note. x : Undefined  
 \* : The initial values of CM<sub>1</sub> are determined by the level at the CNV<sub>SS</sub> pin.  
 The contents of all other registers and RAM are undefined after a reset, so they must be initialized by software.

Fig. 23 Internal status of microcomputer after reset

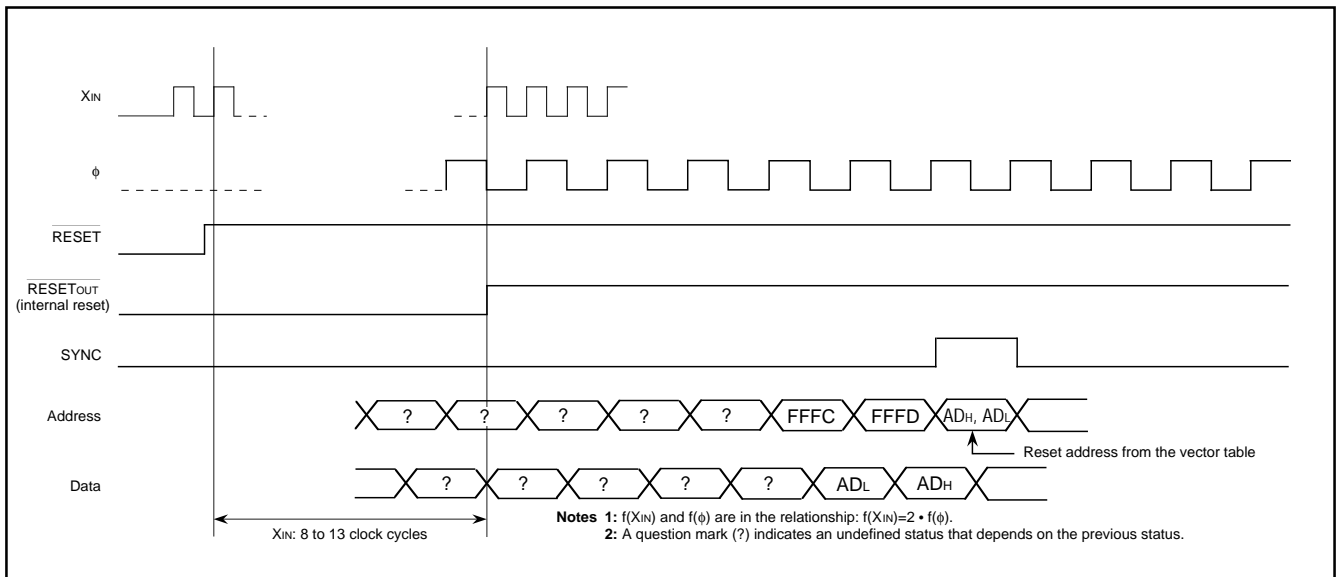


Fig. 24 Timing of reset

**Clock Generating Circuit**

An oscillation circuit can be formed by connecting a resonator between XIN and XOUT. To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open.

**Oscillation control**

**Stop Mode**

If the STP instruction is executed, the internal clock  $\phi$  stops at an "H". Timer 1 is set to "0116" and prescaler 12 is set to "FF16". Oscillator restarts when an external interrupt is received, but the internal clock  $\phi$  remains at an "H" until timer 1 underflow. This allows time for the clock circuit oscillation to stabilize. If oscillator is restarted by a reset, no wait time is generated, so keep the RESET pin at an "L" level until oscillation has stabilized.

**Wait Mode**

If the WIT instruction is executed, the internal clock  $\phi$  stops at an "H" level, but the oscillator itself does not stop. The internal clock restarts if a reset occurs or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted. To ensure that interrupts will be received to release the STP or WIT state, interrupt enable bits must be set to "1" before the STP or WIT instruction is executed.

When the STP status is released, prescaler 12 and timer 1 will start counting and reset will not be released until timer 1 underflows, so set the timer 1 interrupt enable bit to "0" before the STP instruction is executed.

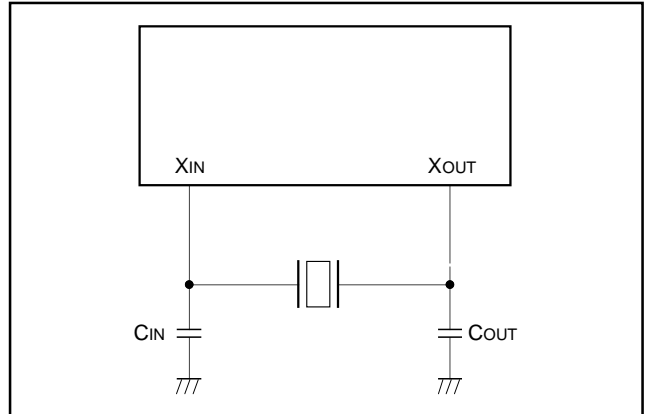


Fig. 25 Ceramic resonator circuit

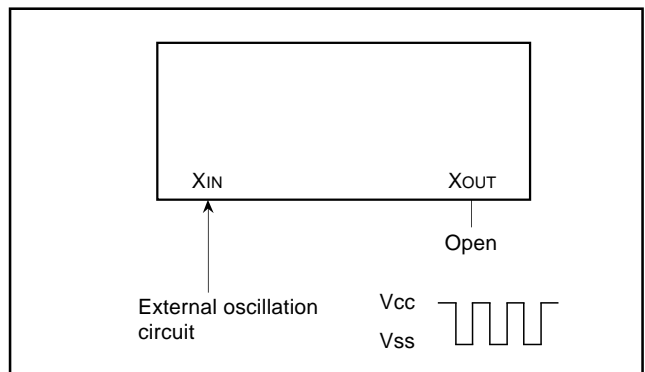


Fig. 26 External clock input circuit

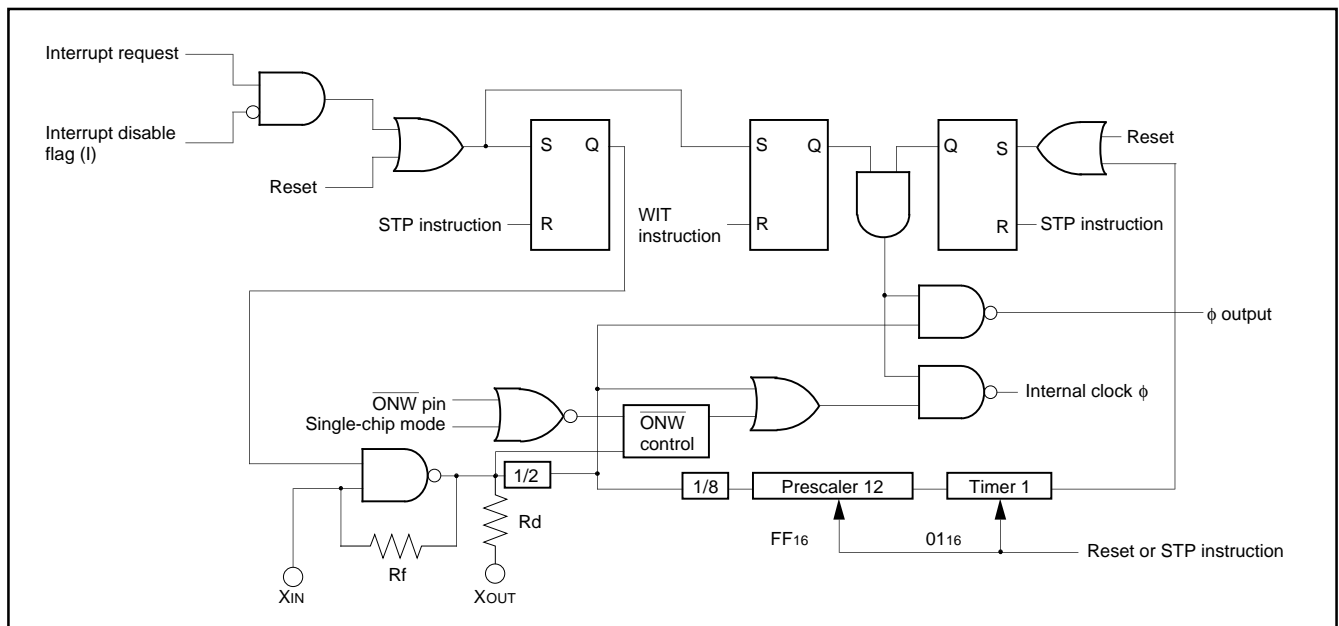


Fig. 27 Block diagram of clock generating circuit

**Processor Modes**

Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits CM0 and CM1 (bits 0 and 1 of address 003B<sub>16</sub>). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

**Table 2. Functions of ports in memory expansion mode and microprocessor mode**

Port Name	Function
Port P0	Outputs low-order byte of address.
Port P1	Outputs high-order byte of address.
Port P2	Operates as I/O pins for data D7 to D0 (including instruction codes).
Port P3	P30 and P31 function only as output pins (except that the port latch cannot be read). P32 is the ONW input pin. P33 is the RESET <sub>OUT</sub> output pin. (Note) P34 is the φ output pin. P35 is the SYNC output pin. P36 is the WR output pin, and P37 is the RD output pin.

**Note:** If CNV<sub>SS</sub> is connected to V<sub>SS</sub>, the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the RESET<sub>OUT</sub> output pin.

**Single-Chip Mode**

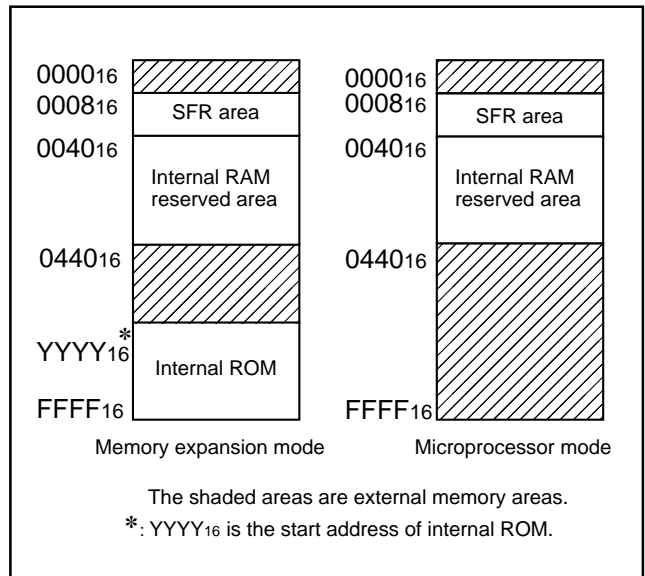
Select this mode by resetting the microcomputer with CNV<sub>SS</sub> connected to V<sub>SS</sub>.

**Memory Expansion Mode**

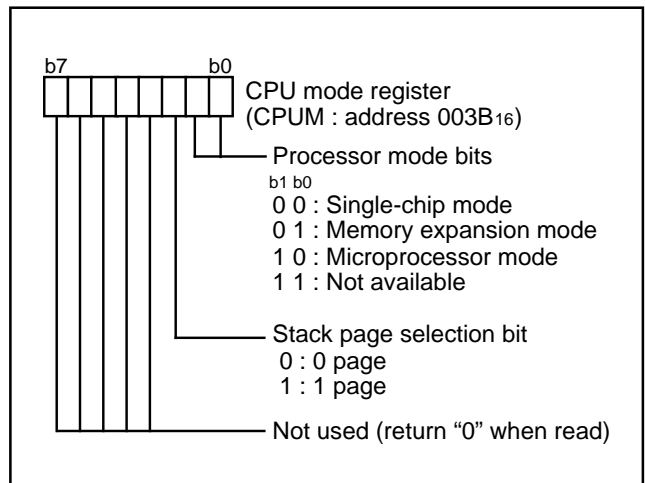
Select this mode by setting the processor mode bits to "01" in software with CNV<sub>SS</sub> connected to V<sub>SS</sub>. This mode enables external memory expansion while maintaining the validity of the internal ROM. Internal ROM will take precedence over external memory if addresses conflict.

**Microprocessor Mode**

Select this mode by resetting the microcomputer with CNV<sub>SS</sub> connected to V<sub>CC</sub>, or by setting the processor mode bits to "10" in software with CNV<sub>SS</sub> connected to V<sub>SS</sub>. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.



**Fig. 28 Memory maps in various processor modes**



**Fig. 29 Structure of CPU mode register**

**Bus control with memory expansion**

The 3806 group has a built-in ONW function to facilitate access to external memory and I/O devices in memory expansion mode or microprocessor mode.

If an "L" level signal is input to the  $\overline{\text{ONW}}$  pin when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of  $\phi$ . During this extended period, the  $\overline{\text{RD}}$  or  $\overline{\text{WR}}$  signal remains at "L". This extension period is valid only for writing to and reading from addresses  $0000_{16}$  to  $0007_{16}$  and  $0440_{16}$  to  $FFFF_{16}$  in microprocessor mode,  $0440_{16}$  to  $YYYY_{16}$  in memory expansion mode, and only read and write cycles are extended.

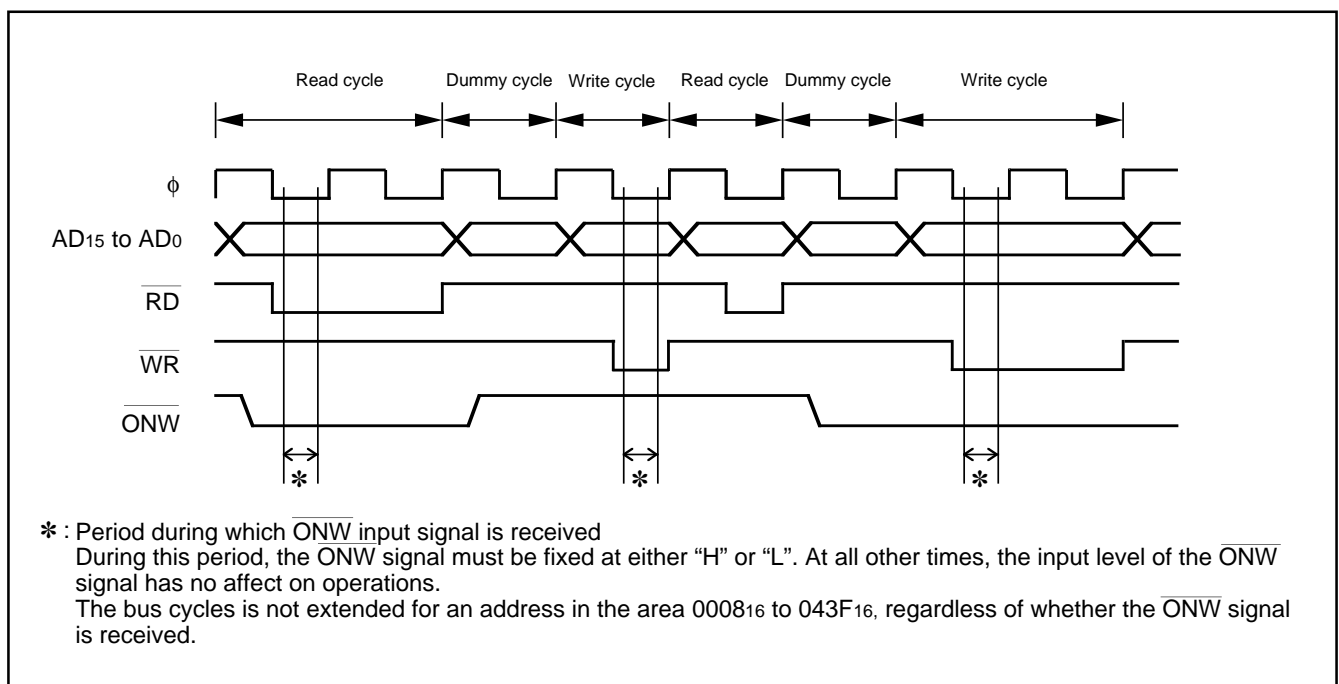


Fig. 30  $\overline{\text{ONW}}$  function timing

## NOTES ON PROGRAMMING

### Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

### Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before executing a BBC or BBS instruction.

### Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

The carry flag can be used to indicate whether a carry or borrow has occurred. Initialize the carry flag before each calculation. Clear the carry flag before an ADC and set the flag before an SBC.

### Timers

If a value  $n$  (between 0 and 255) is written to a timer latch, the frequency division ratio is  $1/(n + 1)$ .

### Multiplication and Division Instructions

The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.

The execution of these instructions does not change the contents of the processor status register.

### Ports

The contents of the port direction registers cannot be read.

The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instruction (ROR, CLB, or SEB, etc.) to a direction register

Use instructions such as LDM and STA, etc., to set the port direction registers.

### Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the  $\overline{\text{SRDY}}_1$  signal, set the transmit enable bit, the receive enable bit, and the  $\overline{\text{SRDY}}_1$  output enable bit to "1".

Serial I/O1 continues to output the final bit from the TXD pin after transmission is completed. The SOUT2 pin from serial I/O2 goes to high impedance after transmission is completed.

### A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Make sure that  $f(\text{XIN})$  is at least 500 kHz during an A-D conversion. (If the  $\overline{\text{ONW}}$  pin has been set to "L", the A-D conversion will take twice as long to match the longer bus cycle, and so  $f(\text{XIN})$  must be at least 1 MHz.)

Do not execute the STP or WIT instruction during an A-D conversion.

### D-A Converter

The accuracy of the D-A converter becomes poor rapidly under the  $V_{CC} = 4.0 \text{ V}$  or less condition.

### Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock  $\phi$  by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock  $\phi$  is half of the  $\text{XIN}$  frequency. When the  $\overline{\text{ONW}}$  function is used in modes other than single-chip mode, the frequency of the internal clock  $\phi$  may be one fourth the  $\text{XIN}$  frequency.

### Memory Expansion Mode and Microprocessor Mode

Execute the LDM or STA instruction for writing to port P3 (address 000616) in memory expansion mode and microprocessor mode.

Set areas which can be read out and write to port P3 (address 000616) in a memory, using the read-modify-write instruction (SEB, CLB).



**DATA REQUIRED FOR MASK ORDERS**

The following are necessary when ordering a mask ROM production:

1. Mask ROM Order Confirmation Form
2. Mark Specification Form
3. Data to be written to ROM, in EPROM form (three identical copies)

**ROM PROGRAMMING METHOD**

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80P6S-A	PCA4738G-80A
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 40 is recommended to verify programming.

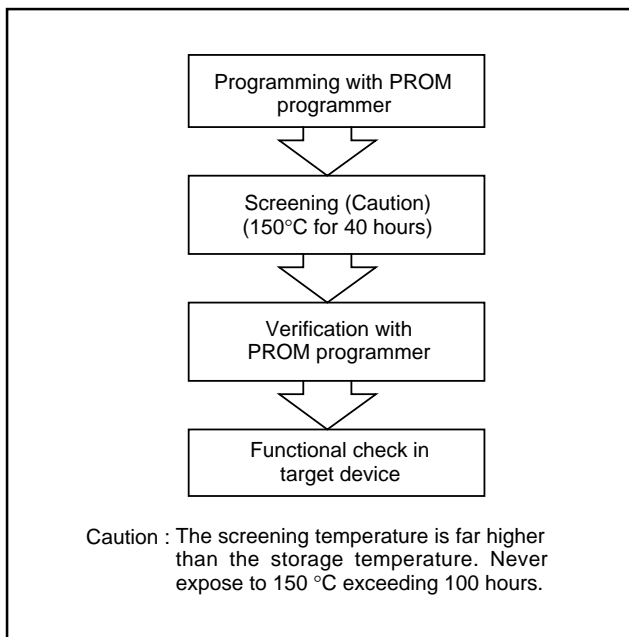


Fig. 31 Programming and testing of One Time PROM version

**ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Power source voltage		-0.3 to 7.0	V
V <sub>I</sub>	Input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, VREF	All voltages are based on V <sub>SS</sub> . Output transistors are cut off.	-0.3 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage RESET, X <sub>IN</sub>		-0.3 to V <sub>CC</sub> +0.3	V
V <sub>I</sub>	Input voltage CNV <sub>SS</sub>		-0.3 to 13	V
V <sub>O</sub>	Output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, X <sub>OUT</sub>		-0.3 to V <sub>CC</sub> +0.3	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25 °C	500	mW
T <sub>opr</sub>	Operating temperature		-20 to 85	°C
T <sub>stg</sub>	Storage temperature		-40 to 125	°C

**RECOMMENDED OPERATING CONDITIONS (V<sub>CC</sub>=3.0 to 5.5v, T<sub>a</sub>=-20 to 85°C, unless otherwise noted)**

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>CC</sub>	Power source voltage (f(X <sub>IN</sub> ) < 2 MHz) (Note 1)	3.0	5.0	5.5	V
	Power source voltage (f(X <sub>IN</sub> ) = 8 MHz) (Note 1)	4.0	5.0	5.5	
V <sub>SS</sub>	Power source voltage		0		V
V <sub>REF</sub>	Analog reference voltage (when A-D converter is used)	2.0		V <sub>CC</sub>	V
	Analog reference voltage (when D-A converter is used)	3.0		V <sub>CC</sub>	
AV <sub>SS</sub>	Analog power source voltage		0		V
V <sub>IA</sub>	Analog input voltage AN <sub>0</sub> -AN <sub>7</sub>		AV <sub>SS</sub>		V <sub>CC</sub>
V <sub>IH</sub>	"H" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	0.8 V <sub>CC</sub>			V <sub>CC</sub>
V <sub>IH</sub>	"H" input voltage RESET, X <sub>IN</sub> , CNV <sub>SS</sub>	0.8 V <sub>CC</sub>			V <sub>CC</sub>
V <sub>IL</sub>	"L" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	0		0.2 V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage RESET	0		0.2 V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage X <sub>IN</sub>	0		0.16 V <sub>CC</sub>	V
V <sub>IL</sub>	"L" input voltage CNV <sub>SS</sub>	0		0.2 V <sub>CC</sub>	V
ΣIOH(peak)	"H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 2)			-80	mA
ΣIOH(peak)	"H" total peak output current P40-P47, P50-P57, P60-P67 (Note 2)			-80	mA
ΣIOL(peak)	"L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 2)			80	mA
ΣIOL(peak)	"L" total peak output current P40-P47, P50-P57, P60-P67, P70-P77 (Note 2)			80	mA
ΣIOH(avg)	"H" total average output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 2)			-40	mA
ΣIOH(avg)	"H" total average output current P40-P47, P50-P57, P60-P67 (Note 2)			-40	mA
ΣIOL(avg)	"L" total average output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 2)			40	mA
ΣIOL(avg)	"L" total average output current P40-P47, P50-P57, P60-P67, P70-P77 (Note 2)			40	mA
IOH(peak)	"H" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 3)			-10	mA
IOL(peak)	"L" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 (Note 3)			10	mA
IOH(avg)	"H" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 4)			-5	mA
IOL(avg)	"L" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 (Note 4)			5	mA
f(X <sub>IN</sub> )	Internal clock oscillation frequency (V <sub>CC</sub> = 4.0 to 5.5 V)			8	MHz
	Internal clock oscillation frequency (V <sub>CC</sub> = 3.0 to 4.0 V)			6 V <sub>CC</sub> -16	

**Note 1:** The minimum power source voltage is  $\frac{X+16}{6}$  [V] (f(X<sub>IN</sub>) = XMHz) on the condition of 2 MHz < f(X<sub>IN</sub>) < 8 MHz.

**2:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

**3:** The peak output current is the peak current flowing in each port.

**4:** The average output current IOL(avg), IOH(avg) in an average value measured over 100 ms.

**ELECTRICAL CHARACTERISTICS** (VCC = 3.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 1)	IOH = -10 mA VCC = 4.0 to 5.5 V	VCC-2.0			V
		IOH = -1.0 mA VCC = 3.0 to 5.5 V	VCC-1.0			
VOL	"L" output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	IOI = 10 mA VCC = 4.0 to 5.5 V			2.0	V
		IOI = 1.0 mA VCC = 3.0 to 5.5 V			1.0	
VT+ - VT-	Hysteresis CNTR0, CNTR1, INT0-INT4			0.4		V
VT+ - VT-	Hysteresis RXD, SCLK1, SIN2, SCLK2			0.5		V
VT+ - VT-	Hysteresis RESET			0.5		V
IiH	"H" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	Vi = VCC			5.0	μA
IiH	"H" input current RESET, CNVSS	Vi = VCC			5.0	μA
IiH	"H" input current XIN	Vi = VCC		4		μA
IiL	"L" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	Vi = VSS			-5.0	μA
IiL	"L" input current RESET, CNVSS	Vi = VSS			-5.0	μA
IiL	"L" input current XIN	Vi = VSS		-4		μA
V <sub>RAM</sub>	RAM hold voltage	When clock stopped	2.0		5.5	V
ICC	Power source current	f(XIN) = 8 MHz, VCC = 5 V		6.4	13	mA
		f(XIN) = 5 MHz, VCC = 5 V		4	8	
		f(XIN) = 2 MHz, VCC = 3 V		0.8	2.0	
		When WIT instruction is executed with f(XIN) = 8MHz, VCC=5V		1.5		
		When WIT instruction is executed with f(XIN) = 5MHz, VCC=5V		1		
		When WIT instruction is executed with f(XIN) = 2MHz, VCC=3V		0.2		
		When STP instruction is executed with clock stopped, output transistors isolated.	Ta = 25 °C (Note 2) Ta = 85 °C (Note 2)		0.1	1
					10	μA

**Note 1:** P45 is measured when the P45/TXD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".  
**Note 2:** With output transistors isolated and A-D converter having completed conversion, and not including current flowing through VREF pin.

**A-D CONVERTER CHARACTERISTICS**

(VCC = 3.0 to 5.5 V, VSS = AVSS = 0 V, VREF = 2.0 V to VCC, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			±1	±2.5	LSB
tCONV	Conversion time				50	tc(φ)
RLADDER	Ladder resistor			35		kΩ
I <sub>VREF</sub>	Reference power source input current (Note)	VREF = 5.0 V	50	150	200	μA
I <sub>I(AD)</sub>	A-D port input current			0.5	5.0	μA

**Note:** When D-A conversion registers (addresses 003616 and 003716) contain "0016".

**D-A CONVERTER CHARACTERISTICS**

(VCC = 3.0 to 5.5 V, VSS = AVSS = 0 V, VREF = 3.0 V to VCC, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy	VCC = 4.0 to 5.5 V				1.0	%
		VCC = 3.0 to 4.0 V				2.5	
tsu	Setting time					3	μs
RO	Output resistor			1	2.5	4	kΩ
IVREF	Reference power source input current (Note)					3.2	mA

**Note:** Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

**TIMING REQUIREMENTS 1** ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			$\mu\text{s}$
$t_c(X_{IN})$	External clock input cycle time	125			ns
$t_wH(X_{IN})$	External clock input "H" pulse width	50			ns
$t_wL(X_{IN})$	External clock input "L" pulse width	50			ns
$t_c(\text{CNTR})$	CNTR0, CNTR1 input cycle time	200			ns
$t_wH(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	80			ns
$t_wH(\text{INT})$	INT0 to INT4 input "H" pulse width	80			ns
$t_wL(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	80			ns
$t_wL(\text{INT})$	INT0 to INT4 input "L" pulse width	80			ns
$t_c(\text{SCLK1})$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_c(\text{SCLK2})$	Serial I/O2 clock input cycle time	1000			ns
$t_wH(\text{SCLK1})$	Serial I/O1 clock input "H" pulse width (Note)	370			ns
$t_wH(\text{SCLK2})$	Serial I/O2 clock input "H" pulse width	400			ns
$t_wL(\text{SCLK1})$	Serial I/O1 clock input "L" pulse width (Note)	370			ns
$t_wL(\text{SCLK2})$	Serial I/O2 clock input "L" pulse width	400			ns
$t_{su}(\text{RxD-SCLK1})$	Serial I/O1 input set up time	220			ns
$t_{su}(\text{SIN2-SCLK2})$	Serial I/O2 input set up time	200			ns
$t_h(\text{SCLK1-RxD})$	Serial I/O1 input hold time	100			ns
$t_h(\text{SCLK2-SIN2})$	Serial I/O2 input hold time	200			ns

**Note:** When bit 6 of address 001A16 is "1". Divide this value by four when bit 6 of address 001A16 is "0".

**TIMING REQUIREMENTS 2** ( $V_{CC} = 3.0$  to  $4.0$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\text{RESET})$	Reset input "L" pulse width	2			$\mu\text{s}$
$t_c(X_{IN})$	External clock input cycle time	500/ (3 $V_{CC}$ -8)			ns
$t_wH(X_{IN})$	External clock input "H" pulse width	200/ (3 $V_{CC}$ -8)			ns
$t_wL(X_{IN})$	External clock input "L" pulse width	200/ (3 $V_{CC}$ -8)			ns
$t_c(\text{CNTR})$	CNTR0, CNTR1 input cycle time	500			ns
$t_wH(\text{CNTR})$	CNTR0, CNTR1 input "H" pulse width	230			ns
$t_wH(\text{INT})$	INT0 to INT4 input "H" pulse width	230			ns
$t_wL(\text{CNTR})$	CNTR0, CNTR1 input "L" pulse width	230			ns
$t_wL(\text{INT})$	INT0 to INT4 input "L" pulse width	230			ns
$t_c(\text{SCLK1})$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_c(\text{SCLK2})$	Serial I/O2 clock input cycle time	2000			ns
$t_wH(\text{SCLK1})$	Serial I/O1 clock input "H" pulse width (Note)	950			ns
$t_wH(\text{SCLK2})$	Serial I/O2 clock input "H" pulse width	950			ns
$t_wL(\text{SCLK1})$	Serial I/O1 clock input "L" pulse width (Note)	950			ns
$t_wL(\text{SCLK2})$	Serial I/O2 clock input "L" pulse width	950			ns
$t_{su}(\text{RxD-SCLK1})$	Serial I/O1 input set up time	400			ns
$t_{su}(\text{SIN2-SCLK2})$	Serial I/O2 input set up time	400			ns
$t_h(\text{SCLK1-RxD})$	Serial I/O1 input hold time	200			ns
$t_h(\text{SCLK2-SIN2})$	Serial I/O2 input hold time	300			ns

**Note :** When bit 6 of address 001A16 is "1". Divide this value by four when bit 6 of address 001A16 is "0".

**SWITCHING CHARACTERISTICS 1** ( $V_{CC} = 4.0$  to  $5.5$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{wH}(S_{CLK1})$	Serial I/O1 clock output "H" pulse width	Fig. 32	$t_c(S_{CLK1})/2-30$			ns
$t_{wL}(S_{CLK1})$	Serial I/O1 clock output "L" pulse width		$t_c(S_{CLK1})/2-30$			ns
$t_d(S_{CLK1}-TxD)$	Serial I/O1 output delay time (Note 1)				140	ns
$t_v(S_{CLK1}-TxD)$	Serial I/O1 output valid time (Note 1)		-30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time				30	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time				30	ns
$t_{wH}(S_{CLK2})$	Serial I/O2 clock output "H" pulse width		Fig. 33	$t_c(S_{CLK2})/2-160$		
$t_{wL}(S_{CLK2})$	Serial I/O2 clock output "L" pulse width	$t_c(S_{CLK2})/2-160$				ns
$t_d(S_{CLK2}-S_{OUT2})$	Serial I/O2 output delay time				200	ns
$t_v(S_{CLK2}-S_{OUT2})$	Serial I/O2 output valid time	0				ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time				40	ns
$t_r(CMOS)$	CMOS output rising time (Note 2)	Fig. 32		10	30	ns
$t_f(CMOS)$	CMOS output falling time (Note 2)			10	30	ns

**Note1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** Pins XOUT and P70–P77 are excluded.

**SWITCHING CHARACTERISTICS 2** ( $V_{CC} = 3.0$  to  $4.0$  V,  $V_{SS} = 0$  V,  $T_a = -20$  to  $85$  °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{wH}(S_{CLK1})$	Serial I/O1 clock output "H" pulse width	Fig. 32	$t_c(S_{CLK1})/2-50$			ns
$t_{wL}(S_{CLK1})$	Serial I/O1 clock output "L" pulse width		$t_c(S_{CLK1})/2-50$			ns
$t_d(S_{CLK1}-TxD)$	Serial I/O1 output delay time (Note 1)				350	ns
$t_v(S_{CLK1}-TxD)$	Serial I/O1 output valid time (Note 1)		-30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time				50	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time				50	ns
$t_{wH}(S_{CLK2})$	Serial I/O2 clock output "H" pulse width		Fig. 33	$t_c(S_{CLK2})/2-240$		
$t_{wL}(S_{CLK2})$	Serial I/O2 clock output "L" pulse width	$t_c(S_{CLK2})/2-240$				ns
$t_d(S_{CLK2}-S_{OUT2})$	Serial I/O2 output delay time				400	ns
$t_v(S_{CLK2}-S_{OUT2})$	Serial I/O2 output valid time	0				ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time				50	ns
$t_r(CMOS)$	CMOS output rising time (Note 2)	Fig. 32		20	50	ns
$t_f(CMOS)$	CMOS output falling time (Note 2)			20	50	ns

**Note1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** Pins XOUT and P70–P77 are excluded.

**TIMING REQUIREMENTS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tsu(ONW-φ)	Before φ ONW input set up time	-20			ns
th(φ-ONW)	After φ ONW input hold time	-20			ns
tsu(DB-φ)	Before φ data bus set up time	60			ns
th(φ-DB)	After φ data bus hold time	0			ns
tsu(ONW-RD)	Before RD ONW input set up time	-20			ns
tsu(ONW-WR)	Before WR ONW input set up time	-20			ns
th(RD-ONW)	After RD ONW input hold time	-20			ns
th(WR-ONW)	After WR ONW input hold time	-20			ns
tsu(DB-RD)	Before RD data bus set up time	65			ns
th(RD-DB)	After RD data bus hold time	0			ns

**SWITCHING CHARACTERISTICS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
tc(φ)	φ clock cycle time	Fig. 32		2tc(XIN)		ns	
twH(φ)	φ clock "H" pulse width		tc(XIN)-10			ns	
twL(φ)	φ clock "L" pulse width		tc(XIN)-10			ns	
td(φ-AH)	After φ AD15-AD8 delay time			20	40	ns	
tv(φ-AH)	After φ AD15-AD8 valid time			6	10	ns	
td(φ-AL)	After φ AD7-AD0 delay time				25	45	ns
tv(φ-AL)	After φ AD7-AD0 valid time			6	10	ns	
td(φ-SYNC)	SYNC delay time				20	ns	
tv(φ-SYNC)	SYNC valid time				10	ns	
td(φ-WR)	RD and WR delay time				10	20	ns
tv(φ-WR)	RD and WR valid time			3	5	10	ns
td(φ-DB)	After φ data bus delay time				20	70	ns
tv(φ-DB)	After φ data bus valid time			15			ns
twL(RD)	RD pulse width, WR pulse width			tc(XIN)-10			ns
twL(WR)	RD pulse width, WR pulse width (When one-wait is valid)			3tc(XIN)-10			ns
td(AH-RD)	After AD15-AD8 RD delay time			tc(XIN)-35	tc(XIN)-15		ns
td(AH-WR)	After AD15-AD8 WR delay time						ns
td(AL-RD)	After AD7-AD0 RD delay time			tc(XIN)-40	tc(XIN)-20		ns
td(AL-WR)	After AD7-AD0 WR delay time						ns
tv(RD-AH)	After RD AD15-AD8 valid time			0	5		ns
tv(WR-AH)	After WR AD15-AD8 valid time						ns
tv(RD-AL)	After RD AD7-AD0 valid time			0	5		ns
tv(WR-AL)	After WR AD7-AD0 valid time						ns
td(WR-DB)	After WR data bus delay time				15	65	ns
tv(WR-DB)	After WR data bus valid time			10			ns
td(RESET-RESETOUT)	RESETOUT output delay time (Note 1)					200	ns
tv(φ-RESET)	RESETOUT output valid time (Note 1)		0		200	ns	

**Note 1:** The RESETOUT output goes "H" in sync with the fall of the φ clock that is anywhere between about 8 cycle and 13 cycles after the RESET input goes "H".

**TIMING REQUIREMENTS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(V<sub>CC</sub> = 3.0 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>su</sub> (ONW-φ)	Before φ ONW input set up time	-20			ns
t <sub>h</sub> (φ-ONW)	After φ ONW input hold time	-20			ns
t <sub>su</sub> (DB-φ)	Before φ data bus set up time	180			ns
t <sub>h</sub> (φ-DB)	After φ data bus hold time	0			ns
t <sub>su</sub> (ONW-RD) t <sub>su</sub> (ONW-WR)	Before RD ONW input set up time Before WR ONW input set up time	-20			ns
t <sub>h</sub> (RD-ONW) t <sub>h</sub> (WR-ONW)	After RD ONW input hold time After WR ONW input hold time	-20			ns
t <sub>su</sub> (DB-RD)	Before RD data bus set up time	185			ns
t <sub>h</sub> (RD-DB)	After RD data bus hold time	0			ns

**SWITCHING CHARACTERISTICS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

(V<sub>CC</sub> = 3.0 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t <sub>c</sub> (φ)	φ clock cycle time	Fig. 32		2t <sub>c</sub> (X <sub>IN</sub> )		ns
t <sub>w</sub> H(φ)	φ clock "H" pulse width		t <sub>c</sub> (X <sub>IN</sub> )-20			ns
t <sub>w</sub> L(φ)	φ clock "L" pulse width		t <sub>c</sub> (X <sub>IN</sub> )-20			ns
t <sub>d</sub> (φ-AH)	After φ AD <sub>15</sub> -AD <sub>8</sub> delay time				150	ns
t <sub>v</sub> (φ-AH)	After φ AD <sub>15</sub> -AD <sub>8</sub> valid time		10	15		ns
t <sub>d</sub> (φ-AL)	After φ AD <sub>7</sub> -AD <sub>0</sub> delay time				150	ns
t <sub>v</sub> (φ-AL)	After φ AD <sub>7</sub> -AD <sub>0</sub> valid time		10	15		ns
t <sub>d</sub> (φ-SYNC)	SYNC delay time			40		ns
t <sub>v</sub> (φ-SYNC)	SYNC valid time			20		ns
t <sub>d</sub> (φ-WR)	RD and WR delay time			15	25	ns
t <sub>v</sub> (φ-WR)	RD and WR valid time		3	7	15	ns
t <sub>d</sub> (φ-DB)	After φ data bus delay time				200	ns
t <sub>v</sub> (φ-DB)	After φ data bus valid time		15			ns
t <sub>w</sub> L(RD) t <sub>w</sub> L(WR)	RD pulse width, WR pulse width RD pulse width, WR pulse width (when one-wait is valid)		t <sub>c</sub> (X <sub>IN</sub> )-20			ns
t <sub>d</sub> (AH-RD) t <sub>d</sub> (AH-WR)	After AD <sub>15</sub> -AD <sub>8</sub> RD delay time After AD <sub>15</sub> -AD <sub>8</sub> WR delay time		t <sub>c</sub> (X <sub>IN</sub> )-145			ns
t <sub>d</sub> (AL-RD) t <sub>d</sub> (AL-WR)	After AD <sub>7</sub> -AD <sub>0</sub> RD delay time After AD <sub>7</sub> -AD <sub>0</sub> WR delay time		t <sub>c</sub> (X <sub>IN</sub> )-145			ns
t <sub>v</sub> (RD-AH) t <sub>v</sub> (WR-AH)	After RD AD <sub>15</sub> -AD <sub>8</sub> valid time After WR AD <sub>15</sub> -AD <sub>8</sub> valid time		5	10		ns
t <sub>v</sub> (RD-AL) t <sub>v</sub> (WR-AL)	After RD AD <sub>7</sub> -AD <sub>0</sub> valid time After WR AD <sub>7</sub> -AD <sub>0</sub> valid time		5	10		ns
t <sub>d</sub> (WR-DB)	After WR data bus delay time				195	ns
t <sub>v</sub> (WR-DB)	After WR data bus valid time		10			ns
t <sub>d</sub> (RESET-RESETO <sub>UT</sub> )	RESETO <sub>UT</sub> output delay time (Note 1)				300	ns
t <sub>v</sub> (φ-RESET)	RESETO <sub>UT</sub> output valid time (Note 1)		0		300	ns

**Note1:** The RESETO<sub>UT</sub> output goes "H" in sync with the fall of the φ clock that is anywhere between about 8 cycle and 13 cycles after the RESET input goes "H".



**ABSOLUTE MAXIMUM RATINGS (Extended operating temperature version)**

Symbol	Parameter	Conditions	Ratings	Unit
VCC	Power source voltage		-0.3 to 7.0	V
Vi	Input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, VREF	All voltage are based on VSS. Output transistors are cut off.	-0.3 to VCC +0.3	V
Vi	Input voltage RESET, XIN		-0.3 to VCC +0.3	V
Vi	Input voltage CNVSS		-0.3 to 13	V
VO	Output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, XOUT		-0.3 to VCC +0.3	V
Pd	Power dissipation	Ta = 25 °C	500	mW
Topr	Operating temperature		-40 to 85	°C
Tstg	Storage temperature		-65 to 150	°C

**RECOMMENDED OPERATING CONDITIONS (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, Ta = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VCC	Power source voltage	4.0	5.0	5.5	V
VSS	Power source voltage		0		V
VREF	Analog reference voltage (when A-D converter is used)	2.0		VCC	V
	Analog reference voltage (when D-A converter is used)	4.0		VCC	V
AVSS	Analog power source voltage		0		V
VIa	Analog input voltage AN0-AN7	AVSS		VCC	V
VIH	"H" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	0.8 VCC		VCC	V
VIH	"H" input voltage RESET, XIN, CNVSS	0.8 VCC		VCC	V
VIL	"L" input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	0		0.2 VCC	V
VIL	"L" input voltage RESET, CNVSS	0		0.2 VCC	V
VIL	"L" input voltage XIN	0		0.16 VCC	V
ΣIOH(peak)	"H" total peak output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			-80	mA
ΣIOH(peak)	"H" total peak output current P40-P47, P50-P57, P60-P67 (Note 1)			-80	mA
ΣIOL(peak)	"L" total peak output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			80	mA
ΣIOL(peak)	"L" total peak output current P40-P47, P50-P57, P60-P67, P70-P77 (Note 1)			80	mA
ΣIOH(avg)	"H" total average output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			-40	mA
ΣIOH(avg)	"H" total average output current P40-P47, P50-P57, P60-P67 (Note 1)			-40	mA
ΣIOL(avg)	"L" total average output current P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			40	mA
ΣIOL(avg)	"L" total average output current P40-P47, P50-P57, P60-P67, P70-P77 (Note 1)			40	mA
IOH(peak)	"H" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 2)			-10	mA
IOL(peak)	"L" peak output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 (Note 2)			10	mA
IOH(avg)	"H" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 3)			-5	mA
IOL(avg)	"L" average output current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 (Note 3)			5	mA
f(XIN)	Internal clock oscillation frequency			8	MHz

**Note 1:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

**2:** The peak output current is the peak current flowing in each port.

**3:** The average output current IOL(avg), IOH(avg) in an average value measured over 100 ms.

**ELECTRICAL CHARACTERISTICS (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 1)	IOH = -10 mA	VCC-2.0			V
VOL	"L" output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	IOL = 10 mA			2.0	V
VT+ - VT-	Hysteresis	CNTR0, CNTR1, INT0-INT4		0.4		V
VT+ - VT-	Hysteresis	RxD, SCLK1, SIN2, SCLK2		0.5		V
VT+ - VT-	Hysteresis	RESET		0.5		V
IiH	"H" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	Vi = VCC			5.0	μA
IiH	"H" input current	RESET, CNVSS			5.0	μA
IiH	"H" input current	XIN		4		μA
IiL	"L" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	Vi = VSS			-5.0	μA
IiL	"L" input current	RESET, CNVSS			-5.0	μA
IiL	"L" input current	XIN		-4		μA
V <sub>RAM</sub>	RAM hold voltage	When clock stopped	2.0		5.5	V
ICC	Power source current	f(XIN) = 8 MHz		6.4	13	mA
		f(XIN) = 5 MHz		4	8	
		When WIT instruction is executed with f(XIN) = 8 MHz		1.5		
		When WIT instruction is executed with f(XIN) = 5 MHz		1		
		When STP instruction is executed with clock stopped, output transistors isolated.	Ta = 25 °C (Note 2)		0.1	1
	Ta = 85 °C (Note 2)			10		

**Note 1:** P45 is measured when the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".  
**Note 2:** With output transistors isolated and A-D converter having completed conversion, and not including current flowing through VREF pin.

**A-D CONVERTER CHARACTERISTICS(Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = AVSS = 0 V, VREF = 2.0 V to VCC, Ta = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			±1	±2.5	LSB
tCONV	Conversion time				50	tc(φ)
RLADDER	Ladder resistor			35		kΩ
I <sub>VREF</sub>	Reference power source input current (Note)	VREF = 5.0 V	50	150	200	μA
I <sub>I(AD)</sub>	A-D port input current			0.5	5.0	μA

**Note:** When D-A conversion registers (addresses 003616 and 003716) contain "0016".

**D-A CONVERTER CHARACTERISTICS (Extended operating temperature version)**

(VCC = 4.0 to 5.5 V, VSS = AVSS = 0 V, VREF = 3.0 V to VCC, Ta = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				1.0	%
tsu	Setting time				3	μs
RO	Output resistor		1	2.5	4	kΩ
IVREF	Reference power source input current (Note)				3.2	mA

**Note:** Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.

**TIMING REQUIREMENTS (Extended operating temperature version)**

(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	External clock input cycle time	125			ns
twH(XIN)	External clock input "H" pulse width	50			ns
twL(XIN)	External clock input "L" pulse width	50			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	200			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	80			ns
twH(INT)	INT0 to INT4 input "H" pulse width	80			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	80			ns
twL(INT)	INT0 to INT4 input "L" pulse width	80			ns
tc(SCLK1)	Serial I/O1 clock input cycle time (Note)	800			ns
tc(SCLK2)	Serial I/O2 clock input cycle time	1000			ns
twH(SCLK1)	Serial I/O1 clock input "H" pulse width (Note)	370			ns
twH(SCLK2)	Serial I/O2 clock input "H" pulse width	400			ns
twL(SCLK1)	Serial I/O1 clock input "L" pulse width (Note)	370			ns
twL(SCLK2)	Serial I/O2 clock input "L" pulse width	400			ns
tsu(RxD-SCLK1)	Serial I/O1 input set up time	220			ns
tsu(SIN2-SCLK2)	Serial I/O2 input set up time	200			ns
th(SCLK1-RxD)	Serial I/O1 input hold time	100			ns
th(SCLK2-SIN2)	Serial I/O2 input hold time	200			ns

**Note:** When bit 6 of address 001A16 is "1". Divide this value by four when bit 6 of address 001A16 is "0".

**SWITCHING CHARACTERISTICS (Extended operating temperature version)**

(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
twH(SCLK1)	Serial I/O1 clock output "H" pulse width	Fig. 32	tc(SCLK1)/2-30			ns
twL(SCLK1)	Serial I/O1 clock output "L" pulse width		tc(SCLK1)/2-30			ns
td(SCLK1-TxD)	Serial I/O1 output delay time (Note 1)				140	ns
tv(SCLK1-TxD)	Serial I/O1 output valid time (Note 1)			-30		ns
tr(SCLK1)	Serial I/O1 clock output rise time				30	ns
tf(SCLK1)	Serial I/O1 clock output fall time				30	ns
twH(SCLK2)	Serial I/O2 clock output "H" pulse width	Fig. 33	tc(SCLK2)/2-160			ns
twL(SCLK2)	Serial I/O2 clock output "L" pulse width		tc(SCLK2)/2-160			ns
td(SCLK2-SOUT2)	Serial I/O2 output delay time				200	ns
tv(SCLK2-SOUT2)	Serial I/O2 output valid time			0		ns
tf(SCLK2)	Serial I/O2 clock output fall time				40	ns
tr(CMOS)	CMOS output rise time (Note 2)		Fig. 32		10	30
tf(CMOS)	CMOS output fall time (Note 2)			10	30	ns

**Note1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** Pins XOUT pin and P70-P77 are excluded.

**TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**  
**(Extended operating temperature version)** (V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tsu(ONW-φ)	Before φ ONW input set up time	-20			ns
th(φ-ONW)	After φ ONW input hold time	-20			ns
tsu(DB-φ)	Before φ data bus set up time	60			ns
th(φ-DB)	After φ data bus hold time	0			ns
tsu(ONW-RD) tsu(ONW-WR)	Before RD ONW input set up time Before WR ONW input set up time	-20			ns
th(RD-ONW) th(WR-ONW)	After RD ONW input hold time After WR ONW input hold time	-20			ns
tsu(DB-RD)	Before RD data bus set up time	65			ns
th(RD-DB)	After RD data bus hold time	0			ns

**SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**  
**(Extended operating temperature version)** (V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -40 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tc(φ)	φ clock cycle time	Fig. 32		2tc(XIN)		ns
twH(φ)	φ clock "H" pulse width		tc(XIN)-10			ns
twL(φ)	φ clock "L" pulse width		tc(XIN)-10			ns
td(φ-AH)	After φ AD15-AD8 delay time			20	40	ns
tv(φ-AH)	After φ AD15-AD8 valid time		6	10		ns
td(φ-AL)	After φ AD7-AD0 delay time			25	45	ns
tv(φ-AL)	After φ AD7-AD0 valid time		6	10		ns
td(φ-SYNC)	SYNC delay time			20		ns
tv(φ-SYNC)	SYNC valid time			10		ns
td(φ-WR)	RD and WR delay time			10	20	ns
tv(φ-WR)	RD and WR valid time		3	5	10	ns
td(φ-DB)	After φ data bus delay time			20	70	ns
tv(φ-DB)	After φ data bus valid time		15			ns
twL(RD) twL(WR)	RD pulse width, WR pulse width RD pulse width, WR pulse width (When one-wait is valid)		tc(XIN)-10			ns
td(AH-RD) td(AH-WR)	After AD15-AD8 RD delay time After AD15-AD8 WR delay time		tc(XIN)-35	tc(XIN)-15		ns
td(AL-RD) td(AL-WR)	After AD7-AD0 RD delay time After AD7-AD0 WR delay time		tc(XIN)-40	tc(XIN)-20		ns
tv(RD-AH) tv(WR-AH)	After RD AD15-AD8 valid time After WR AD15-AD8 valid time		0	5		ns
tv(RD-AL) tv(WR-AL)	After RD AD7-AD0 valid time After WR AD7-AD0 valid time		0	5		ns
td(WR-DB)	After WR data bus delay time			15	65	ns
tv(WR-DB)	After WR data bus valid time		10			ns
td(RESET-RESETOUT)	RESETOUT output delay time (Note 1)				200	ns
tv(φ-RESET)	RESETOUT output valid time (Note 1)		0		200	ns

**Note 1:** The RESETOUT output goes "H" in sync with the fall of the φ clock that is anywhere between about 8 cycle and 13 cycles after the RESET input goes "H".

**ABSOLUTE MAXIMUM RATINGS (High-speed version)**

Symbol	Parameter	Conditions	Ratings	Unit	
VCC	Power source voltage	All voltages are based on Vss. Output transistors are cut off.	-0.3 to 7.0	V	
Vi	Input voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, VREF, XIN		-0.3 to Vcc +0.3	V	
Vi	Input voltage RESET		-0.3 to 7.0	V	
Vi	Input voltage CNVss		Mask ROM version	-0.3 to 7.0	V
			PROM version	-0.3 to 13	
VO	Output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, XOUT		-0.3 to Vcc +0.3	V	
Pd	Power dissipation	Ta = 25 °C	500	mW	
Topr	Operating temperature		-20 to 85	°C	
Tstg	Storage temperature		-40 to 125	°C	

**RECOMMENDED OPERATING CONDITIONS (High-speed version)**

(VCC = 2.7 to 5.5 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
VCC	Power source voltage (f(XIN) < 4.15 MHz)		2.7	5.0	5.5	V
	Power source voltage (f(XIN) = 10 MHz)		4.0	5.0	5.5	
VSS	Power source voltage			0		V
VREF	Analog reference voltage (when A-D converter is used)		2.0		Vcc	V
	Analog reference voltage (when D-A converter is used)		2.7		Vcc	
AVSS	Analog power source voltage			0		V
VIA	Analog input voltage	AN0-AN7	AVss		Vcc	V
VIH	"H" input voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, RESET, XIN, CNVss	0.8 Vcc		Vcc	V
VIL	"L" input voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, RESET, CNVss	0		0.2 Vcc	V
VIL	"L" input voltage	XIN	0		0.16 Vcc	V
ΣIOH(peak)	"H" total peak output current	P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			-80	mA
ΣIOH(peak)	"H" total peak output current	P40-P47, P50-P57, P60-P67 (Note 1)			-80	
ΣIOL(peak)	"L" total peak output current	P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			80	mA
ΣIOL(peak)	"L" total peak output current	P40-P47, P50-P57, P60-P67, P70-P77 (Note 1)			80	
ΣIOH(avg)	"H" total average output current	P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			-40	mA
ΣIOH(avg)	"H" total average output current	P40-P47, P50-P57, P60-P67 (Note 1)			-40	
ΣIOL(avg)	"L" total average output current	P00-P07, P10-P17, P20-P27, P30-P37, P80-P87 (Note 1)			40	mA
ΣIOL(avg)	"L" total average output current	P40-P47, P50-P57, P60-P67, P70-P77 (Note 1)			40	
IOH(peak)	"H" peak output current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 2)			-10	mA
IOL(peak)	"L" peak output current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 (Note 2)			10	
IOH(avg)	"H" average output current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 3)			-5	mA
IOL(avg)	"L" average output current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87 (Note 3)			5	
f(XIN)	Internal clock oscillation frequency (4.0 V < VCC < 5.5 V)				10	MHz
	Internal clock oscillation frequency (2.7 V < VCC < 4.0 V)				4.5VCC-8	

**Note 1:** The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

**2:** The peak output current is the peak current flowing in each port.

**3:** The average output current IOL(avg), IOH(avg) in an average value measured over 100 ms.

**ELECTRICAL CHARACTERISTICS (High-speed version)**

(VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
VOH	"H" output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P80-P87 (Note 1)	IOH = -10 mA VCC = 4.0 to 5.5 V	VCC-2.0			V
		IOH = -1.0 mA VCC = 2.7 to 5.5 V	VCC-1.0			
VOL	"L" output voltage P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	IOL = 10 mA VCC = 4.0 to 5.5 V			2.0	V
		IOL = 1.0 mA VCC = 2.7 to 5.5 V			1.0	
VT+ - VT-	Hysteresis	CNTR0, CNTR1, INT0-INT4		0.4		V
VT+ - VT-	Hysteresis	RxD, SCLK1, SIN2, SCLK2		0.5		V
VT+ - VT-	Hysteresis	RESET		0.5		V
IiH	"H" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87	Vi = VCC			5.0	μA
IiH	"H" input current	RESET, CNVss	Vi = VCC		5.0	μA
IiH	"H" input current	XIN	Vi = VCC	4		μA
IiL	"L" input current P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, RESET, CNVss	Vi = VSS			-5.0	μA
IiL	"L" input current	XIN	Vi = VSS	-4		μA
VRAM	RAM hold voltage	With clock stopped	2.0		5.5	V
ICC	Power source current	f(XIN) = 10 MHz, VCC = 5 V		8	16	mA
		f(XIN) = 4 MHz, VCC = 2.7 V		1.3	2	
		When WIT instruction is executed with f(XIN) = 10 MHz, VCC = 5 V		2		
		When WIT instruction is executed with f(XIN) = 4 MHz, VCC = 2.7 V		0.3		
		When STP instruction is executed with clock stopped, output transistors isolated.	Ta = 25 °C (Note 2)		0.1	1
	Ta = 85 °C (Note 2)			10		

**Note 1:** P45 is measured when the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** With output transistors isolated and A-D converter having completed conversion, and not including current flowing through VREF pin.

**A-D CONVERTER CHARACTERISTICS (High-speed version)**

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, VREF = 2.0 V to VCC, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy (excluding quantization error)			±1	±2.5	LSB
tCONV	Conversion time				50	tc(φ)
RLADDER	Ladder resistor			35		kΩ
IvREF	Reference power source input current (Note)	VREF = 5.0 V	50	150	200	μA
Ii(AD)	A-D port input current			0.5	5.0	μA

**Note:** When D-A conversion registers (addresses 003616 and 003716) contain "0016".

**D-A CONVERTER CHARACTERISTICS (High-speed version)**

(VCC = 2.7 to 5.5 V, VSS = AVSS = 0 V, VREF = 2.7 V to VCC, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy	VCC = 4.0 to 5.5 V				1.0	%
		VCC = 2.7 to 5.5 V				2.5	
tsu	Setting time					3	μs
RO	Output resistor			1	2.5	4	kΩ
IVREF	Reference power source input current (Note)					3.2	mA

**Note:** Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "0016", and excluding currents flowing through the A-D resistance ladder.



**TIMING REQUIREMENTS 1 (High-speed version)**

(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	External clock input cycle time	100			ns
twH(XIN)	External clock input "H" pulse width	40			ns
twL(XIN)	External clock input "L" pulse width	40			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	200			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	80			ns
twH(INT)	INT0 to INT4 input "H" pulse width	80			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	80			ns
twL(INT)	INT0 to INT4 input "L" pulse width	80			ns
tc(SCLK1)	Serial I/O1 clock input cycle time (Note)	800			ns
tc(SCLK2)	Serial I/O2 clock input cycle time	1000			ns
twH(SCLK1)	Serial I/O1 clock input "H" pulse width (Note)	370			ns
twH(SCLK2)	Serial I/O2 clock input "H" pulse width	400			ns
twL(SCLK1)	Serial I/O1 clock input "L" pulse width (Note)	370			ns
twL(SCLK2)	Serial I/O2 clock input "L" pulse width	400			ns
tsu(RxD-SCLK1)	Serial I/O1 input set up time	220			ns
tsu(SIN2-SCLK2)	Serial I/O2 input set up time	200			ns
th(SCLK1-RxD)	Serial I/O1 input hold time	100			ns
th(SCLK2-SIN2)	Serial I/O2 input hold time	200			ns

**Note:** When f(XIN) = 8 MHz and bit 6 of address 001A16 is "1". Divide this value by four when f(XIN) = 8 MHz and bit 6 of address 001A16 is "0".

**TIMING REQUIREMENTS 2 (High-speed version)**

(V<sub>CC</sub> = 2.7 to 4.0 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw(RESET)	Reset input "L" pulse width	2			μs
tc(XIN)	External clock input cycle time	1000/ (4.5 V <sub>CC</sub> -8)			ns
twH(XIN)	External clock input "H" pulse width	400/ (4.5 V <sub>CC</sub> -8)			ns
twL(XIN)	External clock input "L" pulse width	400/ (4.5 V <sub>CC</sub> -8)			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	500			ns
twH(CNTR)	CNTR0, CNTR1 input "H" pulse width	230			ns
twH(INT)	INT0 to INT4 input "H" pulse width	230			ns
twL(CNTR)	CNTR0, CNTR1 input "L" pulse width	230			ns
twL(INT)	INT0 to INT4 input "L" pulse width	230			ns
tc(SCLK1)	Serial I/O1 clock input cycle time (Note)	2000			ns
tc(SCLK2)	Serial I/O2 clock input cycle time	2000			ns
twH(SCLK1)	Serial I/O1 clock input "H" pulse width (Note)	950			ns
twH(SCLK2)	Serial I/O2 clock input "H" pulse width	950			ns
twL(SCLK1)	Serial I/O1 clock input "L" pulse width (Note)	950			ns
twL(SCLK2)	Serial I/O2 clock input "L" pulse width	950			ns
tsu(RxD-SCLK1)	Serial I/O1 input set up time	400			ns
tsu(SIN2-SCLK2)	Serial I/O2 input set up time	400			ns
th(SCLK1-RxD)	Serial I/O1 input hold time	200			ns
th(SCLK2-SIN2)	Serial I/O2 input hold time	300			ns

**Note:** When f(XIN) = 2 MHz and bit 6 of address 001A16 is "1". Divide this value by four when f(XIN) = 2 MHz and bit 6 of address 001A16 is "0".

**SWITCHING CHARACTERISTICS 1 (High-speed version)**

(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
twH(SCLK1)	Serial I/O1 clock output "H" pulse width	Fig. 32	tc(SCLK1)/2-30			ns
twL(SCLK1)	Serial I/O1 clock output "L" pulse width		tc(SCLK1)/2-30			ns
td(SCLK1-TxD)	Serial I/O1 output delay time (Note 1)				140	ns
tv(SCLK1-TxD)	Serial I/O1 output valid time (Note 1)			-30		ns
tr(SCLK1)	Serial I/O1 clock output rising time				30	ns
tf(SCLK1)	Serial I/O1 clock output falling time				30	ns
twH(SCLK2)	Serial I/O2 clock output "H" pulse width	Fig. 33	tc(SCLK2)/2-160			ns
twL(SCLK2)	Serial I/O2 clock output "L" pulse width		tc(SCLK2)/2-160			ns
td(SCLK2-SOUT2)	Serial I/O2 output delay time				200	ns
tv(SCLK2-SOUT2)	Serial I/O2 output valid time			0		ns
tf(SCLK2)	Serial I/O2 clock output falling time				30	ns
tr(CMOS)	CMOS output rising time (Note 2)	Fig. 32		10	30	ns
tf(CMOS)	CMOS output falling time (Note 2)			10	30	ns

**Note1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** XOUT pin is excluded.

**SWITCHING CHARACTERISTICS 2 (High-speed version)**

(VCC = 2.7 to 4.0 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
twH(SCLK1)	Serial I/O1 clock output "H" pulse width	Fig. 32	tc(SCLK1)/2-50			ns
twL(SCLK1)	Serial I/O1 clock output "L" pulse width		tc(SCLK1)/2-50			ns
td(SCLK1-TxD)	Serial I/O1 output delay time (Note 1)				350	ns
tv(SCLK1-TxD)	Serial I/O1 output valid time (Note 1)			-30		ns
tr(SCLK1)	Serial I/O1 clock output rising time				50	ns
tf(SCLK1)	Serial I/O1 clock output falling time				50	ns
twH(SCLK2)	Serial I/O2 clock output "H" pulse width	Fig. 33	tc(SCLK2)/2-240			ns
twL(SCLK2)	Serial I/O2 clock output "L" pulse width		tc(SCLK2)/2-240			ns
td(SCLK2-SOUT2)	Serial I/O2 output delay time				400	ns
tv(SCLK2-SOUT2)	Serial I/O2 output valid time			0		ns
tf(SCLK2)	Serial I/O2 clock output falling time				50	ns
tr(CMOS)	CMOS output rising time (Note 2)	Fig. 32		20	50	ns
tf(CMOS)	CMOS output falling time (Note 2)			20	50	ns

**Note 1:** When the P45/TxD P-channel output disable bit of the UART control register (bit 4 of address 001B16) is "0".

**2:** XOUT pin is excluded.

**TIMING REQUIREMENTS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (High-speed version)**

(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t <sub>su</sub> (ONW-φ)	Before φ ONW input set up time	-20			ns
t <sub>h</sub> (φ-ONW)	After φ ONW input hold time	-20			ns
t <sub>su</sub> (DB-φ)	Before φ data bus set up time	50	25		ns
t <sub>h</sub> (φ-DB)	After φ data bus hold time	0			ns
t <sub>su</sub> (ONW-RD) t <sub>su</sub> (ONW-WR)	Before RD ONW input set up time Before WR ONW input set up time	-20			ns
t <sub>h</sub> (RD-ONW) t <sub>h</sub> (WR-ONW)	After RD ONW input hold time After WR ONW input hold time	-20			ns
t <sub>su</sub> (DB-RD)	Before RD data bus set up time	50	25		ns
t <sub>h</sub> (RD-DB)	After RD data bus hold time	0			ns

**SWITCHING CHARACTERISTICS 1 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE (High-speed version)**

(V<sub>CC</sub> = 4.0 to 5.5 V, V<sub>SS</sub> = 0 V, T<sub>a</sub> = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit	
			Min.	Typ.	Max.		
t <sub>c</sub> (φ)	φ clock cycle time	Fig. 32		2t <sub>c</sub> (X <sub>IN</sub> )		ns	
t <sub>wH</sub> (φ)	φ clock "H" pulse width		t <sub>c</sub> (X <sub>IN</sub> )-10			ns	
t <sub>wL</sub> (φ)	φ clock "L" pulse width		t <sub>c</sub> (X <sub>IN</sub> )-10			ns	
t <sub>d</sub> (φ-AH)	After φ AD <sub>15</sub> -AD <sub>8</sub> delay time			16	35	ns	
t <sub>v</sub> (φ-AH)	After φ AD <sub>15</sub> -AD <sub>8</sub> valid time			2	5	ns	
t <sub>d</sub> (φ-AL)	After φ AD <sub>7</sub> -AD <sub>0</sub> delay time			20	40	ns	
t <sub>v</sub> (φ-AL)	After φ AD <sub>7</sub> -AD <sub>0</sub> valid time			2	5	ns	
t <sub>d</sub> (φ-SYNC)	SYNC delay time			16		ns	
t <sub>v</sub> (φ-SYNC)	SYNC valid time			5		ns	
t <sub>d</sub> (φ-DB)	After φ data bus delay time			15	30	ns	
t <sub>v</sub> (φ-DB)	After φ data bus valid time			10		ns	
t <sub>wL</sub> (RD) t <sub>wL</sub> (WR)	RD pulse width, WR pulse width RD pulse width, WR pulse width (when one-wait is valid)			t <sub>c</sub> (X <sub>IN</sub> )-10 3t <sub>c</sub> (X <sub>IN</sub> )-10		ns	
t <sub>d</sub> (AH-RD) t <sub>d</sub> (AH-WR)	After AD <sub>15</sub> -AD <sub>8</sub> RD delay time After AD <sub>15</sub> -AD <sub>8</sub> WR delay time			t <sub>c</sub> (X <sub>IN</sub> )-35	t <sub>c</sub> (X <sub>IN</sub> )-16	ns	
t <sub>d</sub> (AL-RD) t <sub>d</sub> (AL-WR)	After AD <sub>7</sub> -AD <sub>0</sub> RD delay time After AD <sub>7</sub> -AD <sub>0</sub> WR delay time			t <sub>c</sub> (X <sub>IN</sub> )-40	t <sub>c</sub> (X <sub>IN</sub> )-20	ns	
t <sub>v</sub> (RD-AH) t <sub>v</sub> (WR-AH)	After RD AD <sub>15</sub> -AD <sub>8</sub> valid time After WR AD <sub>15</sub> -AD <sub>8</sub> valid time			2	5	ns	
t <sub>v</sub> (RD-AL) t <sub>v</sub> (WR-AL)	After RD AD <sub>7</sub> -AD <sub>0</sub> valid time After WR AD <sub>7</sub> -AD <sub>0</sub> valid time			2	5	ns	
t <sub>d</sub> (WR-DB)	After WR data bus delay time				15	30	ns
t <sub>v</sub> (WR-DB)	After WR data bus valid time			10		ns	
t <sub>d</sub> (RESET-RESETO <sub>UT</sub> )	RESETO <sub>UT</sub> output delay time (Note 1)					200	ns
t <sub>v</sub> (φ-RESET)	RESETO <sub>UT</sub> output valid time (Note 1)			0		100	ns

**Note 1:** The RESETO<sub>UT</sub> output goes "H" in sync with the fall of the φ clock that is anywhere between about 8 cycle and 13 cycles after the RESET input goes "H".

**TIMING REQUIREMENTS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

**(High-speed version)**

(VCC = 2.7 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tsu(ONW-φ)	Before φ ONW input set up time	-20			ns
th(φ-ONW)	After φ ONW input hold time	-20			ns
tsu(DB-φ)	Before φ data bus set up time	120	60		ns
th(φ-DB)	After φ data bus hold time	0			ns
tsu(ONW-RD)	Before RD ONW input set up time	-20			ns
tsu(ONW-WR)	Before WR ONW input set up time	-20			ns
th(RD-ONW)	After RD ONW input hold time	-20			ns
th(WR-ONW)	After WR ONW input hold time	-20			ns
tsu(DB-RD)	Before RD data bus set up time	120	60		ns
th(RD-DB)	After RD data bus hold time	0			ns

**SWITCHING CHARACTERISTICS 2 IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE**

**(High-Speed Version)**

(VCC = 2.7 V, VSS = 0 V, Ta = -20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tc(φ)	φ clock cycle time	Fig. 32		2tc(XIN)		ns
twH(φ)	φ clock "H" pulse width		tc(XIN)-20			ns
twL(φ)	φ clock "L" pulse width		tc(XIN)-20			ns
td(φ-AH)	AD15-AD8 delay time			40	100	ns
tv(φ-AH)	AD15-AD8 valid time		5	10		ns
td(φ-AL)	AD7-AD0 delay time			50	100	ns
tv(φ-AL)	AD7-AD0 valid time		5	10		ns
td(φ-SYNC)	SYNC delay time			40		ns
tv(φ-SYNC)	SYNC valid time			10		ns
td(φ-DB)	Data bus delay time			30	80	ns
tv(φ-DB)	Data bus valid time		10			ns
twL(RD)	RD pulse width, WR pulse width		tc(XIN)-20			ns
twL(WR)	RD pulse width, WR pulse width (when one-wait is valid)		3tc(XIN)-20			ns
td(AH-RD)	After AD15-AD8 RD delay time		tc(XIN)-100	tc(XIN)-40		ns
td(AL-RD)	After AD7-AD0 RD delay time		tc(XIN)-100	tc(XIN)-50		ns
td(AH-WR)	After AD15-AD8 WR delay time					ns
td(AL-WR)	After AD7-AD0 WR delay time					ns
tv(RD-AH)	After RD AD15-AD8 valid time		5	10		ns
tv(WR-AH)	After WR AD15-AD8 valid time					ns
tv(RD-AL)	After RD AD7-AD0 valid time		5	10		ns
tv(WR-AL)	After WR AD7-AD0 valid time				ns	
td(WR-DB)	After WR data bus delay time		30	80	ns	
tv(WR-DB)	After WR data bus valid time	10			ns	
td(RESET-RESETOUT)	RESETOUT output delay time (Note 1)			300	ns	
tv(φ-RESET)	RESETOUT output valid time (Note 1)	0		150	ns	

**Note 1:** The RESETOUT output goes "H" in sync with the rise of the φ clock that is anywhere between about 8 cycle and 13 cycles after the RESET input goes "H".

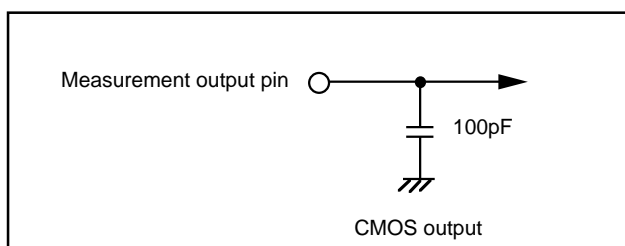


Fig. 32 Circuit for measuring output switching characteristics (1)

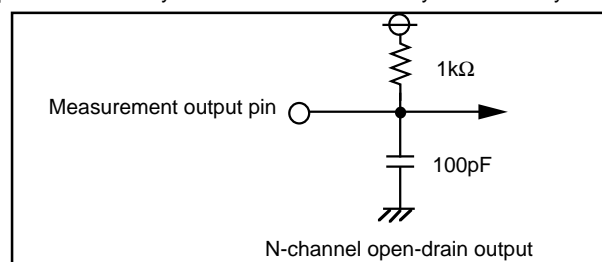
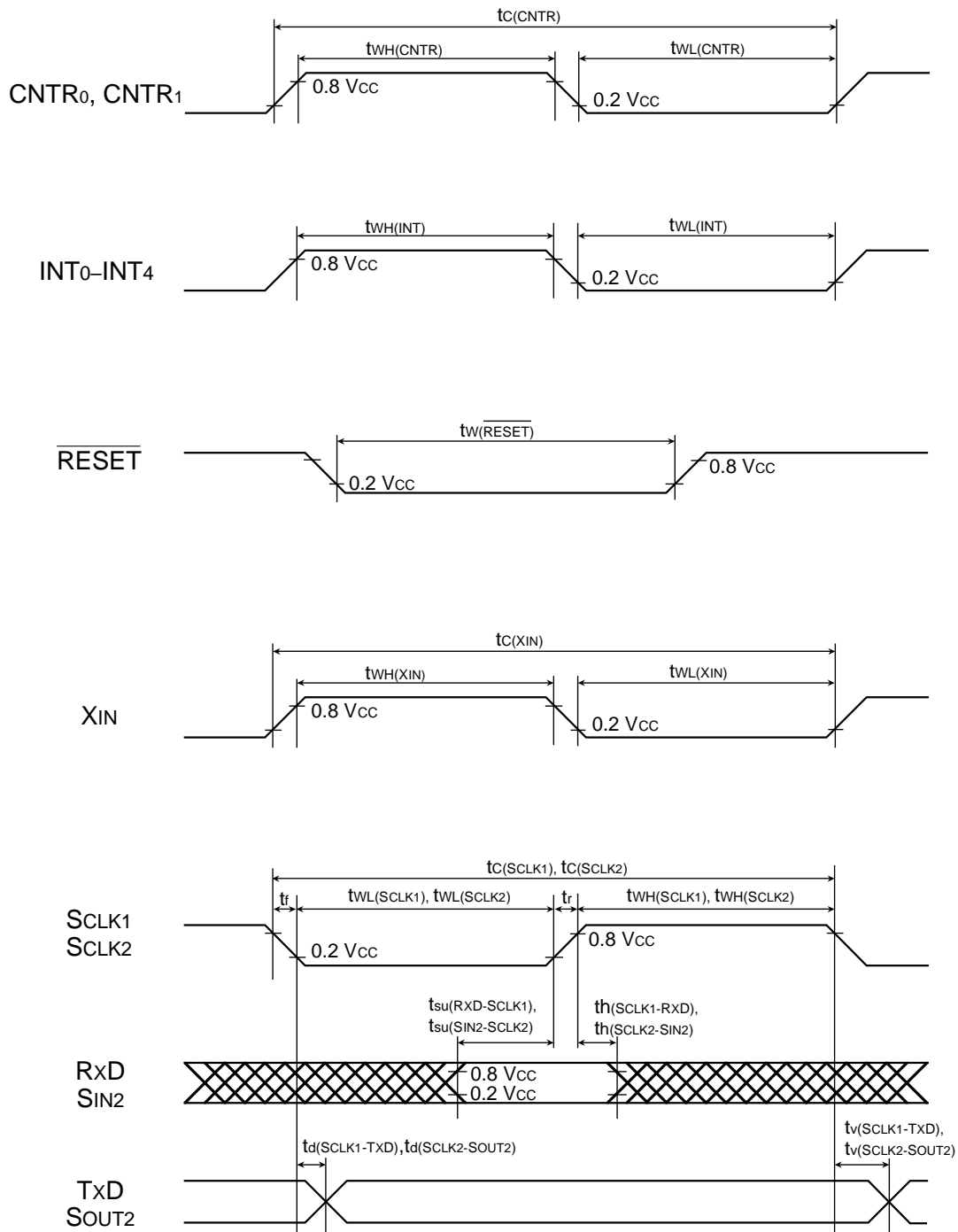


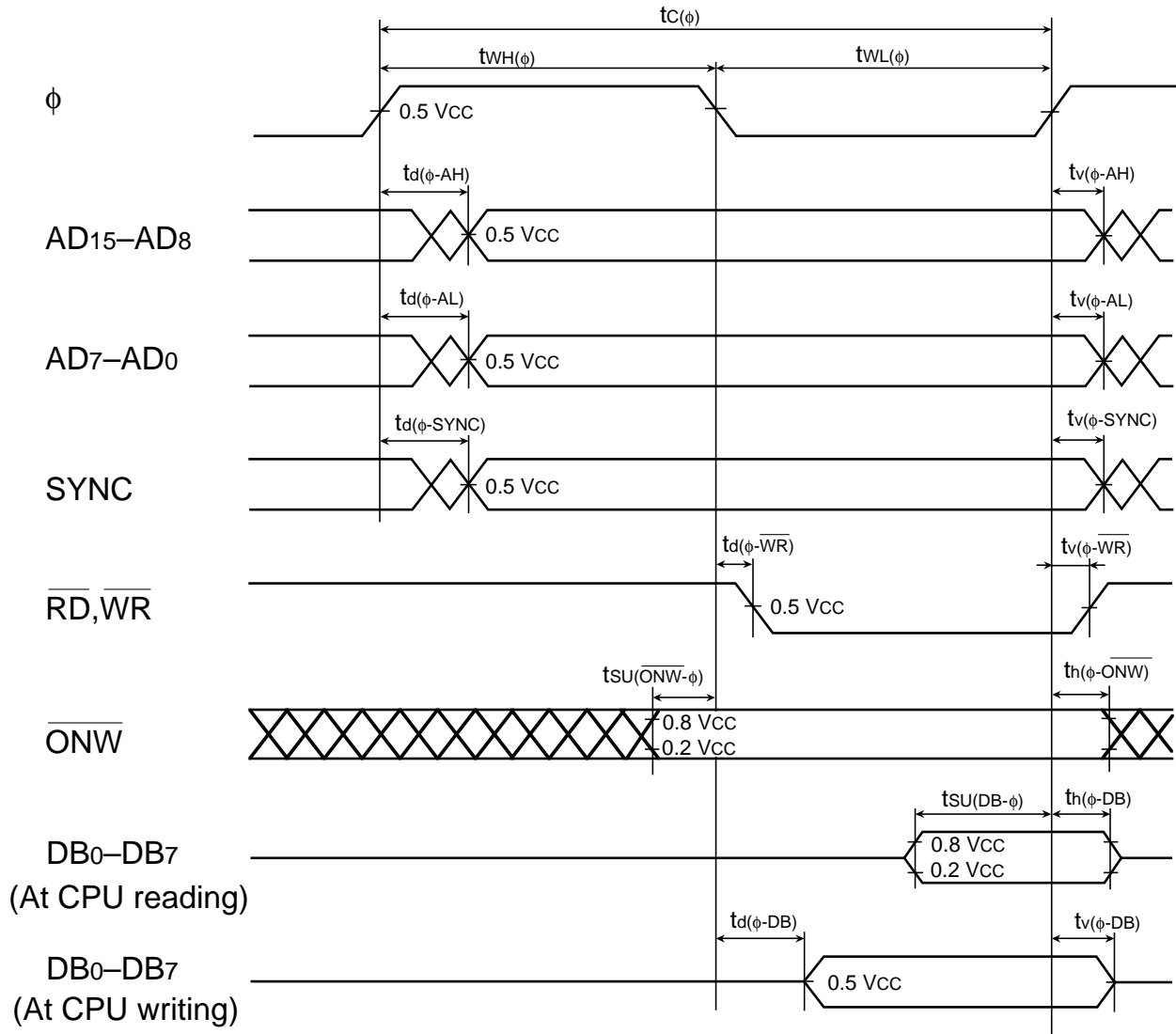
Fig. 33 Circuit for measuring output switching characteristics (2)

TIMING DIAGRAM

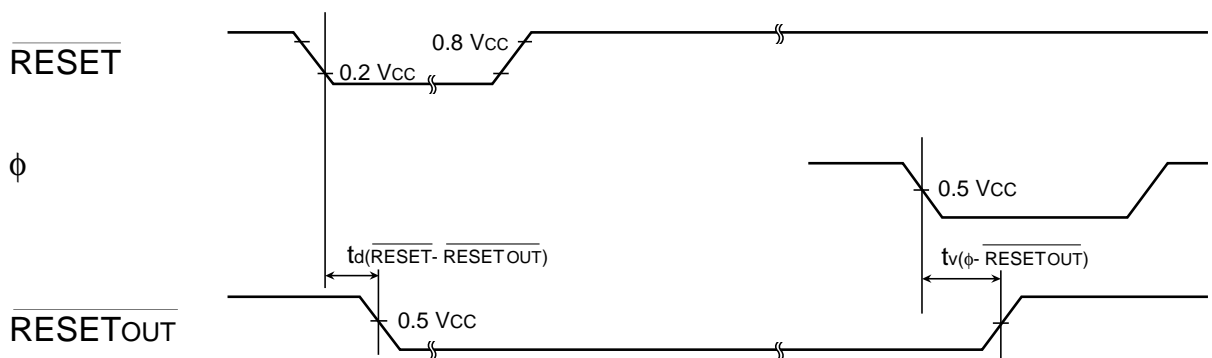
(1) Timing Diagram



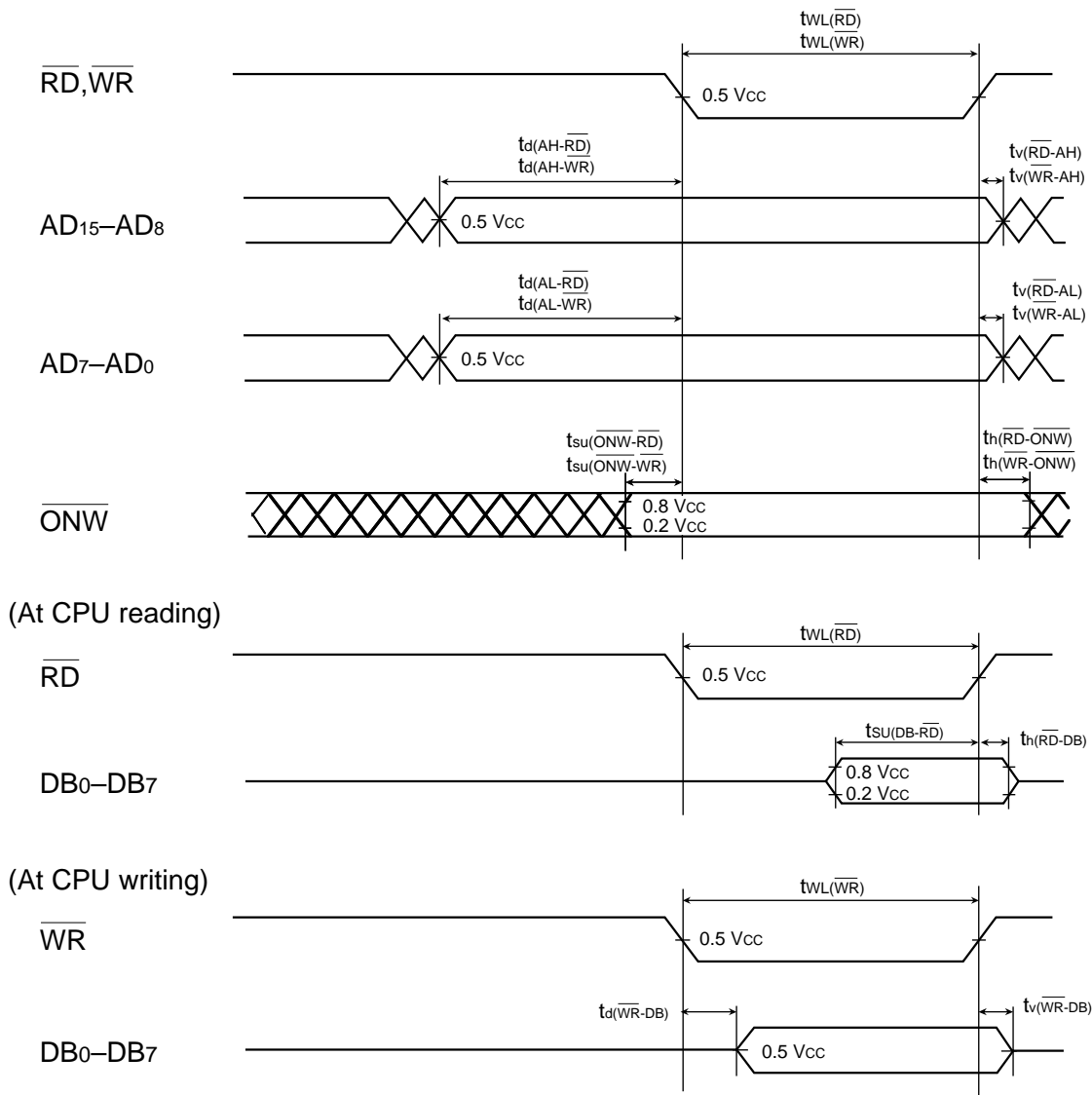
**(2)Timing Diagram in Memory Expansion Mode and Microprocessor Mode (a)**



**(3)Timing Diagram in Microprocessor Mode**



(4) Timing Diagram in Memory Expansion Mode and Microprocessor Mode (b)



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REVISION DESCRIPTION LIST

3806GROUP DATA SHEET

Rev. No.	Revision Description	Rev. date
1.0	First Edition	971128