

# PRELIMINARY

Notice. This is not a final specification.  
Some parametric limits are subject to change.

MITSUBISHI ICs (AV COMMON)

## M52795SP/FP

AV SWITCH with I2C BUS CONTROL

### DESCRIPTION

The M52795 is AV switch semiconductor integrated circuit with I2C bus control .

This IC contains 2-channels of 4-input audio switches and 2-channels of 4-input video switches. Each channel can be controlled independently .

The video switches contain amplifiers can be controlled a gain of output 0dB or 6dB .

### FEATURES

- Video and stereo sound switches in one package
- Wide frequency range ( video switch ).....DC~20MHz
- High separation ( video switch )  
.....Crosstalk -60dB ( typ. ) at 1MHz
- Two types of packages are provided : SDIP with a lead pitch of 1.778mm ( M52795SP ) ; and SOP with a lead pitch of 1.27mm ( M52795FP ) .

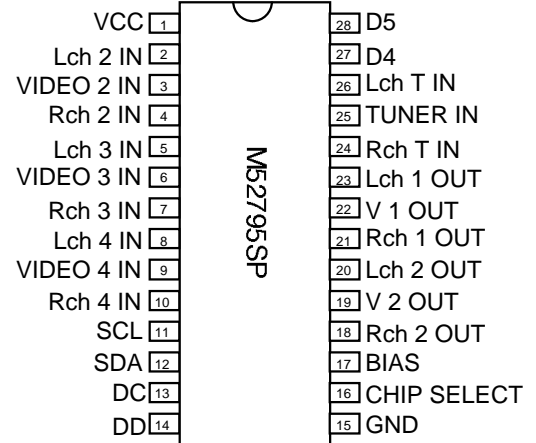
### APPLICATION

Video equipment

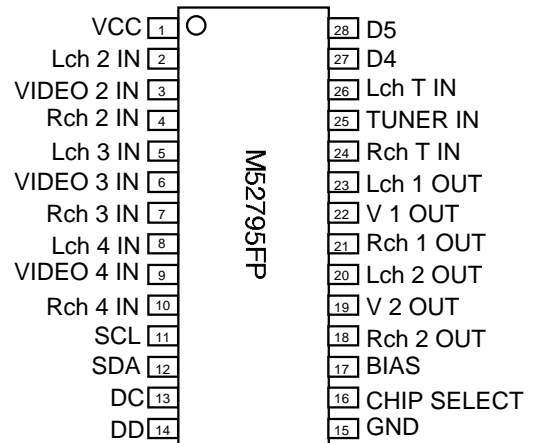
### RECOMMENDED OPERATING CONDITION

|                        |             |
|------------------------|-------------|
| Supply voltage         | 4.7V~9.3V   |
| Rated supply voltage   | 5V,9V       |
| Maximum output current | 32mA(at 9V) |

### PIN CONFIGURATION ( TOP VIEW )



### PIN CONFIGURATION ( TOP VIEW )



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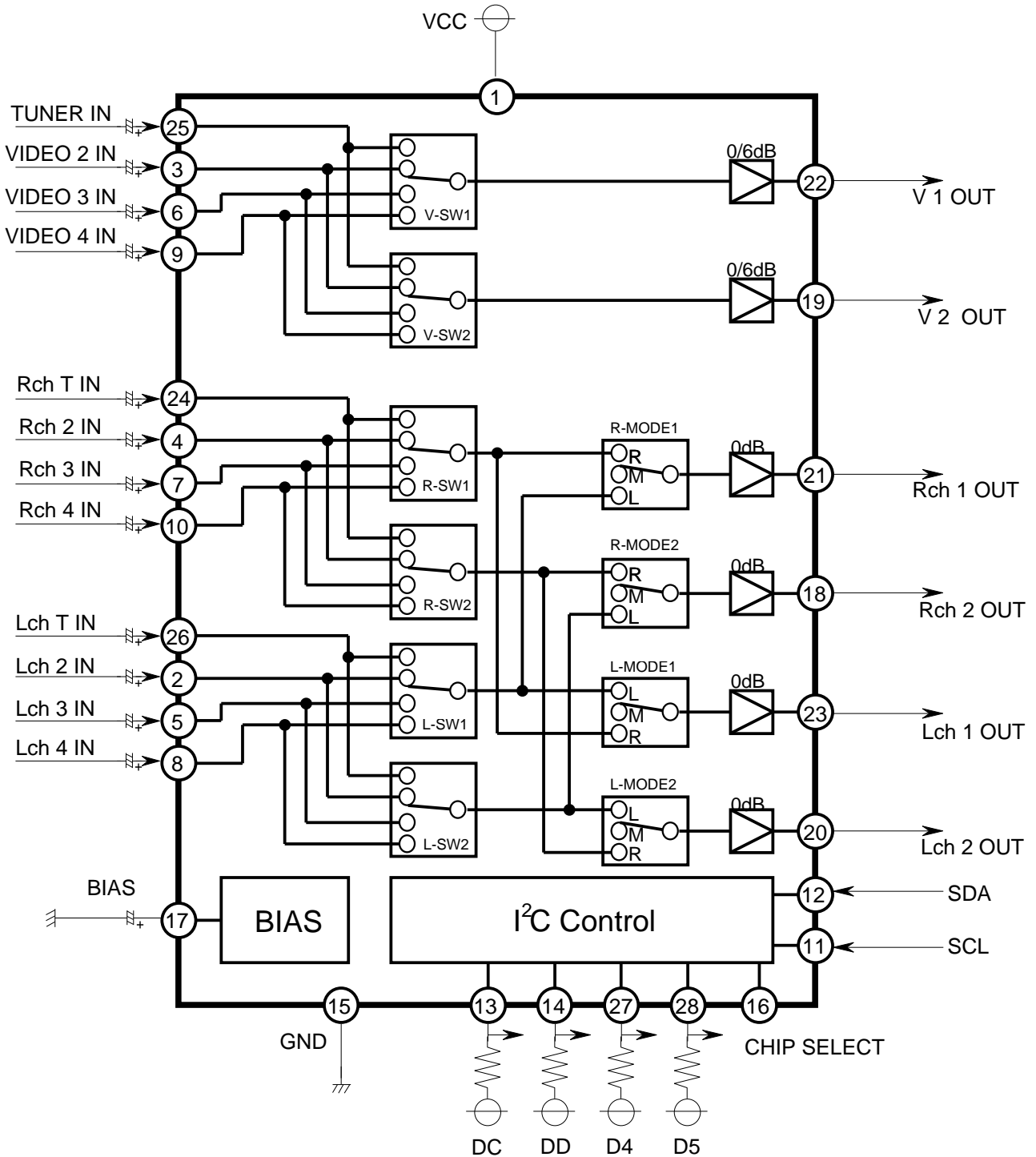
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### BLOCK DIAGRAM



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## DESCRIPTION OF PIN

| Pin No. | Name       | Peripheral circuit pins | DC voltage(V) | Remarks  |
|---------|------------|-------------------------|---------------|--|
| 1       | VCC        |                         | 9V            | 5~9V   |
| 2       | Lch 2 IN   |                         | 4.7V          |  |
| 4       | Rch 2 IN   |                         |               |  |
| 5       | Lch 3 IN   |                         |               |  |
| 7       | Rch 3 IN   |                         |               |  |
| 8       | Lch 4 IN   |                         |               |  |
| 10      | Rch 4 IN   |                         |               |  |
| 24      | Rch T IN   |                         |               |  |
| 26      | Lch T IN   |                         |               |  |
| 3       | VIDEO 2 IN |                         | 3.6V          | Clamp in   |
| 6       | VIDEO 3 IN |                         |               |  |
| 9       | VIDEO 4 IN |                         |               |  |
| 25      | TUNER IN   |                         |               |  |
| 11      | SCL        |                         |               | $V_{IL} \text{ max.}=1.5V$<br>$V_{IH} \text{ min.}=3.0V$   |
| 12      | SDA        |                         |               | $V_{IL} \text{ max.}=1.5V$<br>$V_{IH} \text{ min.}=3.0V$<br>$V_{OL} \text{ max.}=0.4V$<br>(at $I_{in}=3mA$ ) |
| 13      | DC         |                         |               | $V_{OL} \text{ max.}=0.4V$<br>(at $I_{in}=1mA$ )   |
| 14      | DD         |                         |               |  |
| 27      | D4         |                         |               |  |
| 28      | D5         |                         |               |  |

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## DESCRIPTION OF PIN (cont.)

| Pin No. | Name               | Peripheral circuit pins | DC voltage(V)        | Remarks  |
|---------|--------------------|-------------------------|----------------------|--|
| 15      | <b>GND</b>         |                         |                      |  |
| 16      | <b>CHIP SELECT</b> |                         |                      | SLAVE ADDRESS<br>0~1.5V-----90H<br>2.5V~Vcc----92H<br>OPEN-----90H |
| 17      | <b>BIAS</b>        |                         | 4.2V                 |  |
| 18      | <b>Rch 2 OUT</b>   |                         | 4.0V                 |  |
| 20      | <b>Lch 2 OUT</b>   |                         |                      |  |
| 21      | <b>Rch 1 OUT</b>   |                         |                      |  |
| 23      | <b>Lch 1 OUT</b>   |                         |                      |  |
| 19      | <b>V 2 OUT</b>     |                         | SYNC CHIP<br>DC=2.9V |  |
| 22      | <b>V 1 OUT</b>     |                         |                      |  |

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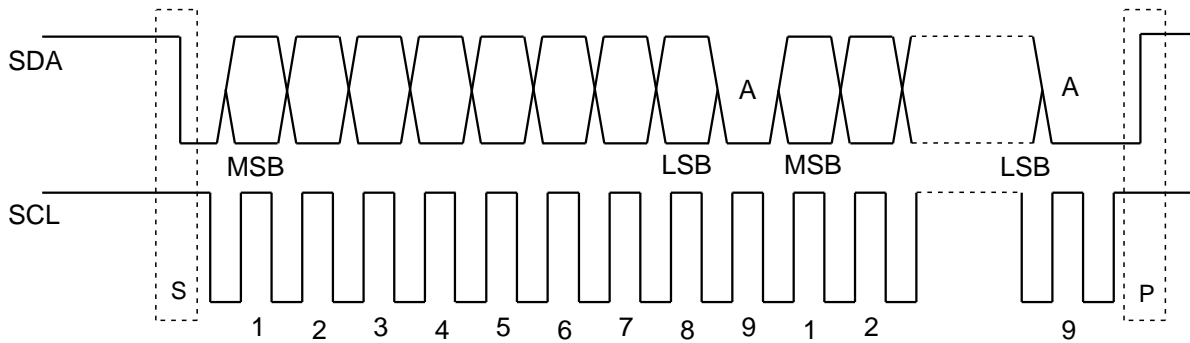
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## I<sup>2</sup>C BUS

I<sup>2</sup>C BUS (Inter IC BUS) is multi master bus system developed by PHILIPS. Two wires (SDA - serial data, SCL - serial clock) realize functions of start, stop, transferring data, synchronization and arbitration. The output stages of device connected to the bus must have an open drain or open collector in order to perform the wired-AND function.



S ; Start condition, a high to low transition of the SDA line while SCL is high  
P ; Stop condition, a low to high transition of the SDA line while SCL is high  
A : Acknowledge

Every byte put on the SDA line must be 8-bits long. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit (MSB) first. The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW.

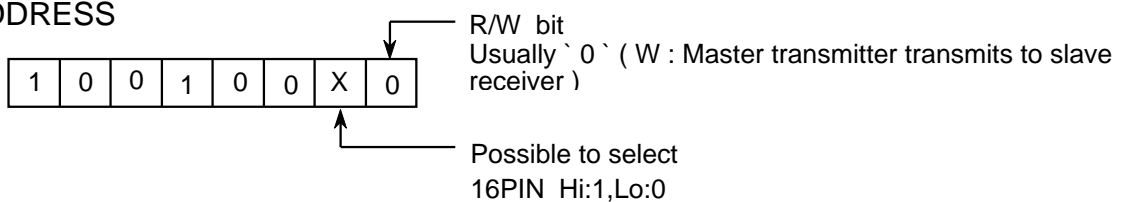
## CONTROL

This IC controls 2-channel switches with 2-byte data (DATA1 and DATA2). SW1 is controlled by DATA1, SW2 is controlled by DATA2.



S : Start  
A : Acknowledge  
P : Stop

## SLAVE ADDRESS



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## Data byte format

M52795 FUNCTION TABLE

|   |               |   |             |   |             |   |   |
|---|---------------|---|-------------|---|-------------|---|---|
| S | SLAVE ADDRESS | A | DATA(D7~D0) | A | DATA(DF~D8) | A | P |
|---|---------------|---|-------------|---|-------------|---|---|

SLAVE ADDRESS

|               |    |    |    |    |    |    |       |     |
|---------------|----|----|----|----|----|----|-------|-----|
| SLAVE ADDRESS | A6 | A5 | A4 | A3 | A2 | A1 | A0    | R/W |
|               | 1  | 0  | 0  | 1  | 0  | 0  | 0 / 1 | 0   |

DATA1(D7~D0) CONT

|           |            |    |     |     |        |    |          |    |
|-----------|------------|----|-----|-----|--------|----|----------|----|
| DATA CONT | D7         | D6 | D5  | D4  | D3     | D2 | D1       | D0 |
|           | AUDIO MODE |    | I/O | I/O | V AMP1 |    | SW1 CONT |    |

VIDEO SW1 CONT

|       |    |        |
|-------|----|--------|
| DATA  |    | OUT    |
| V-SW1 |    | V OUT1 |
| D1    | D0 |        |
| 0     | 0  | T IN   |
| 0     | 1  | V 2 IN |
| 1     | 0  | V 3 IN |
| 1     | 1  | V 4 IN |

OUT1 AMP GAIN CONT.

|      |        |
|------|--------|
| DATA | AMP    |
| D3   | V AMP1 |
| 0    | 0dB    |
| 1    | 6dB    |

I/O CONT.

|      |        |      |        |
|------|--------|------|--------|
| DATA | OUT    | DATA | OUT    |
| D5   | D5 OUT | D4   | D4 OUT |
| 0    | HI     | 0    | HI     |
| 1    | LO     | 1    | LO     |

AUDIO MODE1 CONT

|      |    |        |
|------|----|--------|
| DATA |    | MODE   |
| D7   | D6 |        |
| 0    | 0  | MUTE   |
| 0    | 1  | R/R    |
| 1    | 0  | L/L    |
| 1    | 1  | NORMAL |

AUDIO SW1 CONT

|      |    |           |           |           |           |           |           |           |           |
|------|----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| MODE |    | MUTE      |           | R/R       |           | L/L       |           | NORMAL    |           |
| DATA |    | OUT       |           | OUT       |           | OUT       |           | OUT       |           |
| D1   | D0 | Lch OUT 1 | Rch OUT 1 | Lch OUT 1 | Rch OUT 1 | Lch OUT 1 | Rch OUT 1 | Lch OUT 1 | Rch OUT 1 |
| 0    | 0  | MUTE      | MUTE      | Rch T IN  | Rch T IN  | Lch T IN  | Lch T IN  | Lch T IN  | Rch T IN  |
| 0    | 1  | MUTE      | MUTE      | Rch 2 IN  | Rch 2 IN  | Lch 2 IN  | Lch 2 IN  | Lch 2 IN  | Rch 2 IN  |
| 1    | 0  | MUTE      | MUTE      | Rch 3 IN  | Rch 3 IN  | Lch 3 IN  | Lch 3 IN  | Lch 3 IN  | Rch 3 IN  |
| 1    | 1  | MUTE      | MUTE      | Rch 4 IN  | Rch 4 IN  | Lch 4 IN  | Lch 4 IN  | Lch 4 IN  | Rch 4 IN  |

DATA2(DF~D8) CONT

|           |            |    |     |     |        |    |          |    |
|-----------|------------|----|-----|-----|--------|----|----------|----|
| DATA CONT | DF         | DE | DD  | DC  | DB     | DA | D9       | D8 |
|           | AUDIO MODE |    | I/O | I/O | V AMP2 |    | SW2 CONT |    |

VIDEO SW2 CONT

|       |    |        |
|-------|----|--------|
| DATA  |    | OUT    |
| V-SW2 |    | V OUT2 |
| D9    | D8 |        |
| 0     | 0  | T IN   |
| 0     | 1  | V 2 IN |
| 1     | 0  | V 3 IN |
| 1     | 1  | V 4 IN |

OUT2 AMP GAIN CONT.

|      |        |
|------|--------|
| DATA | AMP    |
| DB   | V AMP2 |
| 0    | 0dB    |
| 1    | 6dB    |

I/O CONT.

|      |        |      |        |
|------|--------|------|--------|
| DATA | OUT    | DATA | OUT    |
| DD   | DD OUT | DC   | DC OUT |
| 0    | HI     | 0    | HI     |
| 1    | LO     | 1    | LO     |

AUDIO MODE CONT

|      |    |        |
|------|----|--------|
| DATA |    | MODE   |
| DF   | DE |        |
| 0    | 0  | MUTE   |
| 0    | 1  | R/R    |
| 1    | 0  | L/L    |
| 1    | 1  | NORMAL |

AUDIO SW2 CONT

|      |    |           |           |           |           |           |           |           |           |
|------|----|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| MODE |    | MUTE      |           | R/R       |           | L/L       |           | NORMAL    |           |
| DATA |    | OUT       |           | OUT       |           | OUT       |           | OUT       |           |
| D9   | D8 | Lch OUT 2 | Rch OUT 2 | Lch OUT 2 | Rch OUT 2 | Lch OUT 2 | Rch OUT 2 | Lch OUT 2 | Rch OUT 2 |
| 0    | 0  | MUTE      | MUTE      | Rch T IN  | Rch T IN  | Lch T IN  | Lch T IN  | Lch T IN  | Rch T IN  |
| 0    | 1  | MUTE      | MUTE      | Rch 2 IN  | Rch 2 IN  | Lch 2 IN  | Lch 2 IN  | Lch 2 IN  | Rch 2 IN  |
| 1    | 0  | MUTE      | MUTE      | Rch 3 IN  | Rch 3 IN  | Lch 3 IN  | Lch 3 IN  | Lch 3 IN  | Rch 3 IN  |
| 1    | 1  | MUTE      | MUTE      | Rch 4 IN  | Rch 4 IN  | Lch 4 IN  | Lch 4 IN  | Lch 4 IN  | Rch 4 IN  |

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## ELECTRICAL CHARACTERISTICS

(Ta=25°C, Vcc=9V, unless otherwise noted)

| Parameter                 | Symbol | Test condition                                  | Min. | Typ. | Max. | Unit |
|---------------------------|--------|---|------|------|------|------|
| Supply voltage            | Vcc    |   | 4.7  | -    | 9.3  | V    |
| Circuit current           | Icc    | Vcc=9V, Vin=0Vp-p, RI=                          | -    | 32   | 42   | mA   |
|                           |        | Vcc=5V, Vin=0Vp-p, RI=                          | -    | 28   | 37   |      |
| VIDEO                     |        |   |      |      |      |      |
| Voltage gain              | G      | f=100kHz, 1Vp-p (0dB)(T→V1OUT)                  | -0.5 | 0    | 0.5  | dB   |
|                           |        | f=100kHz, 1Vp-p (6dB)(T→V1OUT)                  | 5.5  | 6    | 6.5  |      |
| Frequency characteristics | F      | f=10MHz/100kHz, 1Vp-p (0dB)(T→V1OUT)            | -2.0 | 0    | 2.0  | dB   |
|                           |        | f=10MHz/100kHz, 1Vp-p (6dB)(T→V1OUT)            | -2.0 | 0    | 2.0  |      |
| Dynamic Range             | D      | Vcc=9V(0dB)(T→V1OUT)                            | 4    | -    | -    | Vp-p |
|                           |        | Vcc=5V(0dB)(T→V1OUT)                            | 2    | -    | -    |      |
| Input impedance           | ZIV    | Clamp in(T, V2, V3, V4)                         | -    | -    | -    | k    |
| Crosstalk                 | CT     | f=1MHz, 1Vp-p T→V1OUT (at V2 mode)              | -    | -60  | -54  | dB   |
| AUDIO                     |        |   |      |      |      |      |
| Voltage gain              | G      | f=1kHz, 1Vp-p (Vcc9V)(RT→R1OUT)                 | -0.5 | 0    | 0.5  | dB   |
|                           |        | f=1kHz, 1Vp-p (Vcc5V)(RT→R1OUT)                 | -0.5 | 0    | 0.5  |      |
| Frequency characteristics | F      | f=100kHz/1kHz, 1Vp-p(RT→R1OUT)                  | -2.0 | 0    | 1.0  | dB   |
| Total harmonic distortion | THD    | f=1kHz, 2Vp-p, at 400HzHPF+30kHzLPF (RT→R1OUT)  | -    | 0.01 | 0.05 | %    |
| Dynamic Range             | D      | f=1kHz, Maximum with distortion<0.5% (RT→R1OUT) | 5.5  | 6.0  | -    | Vp-p |
| Output DC offset voltage  | VOFF   | (MODE:RT, R2, R3, R4→R1OUT)                     | -20  | 0    | 20   | mV   |
| Input impedance           | Z1     | (RT, R2, R3, R4, LT, L2, L3, L4)                | 22   | 30   | 38   | k    |
| Crosstalk                 | CT     | 1kHz, 1Vp-p RT→R1OUT(at R2 mode)                | -    | -90  | -84  | dB   |

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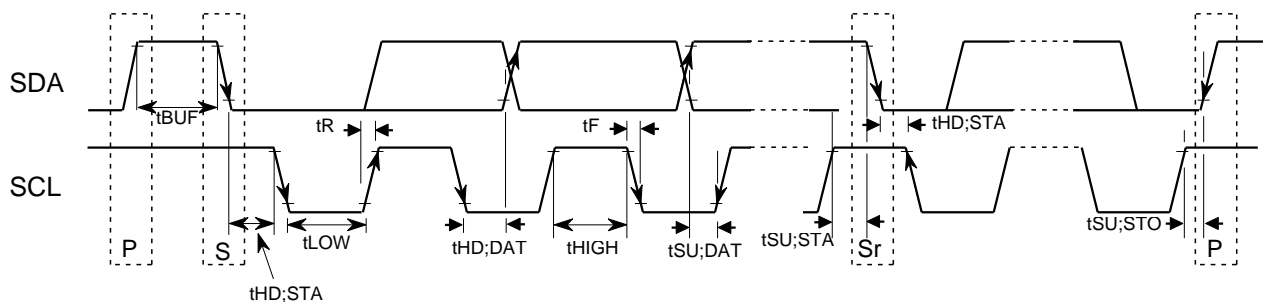
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## ELECTRICAL CHARACTERISTICS

(Ta=25°C, Vcc=9V, unless otherwise noted)

| Parameter  | Symbol              | Test condition   | Min. | Typ. | Max. | Unit |
|--|---------------------|------------------|------|------|------|------|
| I2C BUS CONTROL SIGNAL                                       |                     |                  |      |      |      |      |
| Max. input high voltage                                      | V <sub>IH</sub>     |                  | 3.0  | -    | 5.0  | V    |
| Min. input low voltage                                       | V <sub>IL</sub>     |                  | 0.0  | -    | 1.5  |      |
| Low level output voltage(SDA)                                | V <sub>OL</sub>     | SDA = 3mA        | 0.0  | -    | 0.4  |      |
| High level input current                                     | I <sub>IH</sub>     | SDA, SCL = 4.5 V | -10  | -    | 10   | μA   |
| Low level input current                                      | I <sub>IL</sub>     | SDA, SCL = 0.4 V | -10  | -    | 10   |      |
| SCL clock frequency  | f <sub>SCL</sub>    |                  | 0.0  | -    | 100  | kHz  |
| Time of bus must be free before a new transmission can start | t <sub>BUF</sub>    |                  | 4.7  | -    | -    | μS   |
| Hold time at start condition                                 | t <sub>HD;STA</sub> |                  | 4.0  | -    | -    |      |
| The low period of the clock                                  | t <sub>LOW</sub>    |                  | 4.7  | -    | -    |      |
| The high period of the clock                                 | t <sub>HIGH</sub>   |                  | 4.0  | -    | -    |      |
| Setup time for start condition                               | t <sub>SU;STA</sub> |                  | 4.7  | -    | -    | nS   |
| Hold time DATA   | t <sub>HD;DAT</sub> |                  | 5.0  | -    | -    |      |
| Setup time DATA  | t <sub>SU;DAT</sub> |                  | 250  | -    | -    |      |
| Rise time of both SDA and SCL line                           | t <sub>R</sub>      |                  | -    | -    | 1000 |      |
| Fall time of both SDA and SCL line                           | t <sub>F</sub>      |                  | -    | -    | 300  |      |
| Setup time for stop condition                                | t <sub>SU;STO</sub> |                  | 4.0  | -    | -    | μS   |

## I<sup>2</sup>C BUS CONTROL SIGNAL





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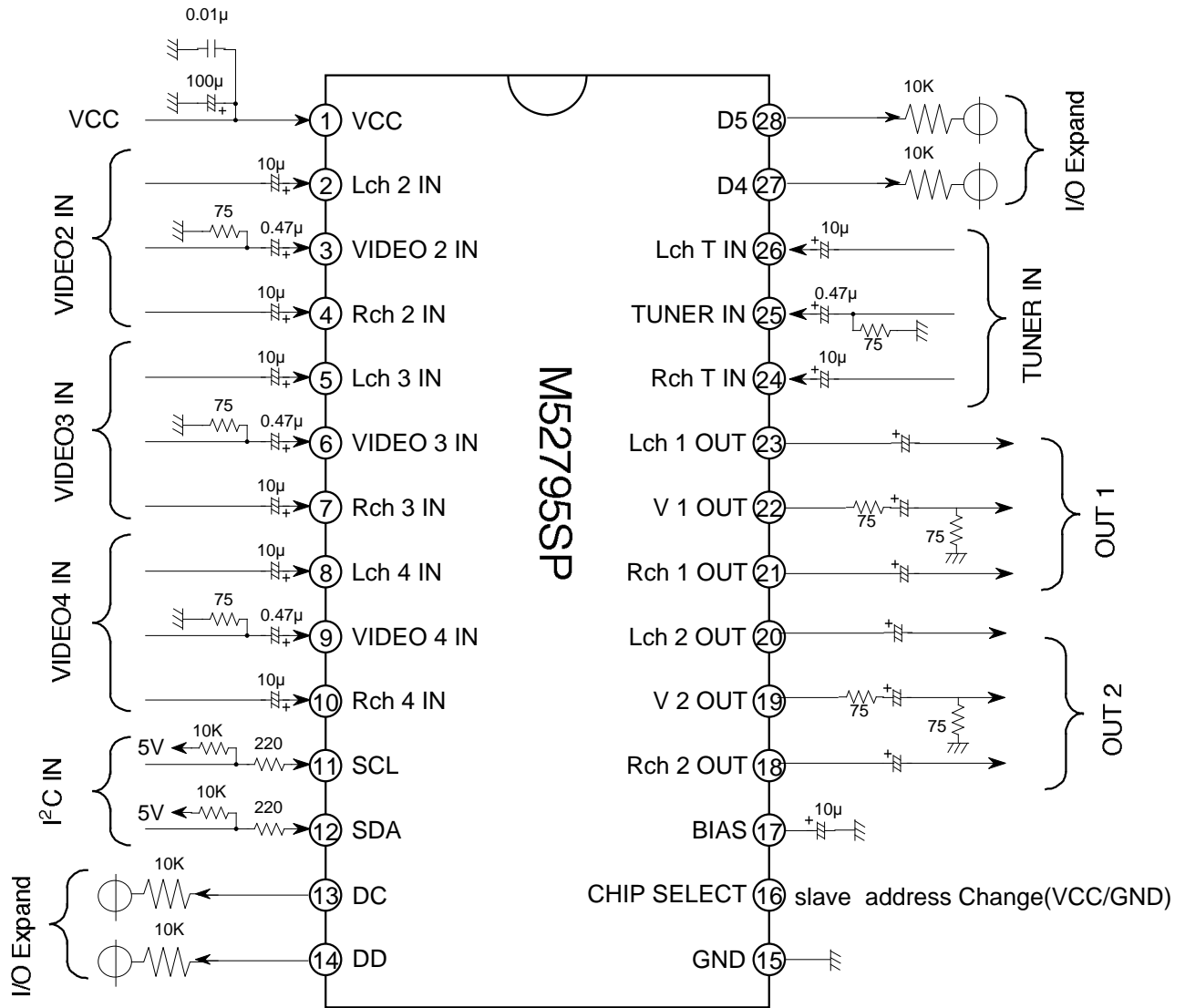
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### Application Circuit Example



Note how to use this IC

Input signal with sufficient low impedance to input terminal.

The capacitance of output terminal as small as possible.

Set the capacitance between Vcc and GND near the pins if possible.

Assign an area as large as possible for grounding.

Power-on Reset

The M52795 has an internal power-on reset function that sets each control register to "0" during IC power ON.

The power-on reset  $V_{TH}$  has 2.5V.