

M54977P

BI-CMOS 12-BIT SERIAL-INPUT LATCHED DRIVER

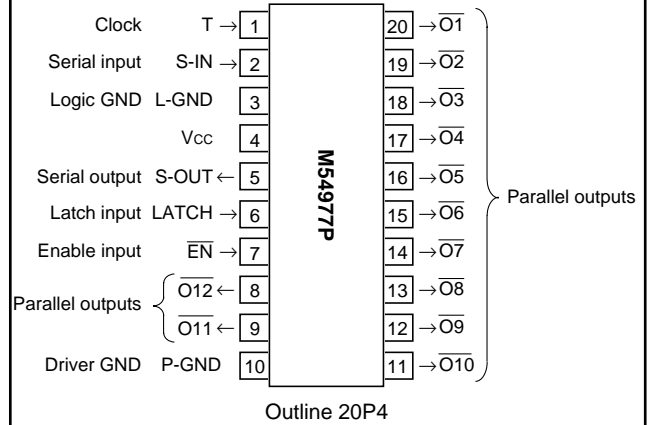
DESCRIPTION

The M54977P is a semiconductor integrated circuit fabricated using Bi-CMOS technology. It contains a serial input to serial/parallel output 12-bit CMOS shift register and CMOS latch as well as bipolar 12-bit parallel-output driver.

FEATURES

- Serial input to serial/parallel output
- Cascade connections possible through serial output
- Latch circuit included for each stage
- Enable input for output control
- Low supply current $I_{CC} \geq 10\mu A$ at standby
- Serial input/output level is compatible with standard CMOS
- Driver : Withstand voltage $BV_{CEO} \geq 30V$
Large drive current ($I_{O(max)}=200mA$)
- Wide operating temperature range $T_a=-20 - +75^\circ C$

PIN CONFIGURATION (TOP VIEW)



APPLICATION

Thermal printer head dot driver, Serial-to parallel conversion, Relay, solenoid driver

Using a number of M54977P units for bit expansion in series will entail connecting serial output (S-OUT) to S-IN of the next-stage M54977P.

FUNCTION

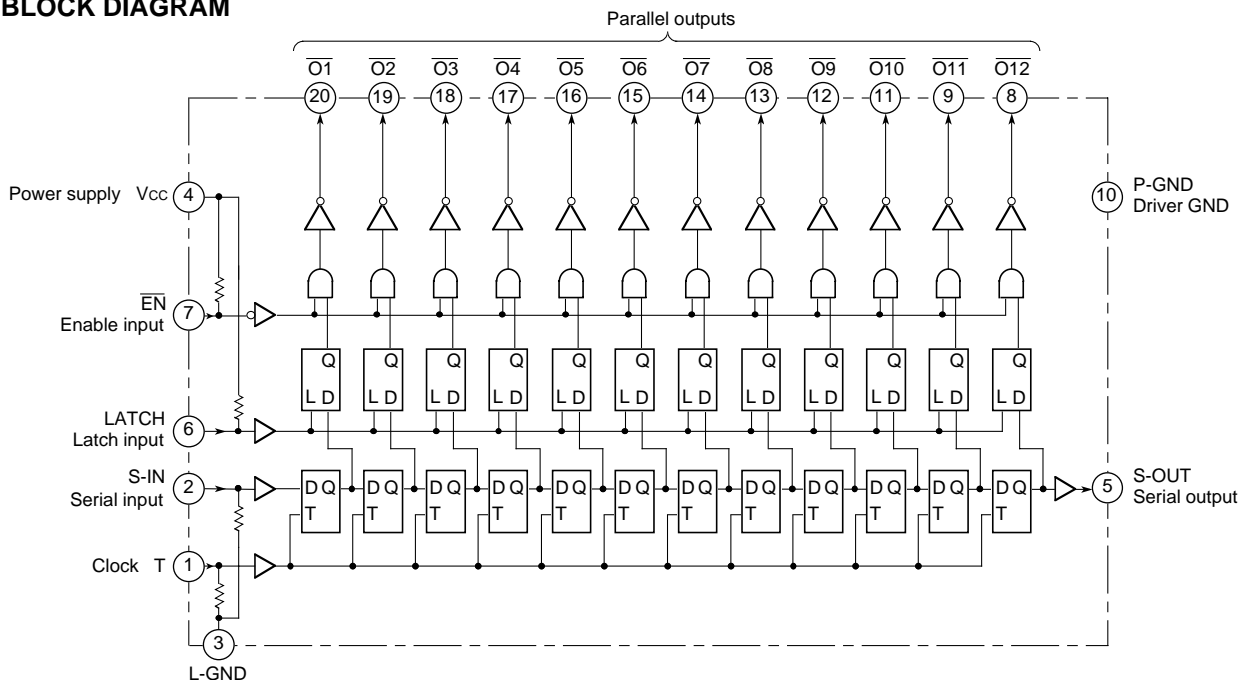
The M54977P consists of an 12-bit D-type flip-flop, the output of which is connected to 12 latches.

In parallel output, when the latch input is set to "H" and the output-control input (enable input \overline{EN}) is "L", a clock pulse changing from "L" to "H" will cause the serial data input signal to appear at output $\overline{O1}$, and the data will be shifted in order at outputs $\overline{O2} - \overline{O12}$.

When data is applied to the serial data input (S-IN) and a clock pulse is applied to clock input (T), an "L" to "H" change of the clock will cause the data input signals to enter the internal shift registers and the data in the shift registers will be shifted in order.

The parallel output will yield a signal that is inverted with respect to the serial data input.

BLOCK DIAGRAM



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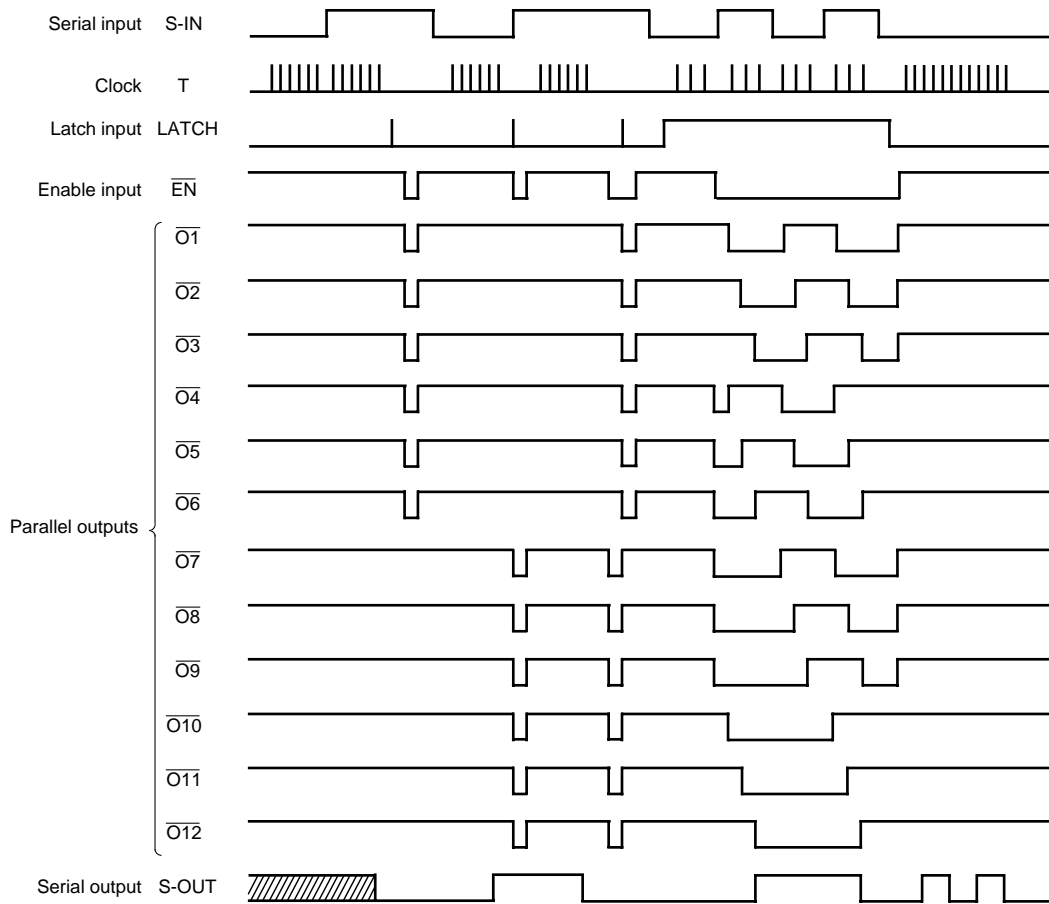
Setting the LATCH input to "L" will prevent data from entering the latch.

When the \overline{EN} input is set to "H", all outputs ($\overline{O1} - \overline{O12}$) will be set to OFF. Since the internal logic state of the IC is uncertain at power-on time, set the \overline{EN} input to "H" (and outputs $\overline{O1} - \overline{O12}$ will set to OFF) until the input data is set and the internal logic state

has been determined.

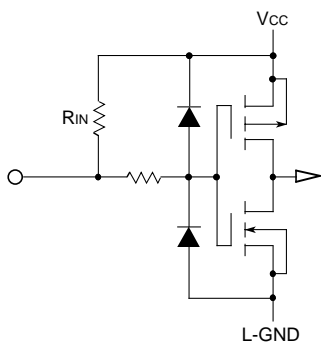
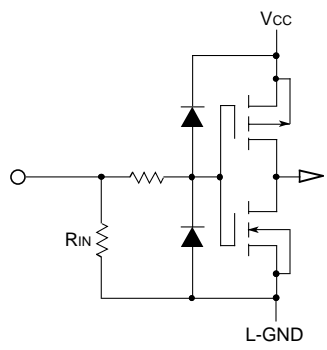
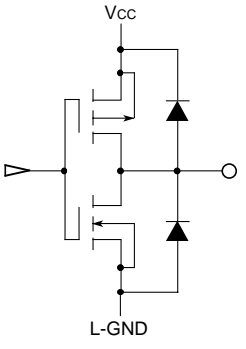
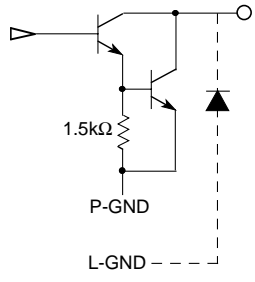
L-GND is the ground of the CMOS logic circuit section and P-GND is the ground for the output driver section ($\overline{O1} - \overline{O12}$), which is made up of bipolar transistors that are capable of driving large currents.

TIMING CHART



*The state of the shaded part is unstable.

INPUT/OUTPUT CIRCUIT DIAGRAM

<p>1</p> <p>Inputs with pullup resistor ($\overline{\text{EN}}$, LATCH)</p> 	<p>2</p> <p>Inputs with pulldown resistor (T, S-IN)</p> 
<p>3</p> <p>Serial output (S-OUT)</p> 	<p>4</p> <p>Parallel output (O1 - O12)</p> 

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ABSOLUTE MAXIMUM RATINGS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		0 – 7	V
Vi	Input voltage		0 – Vcc	V
Vo	Output voltage	S-OUT	0 – Vcc	V
		$\overline{O1} - \overline{O12}$: OFF	0 – 30	
Io	Output current		250	mA
Pd	Power dissipation	Ta=25°C	1.25	W
Topr	Operating temperature		-20 – 75	°C
Tstg	Storage temperature		-55 – 125	°C

RECOMMENDED OPERATING CONDITION (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply voltage		4	5	6	V
Vo	Applied output voltage	$\overline{O1} - \overline{O12}$: OFF			30	V
Io	Output current (per circuit)	All outputs go in the ON state simultaneously. Duty cycle < 20%			200	mA

ELECTRICAL CHARACTERISTICS (Ta=25°C, Vcc=5V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VIH	High-level input voltage		Ta=-20 – 75°C, Vcc=4 – 6V	0.7Vcc		Vcc	V
VIL	Low-level input voltage			0		0.3Vcc	V
RIN	Input resistance			50			kΩ
VOH	High-level output voltage	S-OUT	Io ≤ 1μA	4.9			V
VOL	Low-level output voltage	S-OUT				0.1	V
IOH	High-level output current	S-OUT	VOH=4.5V	-100			μA
IOL	Low-level output current	S-OUT	VOL=0.4V	400			μA
VOL1	Low-level output voltage	$\overline{O1} - \overline{O12}$	IoL=100mA			1.2	V
VOL2			IoL=200mA			1.4	V
IOLK	Output leak current	$\overline{O1} - \overline{O12}$	Vo=30V			50	μA
ICC1	Supply current		Input: open, All driver outputs: OFF			10	μA
ICC2			One driver output is ON.			1.25	mA

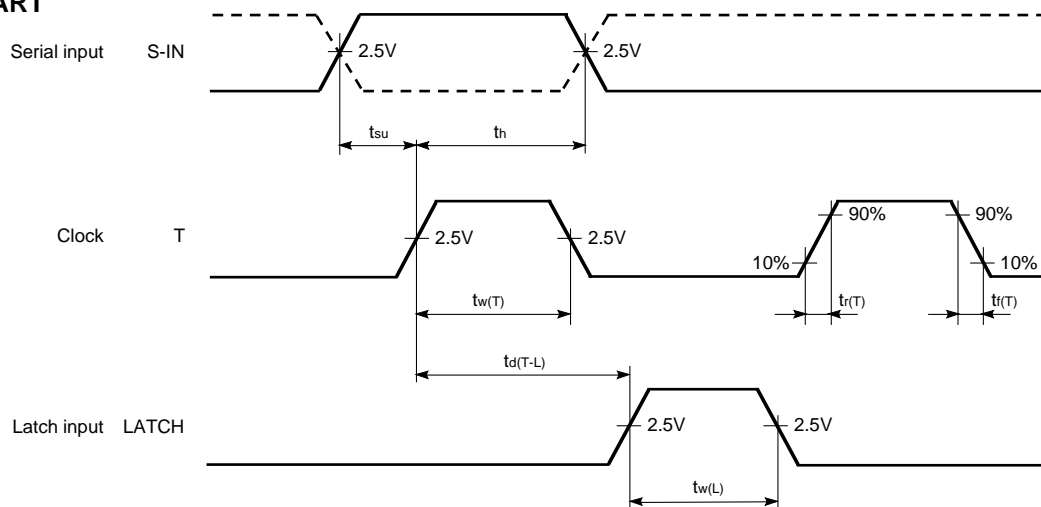
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TIMING REQUIREMENTS (Ta=-20 to 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
f(T)	Clock frequency	Input duty cycle: 40 – 60%			2	MHz
tw(T)	Clock pulse width		200			ns
tw(L)	Latch pulse width		200			ns
tsu	Data setup time		100			ns
th	Data hold time		100			ns
td(T-L)	Clock-latch time		400			ns
tr(T)	Clock pulse rise time				500	ns
tf(T)	Clock pulse fall time				500	ns

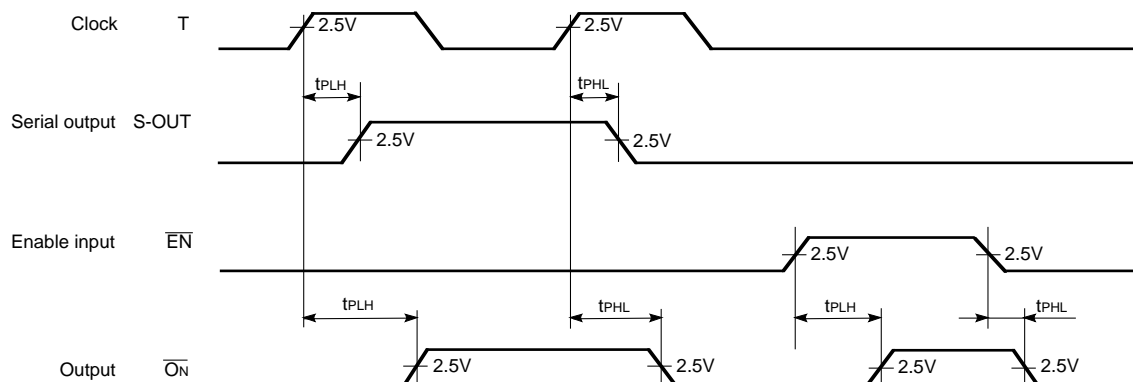
TIMING CHART



SWITCHING CHARACTERISTICS (Ta=25°C, Vcc=5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tPLH	Low-to-high-level output propagation time, From input T to output S-OUT	VIH=5V		(0.15)	0.3	μs
tPHL	High-to-low-level output propagation time, From input T to output S-OUT	VIL=0V		(0.15)	0.3	μs
tPLH	Low-to-high-level output propagation time, From input T to output ON	RL(S-OUT)=∞		(2)	10	μs
tPHL	High-to-low-level output propagation time, From input T to output ON	RL(ON)=100Ω		(0.5)	2	μs
tPLH	Low-to-high-level output propagation time, From input EN to output ON	(N=1-12)		(2)	10	μs
tPHL	High-to-low-level output propagation time, From input EN to output ON	CL=15pF		(0.5)	2	μs

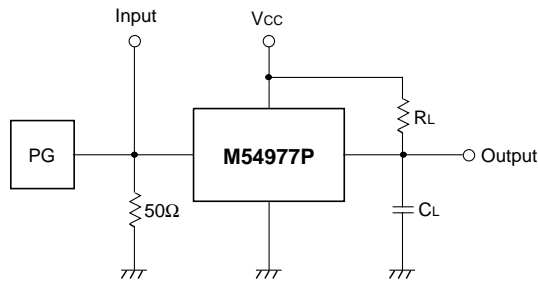
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TEST CIRCUIT



- The input waveform: $t_r \leq 20\text{ns}$, $t_f \leq 20\text{ns}$
- The capacitance C_L includes the wiring stray capacitance and probe input capacitance.

TYPICAL CHARACTERISTICS

