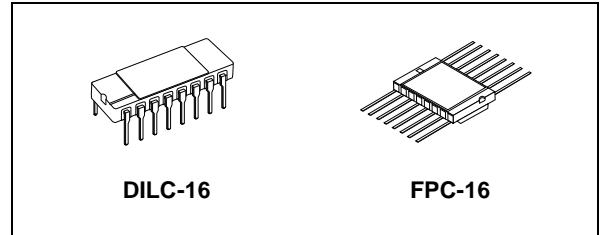


RAD-HARD 12 STAGE BINARY COUNTER

- HIGH SPEED:
 $f_{MAX} = 70 \text{ MHz (TYP.) at } V_{CC} = 6V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A (MAX.) at } T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 4\text{mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2V \text{ to } 6V$
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 4040
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9204-069

DESCRIPTION

The M54HC4040 is an high speed CMOS 12 STAGE BINARY COUNTER fabricated with silicon gate C²MOS technology.



ORDER CODES

| PACKAGE | FM | EM |
|---------|------------|-------------|
| DILC | M54HC4040D | M54HC4040D1 |
| FPC | M54HC4040K | M54HC4040K1 |

A clear input is used to reset the counter to the all low level state. A high level on CLEAR accomplishes the reset function. A negative transition on the CLOCK input increments the counter by one.

For M54HC4040 each division stage has an output; the final frequency is $1/4096 f_{IN}$. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION

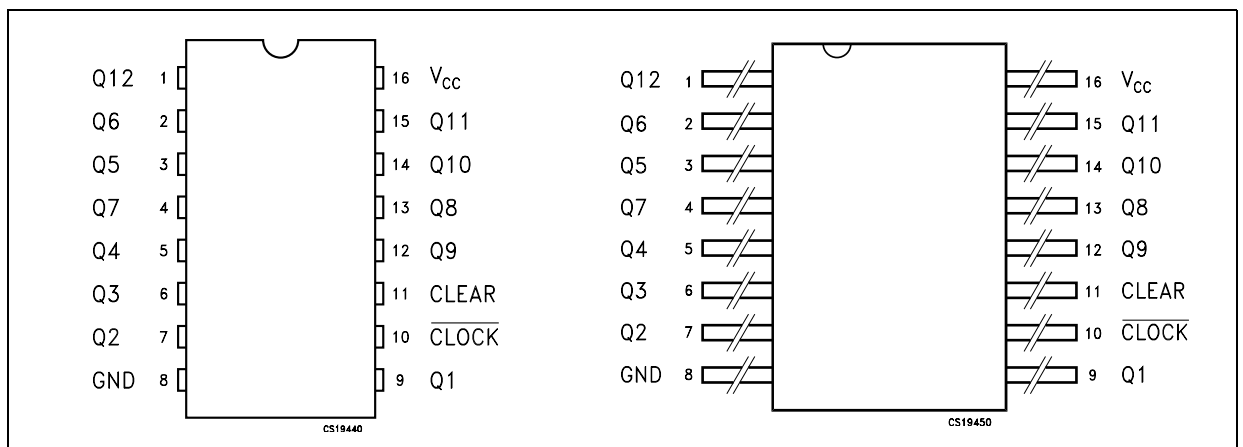


Figure 1: IEC Logic Symbols

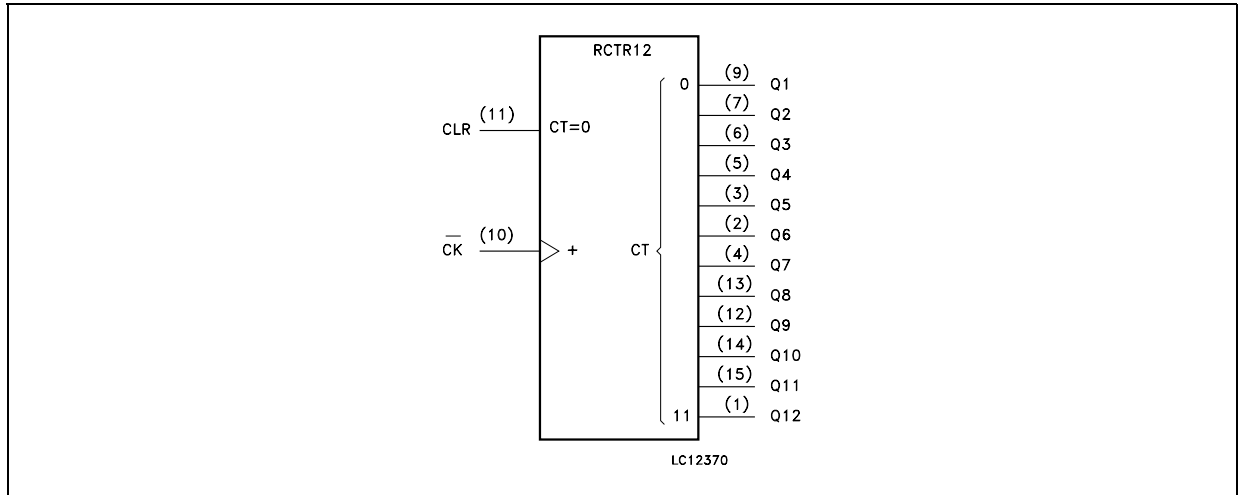


Figure 2: Input And Output Equivalent Circuit

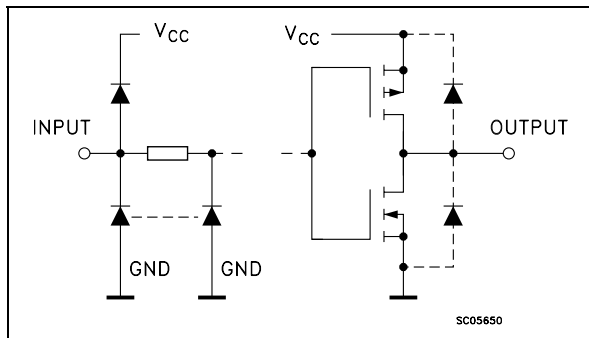


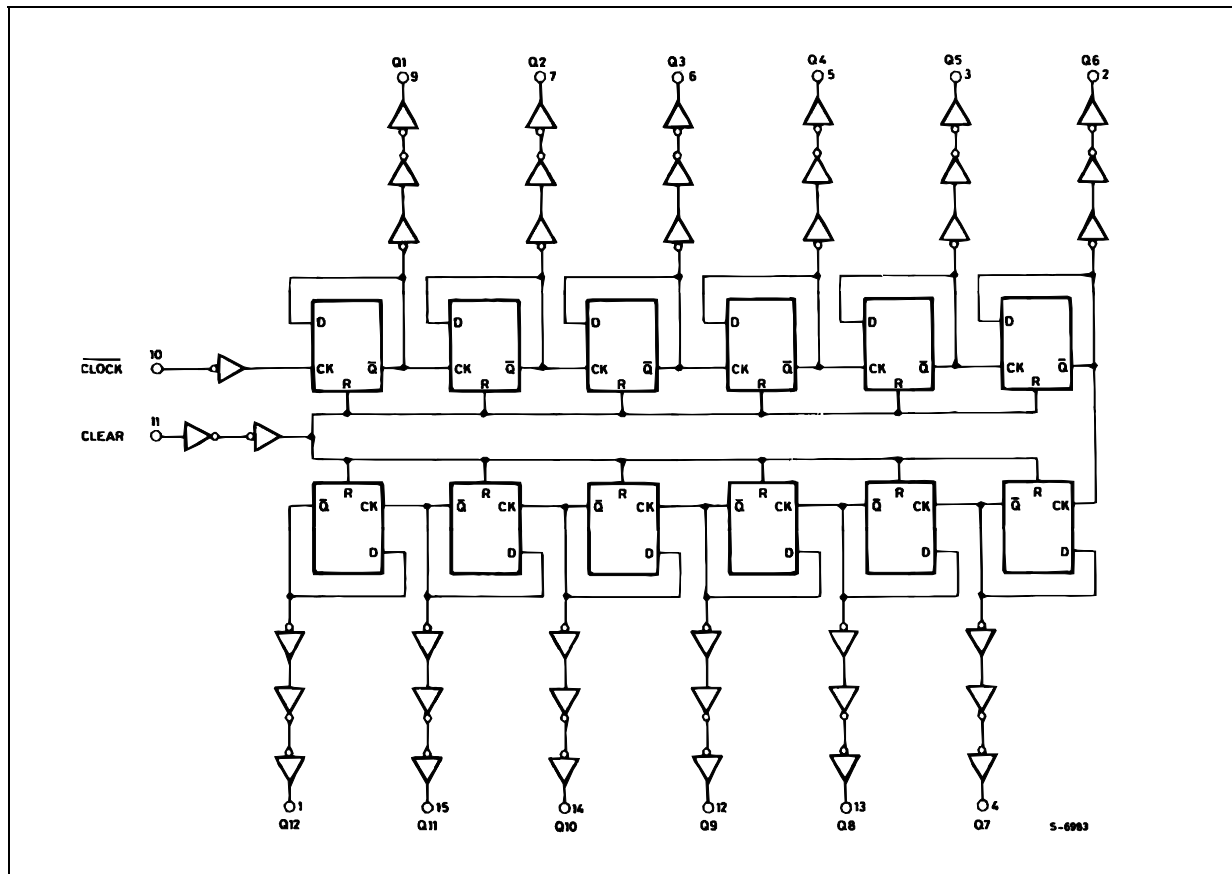
Table 1: Pin Description

| PIN N° | SYMBOL | NAME AND FUNCTION |
|--|---------------------------|---|
| 9, 7, 6, 5, 3, 2, 4, 13, 12, 14, 15, 1 | Q1 to Q12 | Parallel Outputs |
| 10 | $\overline{\text{CLOCK}}$ | Clock Input (LOW to HIGH, Edge Triggered) |
| 11 | CLEAR | Reset Inputs |
| 8 | GND | Ground (0V) |
| 16 | V _{CC} | Positive Supply Voltage |

Table 2: Truth Table

| $\overline{\text{CLOCK}}$ | CLEAR | OUTPUT STATE |
|---------------------------|-------|-----------------------|
| X | H | ALL OUTPUTS = "L" |
| | L | NO CHANGE |
| | L | ADVANCE TO NEXT STATE |

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 3: Absolute Maximum Ratings

| Symbol | Parameter | Value | Unit |
|-------------------------------------|--------------------------------------|-------------------------------|------|
| V _{CC} | Supply Voltage | -0.5 to +7 | V |
| V _I | DC Input Voltage | -0.5 to V _{CC} + 0.5 | V |
| V _O | DC Output Voltage | -0.5 to V _{CC} + 0.5 | V |
| I _{IK} | DC Input Diode Current | ± 20 | mA |
| I _{OK} | DC Output Diode Current | ± 20 | mA |
| I _O | DC Output Current | ± 25 | mA |
| I _{CC} or I _{GND} | DC V _{CC} or Ground Current | ± 50 | mA |
| P _D | Power Dissipation | 300 | mW |
| T _{stg} | Storage Temperature | -65 to +150 | °C |
| T _L | Lead Temperature (10 sec) | 265 | °C |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

| Symbol | Parameter | Value | Unit | |
|------------|--------------------------|-----------------|-----------|----|
| V_{CC} | Supply Voltage | 2 to 6 | V | |
| V_I | Input Voltage | 0 to V_{CC} | V | |
| V_O | Output Voltage | 0 to V_{CC} | V | |
| T_{op} | Operating Temperature | -55 to 125 | °C | |
| t_r, t_f | Input Rise and Fall Time | $V_{CC} = 2.0V$ | 0 to 1000 | ns |
| | | $V_{CC} = 4.5V$ | 0 to 500 | ns |
| | | $V_{CC} = 6.0V$ | 0 to 400 | ns |

Table 5: DC Specifications

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|----------|---------------------------|-----------------|-----------------------|--------------------|------|-----------|-------------|---------|--------------|---------|---------|
| | | V_{CC} (V) | | $T_A = 25^\circ C$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| V_{IH} | High Level Input Voltage | 2.0 | | 1.5 | | | 1.5 | | 1.5 | | V |
| | | 4.5 | | 3.15 | | | 3.15 | | 3.15 | | |
| | | 6.0 | | 4.2 | | | 4.2 | | 4.2 | | |
| V_{IL} | Low Level Input Voltage | 2.0 | | | | 0.5 | | 0.5 | | 0.5 | V |
| | | 4.5 | | | | 1.35 | | 1.35 | | 1.35 | |
| | | 6.0 | | | | 1.8 | | 1.8 | | 1.8 | |
| V_{OH} | High Level Output Voltage | 2.0 | $I_O = -20 \mu A$ | 1.9 | 2.0 | | 1.9 | | 1.9 | | V |
| | | 4.5 | $I_O = -20 \mu A$ | 4.4 | 4.5 | | 4.4 | | 4.4 | | |
| | | 6.0 | $I_O = -20 \mu A$ | 5.9 | 6.0 | | 5.9 | | 5.9 | | |
| | | 4.5 | $I_O = -4.0 mA$ | 4.18 | 4.31 | | 4.13 | | 4.10 | | |
| | | 6.0 | $I_O = -5.2 mA$ | 5.68 | 5.8 | | 5.63 | | 5.60 | | |
| V_{OL} | Low Level Output Voltage | 2.0 | $I_O = 20 \mu A$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | V |
| | | 4.5 | $I_O = 20 \mu A$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 6.0 | $I_O = 20 \mu A$ | | 0.0 | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 | $I_O = 4.0 mA$ | | 0.17 | 0.26 | | 0.33 | | 0.40 | |
| | | 6.0 | $I_O = 5.2 mA$ | | 0.18 | 0.26 | | 0.33 | | 0.40 | |
| I_I | Input Leakage Current | 6.0 | $V_I = V_{CC}$ or GND | | | ± 0.1 | | ± 1 | | ± 1 | μA |
| I_{CC} | Quiescent Supply Current | 6.0 | $V_I = V_{CC}$ or GND | | | 4 | | 40 | | 80 | μA |

Table 6: AC Electrical Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

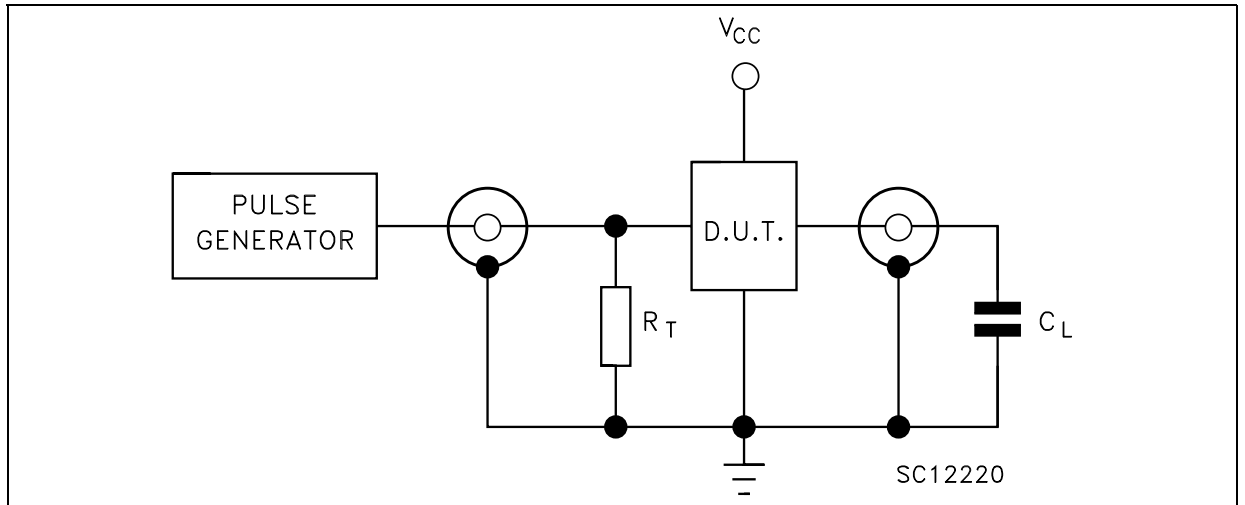
| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|--------------------------|---|-----------------|--|--------------------------|------|------|-----------------------------|------|------------------------------|------|------|
| | | V_{CC} (V) | | $T_A = 25^\circ\text{C}$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| t_{TLH} t_{THL} | Output Transition Time | 2.0 | | | 30 | 75 | | 95 | | 110 | ns |
| | | 4.5 | | | 8 | 15 | | 19 | | 22 | |
| | | 6.0 | | | 7 | 13 | | 16 | | 19 | |
| t_{PLH} t_{PHL} | Propagation Delay Time ($Q_n - Q_{n+1}$) | 2.0 | | | 20 | 50 | | 65 | | 75 | ns |
| | | 4.5 | | | 5 | 10 | | 13 | | 15 | |
| | | 6.0 | | | 4 | 9 | | 11 | | 13 | |
| t_{PLH} t_{PHL} | Propagation Delay Time (CLOCK Q1) | 2.0 | | | 48 | 145 | | 180 | | 220 | ns |
| | | 4.5 | | | 17 | 29 | | 36 | | 44 | |
| | | 6.0 | | | 13 | 25 | | 31 | | 38 | |
| t_{PHL} | Propagation Delay Time (CLEAR - Q_n) | 2.0 | | | 56 | 140 | | 175 | | 210 | ns |
| | | 4.5 | | | 18 | 28 | | 35 | | 42 | |
| | | 6.0 | | | 15 | 24 | | 30 | | 36 | |
| f_{MAX} | Maximum Clock Frequency | 2.0 | | 6.0 | 15 | | 4.8 | | 4 | | MHz |
| | | 4.5 | | 30 | 65 | | 24 | | 20 | | |
| | | 6.0 | | 35 | 70 | | 28 | | 24 | | |
| $t_{W(H)}$ $t_{W(L)}$ | Minimum Pulse Width (CLOCK) | 2.0 | | | 40 | 75 | | 95 | | 110 | ns |
| | | 4.5 | | | 8 | 15 | | 19 | | 22 | |
| | | 6.0 | | | 7 | 13 | | 16 | | 19 | |
| $t_{W(H)}$ | Minimum Pulse Width (CLEAR) | 2.0 | | | 70 | 175 | | 220 | | 265 | ns |
| | | 4.5 | | | 19 | 35 | | 44 | | 53 | |
| | | 6.0 | | | 16 | 30 | | 37 | | 45 | |
| t_{REM} | Minimum Removal Time | 2.0 | | | | 25 | | 30 | | 40 | ns |
| | | 4.5 | | | | 5 | | 6 | | 8 | |
| | | 6.0 | | | | 5 | | 5 | | 7 | |

Table 7: Capacitive Characteristics

| Symbol | Parameter | Test Condition | | Value | | | | | | Unit | |
|----------|--|-----------------|--|--------------------------|------|------|-----------------------------|------|------------------------------|------|------|
| | | V_{CC} (V) | | $T_A = 25^\circ\text{C}$ | | | -40 to 85°C | | -55 to 125°C | | |
| | | | | Min. | Typ. | Max. | Min. | Max. | Min. | | Max. |
| C_{IN} | Input Capacitance | 5.0 | | | 5 | 10 | | 10 | | 10 | pF |
| C_{PD} | Power Dissipation Capacitance (note 1) | 5.0 | | | 34 | | | | | | pF |

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/2$ (per FLIP/FLOP)

Figure 4: Test Circuit



$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5: Waveform - Minimum Pulse Width (Clear) And Removal Time (Clear To Clock) ($f=1\text{MHz}$; 50% duty cycle)

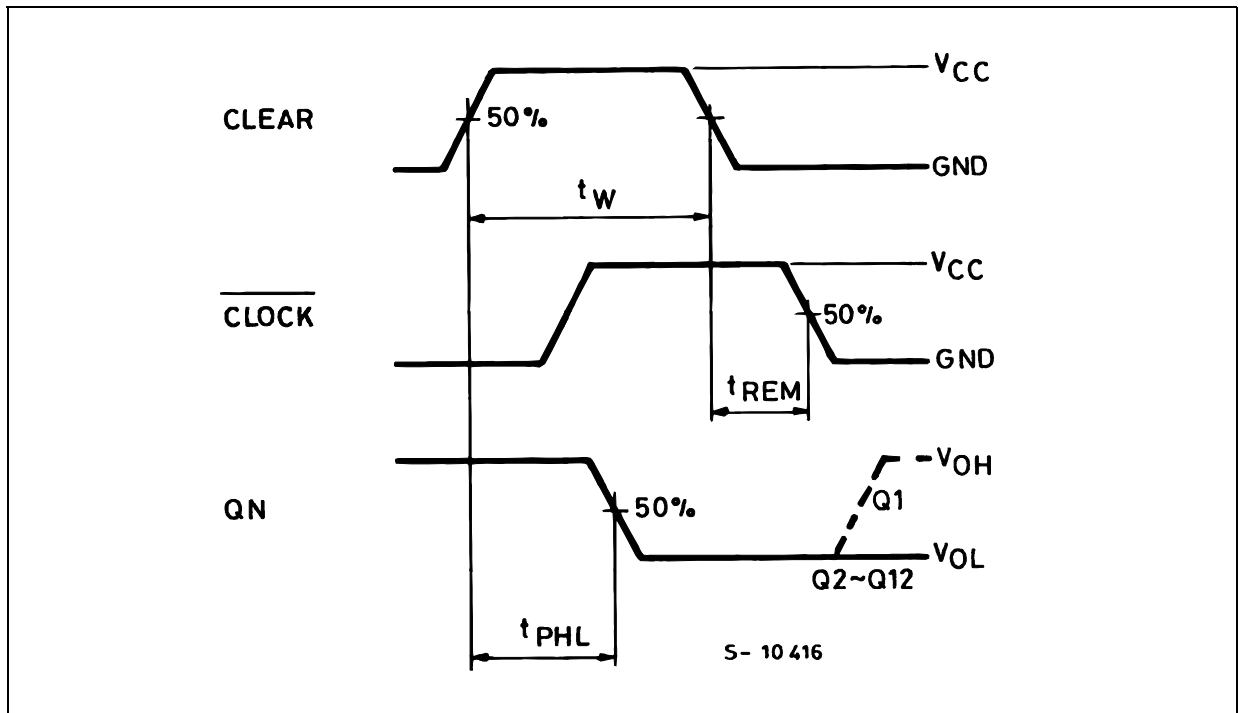
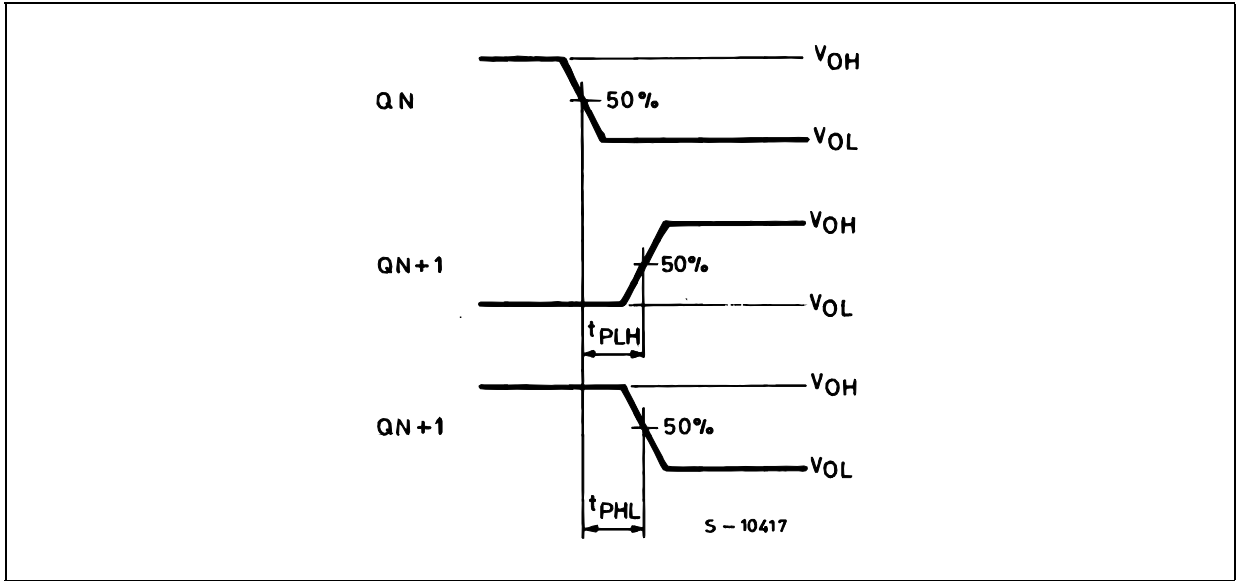
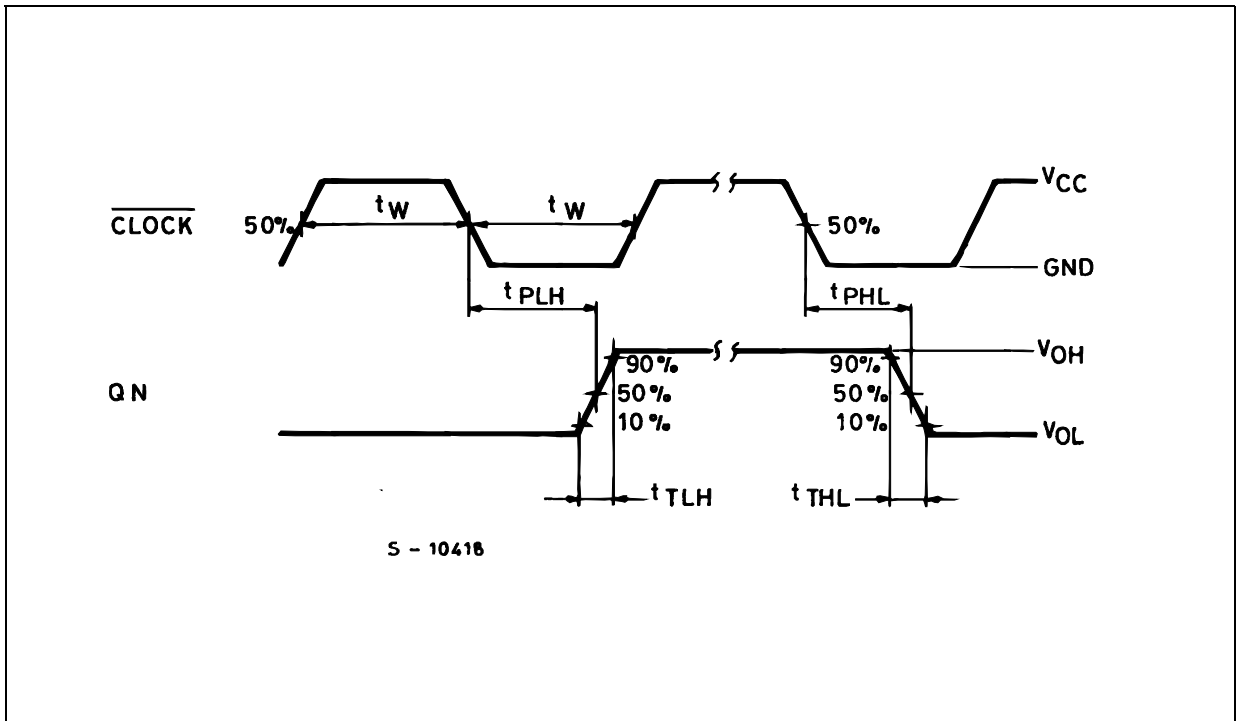
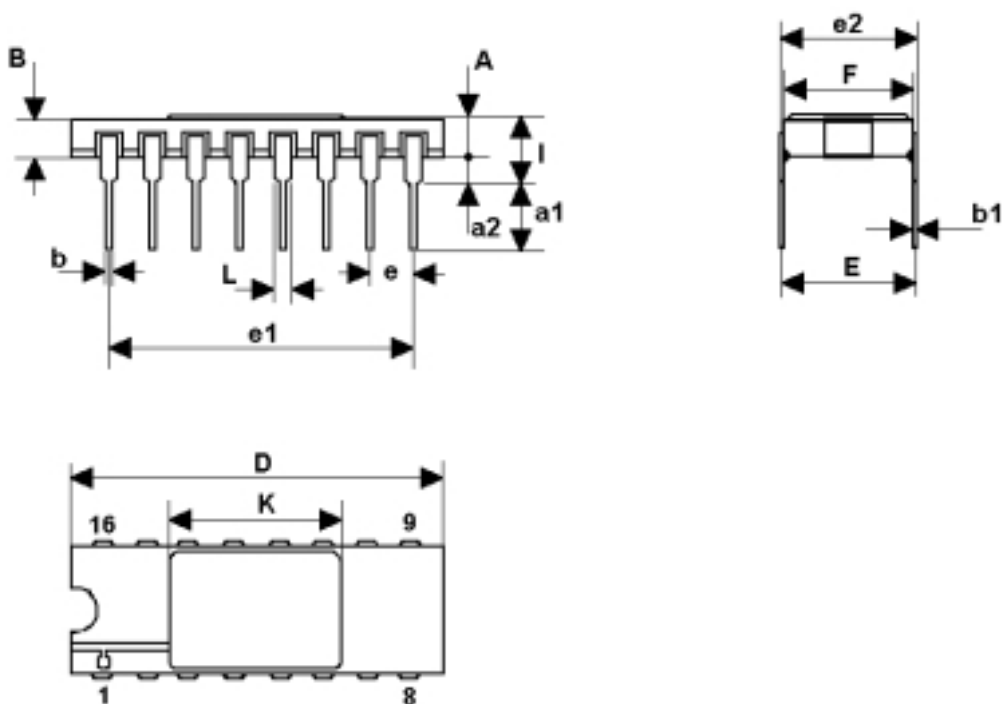


Figure 6: Waveform - Propagation Delay Time ($f=1\text{MHz}$; 50% duty cycle)Figure 7: Waveform - Propagation Delay Time, Minimum Pulse Width (Clock) ($f=1\text{MHz}$; 50% duty cycle)

DILC-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-------|-------|-------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 2.1 | | 2.71 | 0.083 | | 0.107 |
| a1 | 3.00 | | 3.70 | 0.118 | | 0.146 |
| a2 | 0.63 | 0.88 | 1.14 | 0.025 | 0.035 | 0.045 |
| B | 1.82 | | 2.39 | 0.072 | | 0.094 |
| b | 0.40 | 0.45 | 0.50 | 0.016 | 0.018 | 0.020 |
| b1 | 0.20 | 0.254 | 0.30 | 0.008 | 0.010 | 0.012 |
| D | 20.06 | 20.32 | 20.58 | 0.790 | 0.800 | 0.810 |
| e | 7.36 | 7.62 | 7.87 | 0.290 | 0.300 | 0.310 |
| e1 | | 2.54 | | | 0.100 | |
| e2 | 17.65 | 17.78 | 17.90 | 0.695 | 0.700 | 0.705 |
| e3 | 7.62 | 7.87 | 8.12 | 0.300 | 0.310 | 0.320 |
| F | 7.29 | 7.49 | 7.70 | 0.287 | 0.295 | 0.303 |
| I | | | 3.83 | | | 0.151 |
| K | 10.90 | | 12.1 | 0.429 | | 0.476 |
| L | 1.14 | | 1.5 | 0.045 | | 0.059 |



0056437F

FPC-16 MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|------|-------|-------|-------|-------|-------|-------|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 6.75 | 6.91 | 7.06 | 0.266 | 0.272 | 0.278 |
| B | 9.76 | 9.94 | 10.14 | 0.384 | 0.392 | 0.399 |
| C | 1.49 | | 1.95 | 0.059 | | 0.077 |
| D | 0.102 | 0.127 | 0.152 | 0.004 | 0.005 | 0.006 |
| E | 8.76 | 8.89 | 9.01 | 0.345 | 0.350 | 0.355 |
| F | | 1.27 | | | 0.050 | |
| G | 0.38 | 0.43 | 0.48 | 0.015 | 0.017 | 0.019 |
| H | 6.0 | | | 0.237 | | |
| L | 18.75 | | 22.0 | 0.738 | | 0.867 |
| M | 0.33 | 0.38 | 0.43 | 0.013 | 0.015 | 0.017 |
| N | | 4.31 | | | 0.170 | |

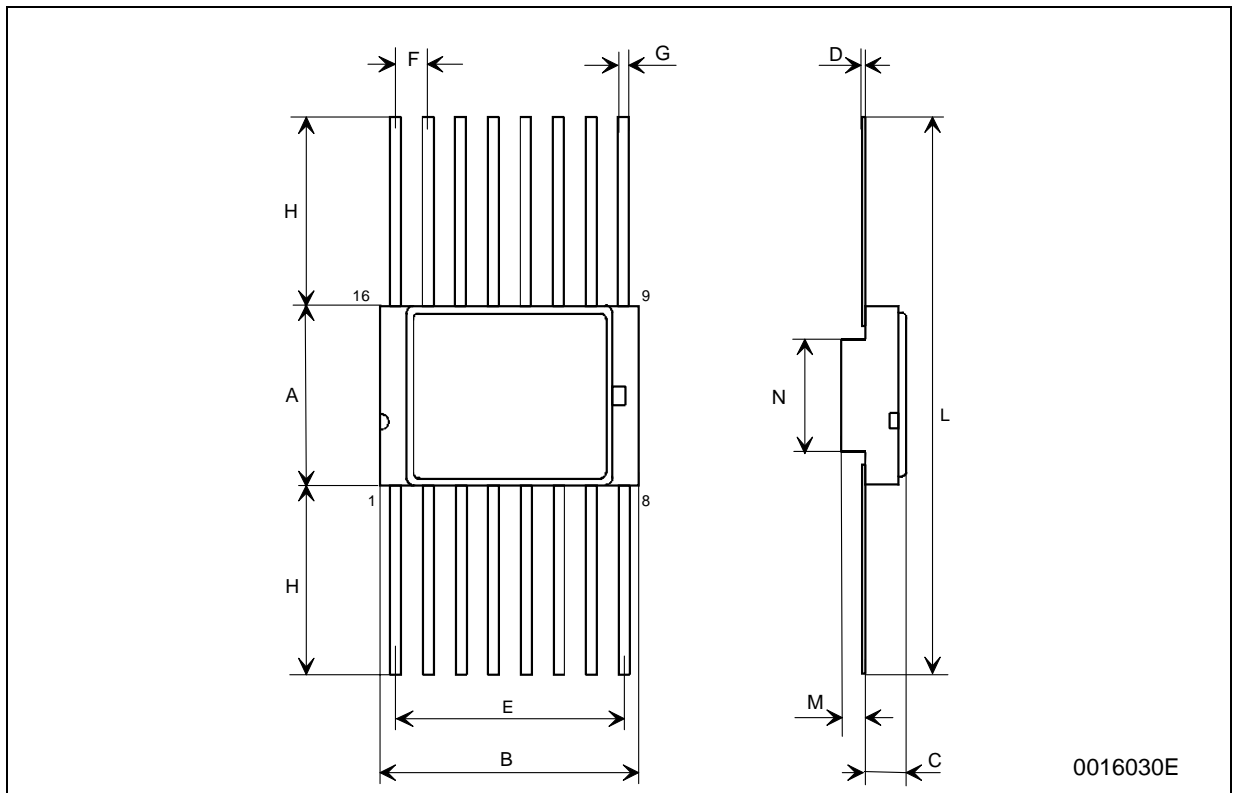


Table 8: Revision History

| Date | Revision | Description of Changes |
|-------------|-----------------|-------------------------------|
| 10-May-2004 | 1 | First Release |

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