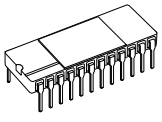
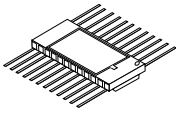
M54HC4514

RAD-HARD 4 TO 16 LINE DECODER/LATCH

- HIGH SPEED:
  t_{PD}= 20 ns (TYP.) at V_{CC} = 6V
- LOW POWER DISSIPATION:
  I_{CC} = 4μA(MAX.) at T_A=25°C
- HIGH NOISE IMMUNITY:
  V_{NIH} = V_{NIL} = 28% V_{CC} (MIN.)
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}|$ = I_{OL} = 4mA (MIN)
- BALANCED PROPAGATION DELAYS:
  $t_{PLH} \cong t_{PHL}$
- WIDE OPERATING VOLTAGE RANGE:
  V_{CC} (OPR) = 2V to 6V
- PIN AND FUNCTION COMPATIBLE WITH 54 SERIES 4514
- SPACE GRADE-1: ESA SCC QUALIFIED
- 50 krad QUALIFIED, 100 krad AVAILABLE ON REQUEST
- NO SEL UNDER HIGH LET HEAVY IONS IRRADIATION
- DEVICE FULLY COMPLIANT WITH SCC-9205-019



DILC-24



FPC-24

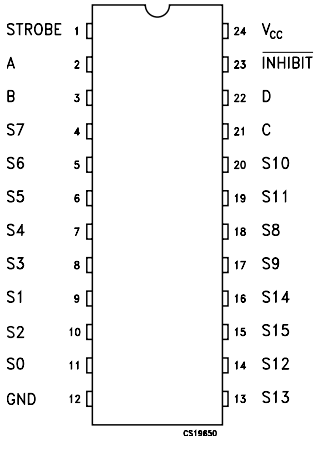
ORDER CODES

PACKAGE	FM	EM
DILC	M54HC4514D	M54HC4514D1
FPC	M54HC4514K	M54HC4514K1

DESCRIPTION

The M54HC4514 is an high speed CMOS 4 LINE TO 16 LINE SEGMENT DECODER WITH LATCHED INPUTS fabricated with silicon gate C^2MOS technology.
A binary code stored in the four input latches (A to D) provides a high level at the selected one of sixteen outputs excluding the other fifteen outputs, when the inhibit input ($\overline{INHIBIT}$) is held low. When the inhibit input ($\overline{INHIBIT}$) is held high, all outputs are kept low level, while the latch function is available. The data applied to the data inputs are transferred to the Q outputs of latches when the strobe input is held high. When the strobe input is taken low, the information data applied to the data input at a time is retained at the output of the latches.
All inputs are equipped with protection circuits against static discharge and transient excess voltage.

PIN CONNECTION



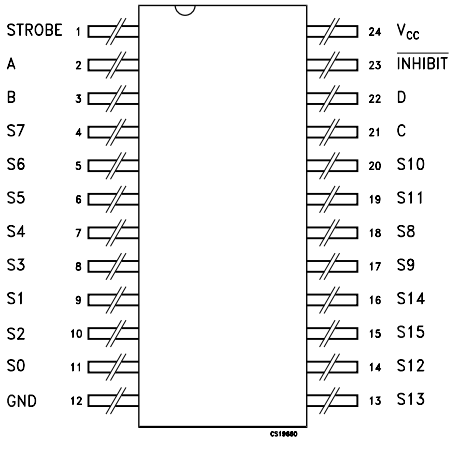


Figure 1: IEC Logic Symbols

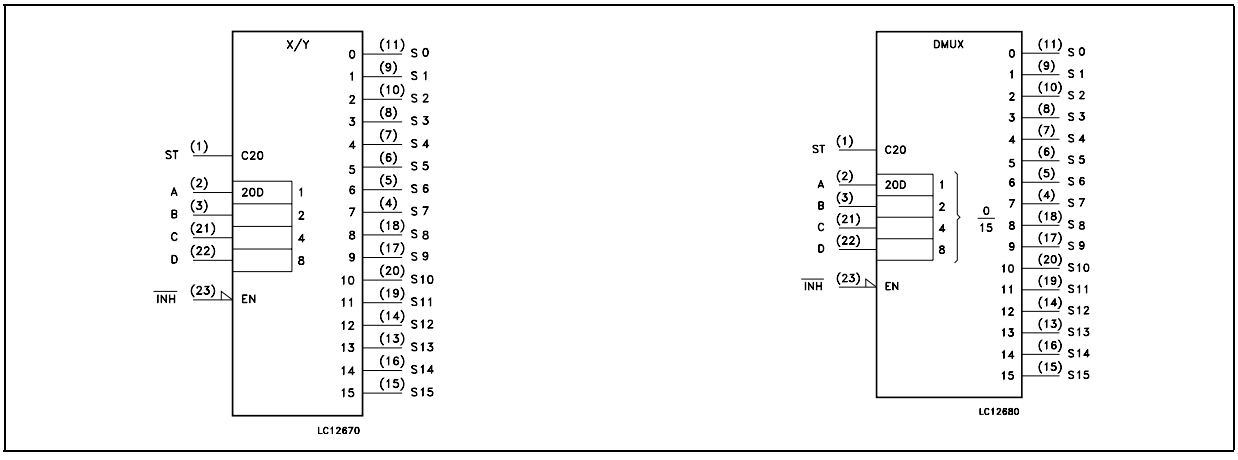


Figure 2: Input And Output Equivalent Circuit

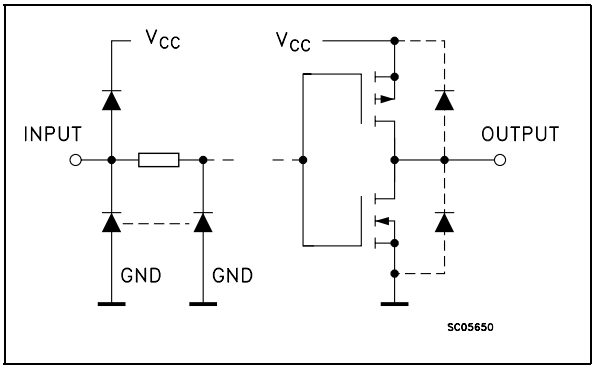


Table 1: Pin Description

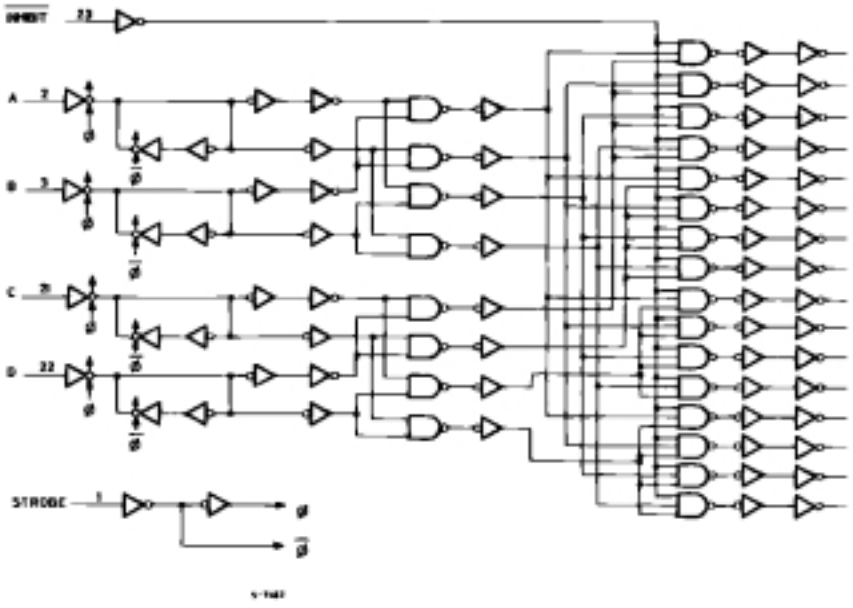
PIN N°	SYMBOL	NAME AND FUNCTION
1	STROBE	Strobe Input
2, 3, 21, 22	A to D	Address Inputs
11, 9, 10, 8, 7, 6, 5, 4, 18, 17, 20, 19, 14, 13, 16, 15	S0 to S15	Multiplexer Outputs (Active HIGH)
23	$\overline{\text{INHIBIT}}$	Enable Input
12	GND	Ground (0V)
24	V_{CC}	Positive Supply Voltage

Table 2: Truth Table

INPUTS					STROBE	SELECT OUTPUT
$\overline{\text{INHIBIT}}$	A	B	C	D		
L	L	L	L	L	STROBE = "H" Refer to truth table STROBE = "L" Data at the negative going transition of strobe shall be provided on the each output while strobe is held low.	S0
L	H	L	L	L		S1
L	L	H	L	L		S2
L	H	H	L	L		S3
L	L	L	H	L		S4
L	H	L	H	L		S5
L	L	H	H	L		S6
L	H	H	H	L		S7
L	L	L	L	H		S8
L	H	L	L	H		S9
L	L	H	L	H		S10
L	H	H	L	H		S11
L	L	L	H	H		S12
L	H	L	H	H		S13
L	L	H	H	H		S14
L	H	H	H	H		S15
H	X	X	X	X		ALL OUTPUTS "L"

X : Don't Care

Figure 3: Logic Diagram



This logic diagram has not be used to estimate propagation delays

Table 3: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to V_{CC} + 0.5	V
V_O	DC Output Voltage	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 25	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 50	mA
P_D	Power Dissipation	300	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	265	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

Table 4: Recommended Operating Conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage		2 to 6	V
V_I	Input Voltage		0 to V_{CC}	V
V_O	Output Voltage		0 to V_{CC}	V
T_{op}	Operating Temperature		-55 to 125	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 2.0V	0 to 1000	ns
		V_{CC} = 4.5V	0 to 500	ns
		V_{CC} = 6.0V	0 to 400	ns

Table 5: DC Specifications

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	2.0		1.5			1.5		1.5		V
		4.5		3.15			3.15		3.15		
		6.0		4.2			4.2		4.2		
V_{IL}	Low Level Input Voltage	2.0				0.5		0.5		0.5	V
		4.5				1.35		1.35		1.35	
		6.0				1.8		1.8		1.8	
V_{OH}	High Level Output Voltage	2.0	I_O=-20 µA	1.9	2.0		1.9		1.9		V
		4.5	I_O=-20 µA	4.4	4.5		4.4		4.4		
		6.0	I_O=-20 µA	5.9	6.0		5.9		5.9		
		4.5	I_O=-4.0 mA	4.18	4.31		4.13		4.10		
		6.0	I_O=-5.2 mA	5.68	5.8		5.63		5.60		
V_{OL}	Low Level Output Voltage	2.0	I_O=20 µA		0.0	0.1		0.1		0.1	V
		4.5	I_O=20 µA		0.0	0.1		0.1		0.1	
		6.0	I_O=20 µA		0.0	0.1		0.1		0.1	
		4.5	I_O=4.0 mA		0.17	0.26		0.37		0.40	
		6.0	I_O=5.2 mA		0.18	0.26		0.37		0.40	
I_I	Input Leakage Current	6.0	V_I = V_{CC} or GND			± 0.1		± 1		± 1	µA
I_{CC}	Quiescent Supply Current	6.0	V_I = V_{CC} or GND			4		40		80	µA

Table 6: AC Electrical Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6ns)

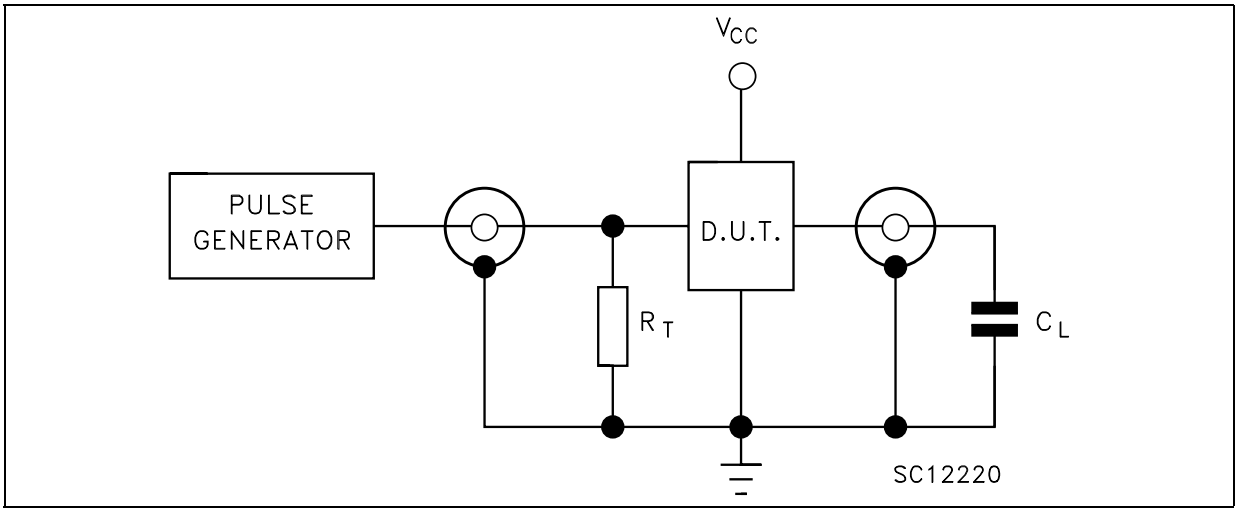
Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
t_{TLH} t_{THL}	Output Transition Time	2.0			30	75		95		110	ns
		4.5			8	15		19		25	
		6.0			7	13		16		23	
t_{PLH} t_{PHL}	Propagation Delay Time (DATA - Sn)	2.0			65	175		220		230	ns
		4.5			22	35		44		56	
		6.0			19	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (STROBE- Sn.)	2.0			75	175		220		260	ns
		4.5			24	35		44		56	
		6.0			20	30		37		45	
t_{PLH} t_{PHL}	Propagation Delay Time (INHIBIT - Sn)	2.0			60	175		220		260	ns
		4.5			20	35		44		56	
		6.0			17	30		37		45	
$t_{W(L)}$	Minimum Pulse Width (STROBE)	2.0			14	75		95		110	ns
		4.5			6	15		19		26	
		6.0			6	13		16		23	
t_s	Minimum Set Up Time (DATA)	2.0			10	50		65		80	ns
		4.5			2	10		13		20	
		6.0			1	9		11		17	
t_h	Minimum Hold Time (DATA)	2.0				5		5		5	ns
		4.5				5		5		5	
		6.0				5		5		5	

Table 7: Capacitive Characteristics

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
C_{IN}	Input Capacitance				5	10		10		10	pF
C_{PD}	Power Dissipation Capacitance (note 1)				61						pF

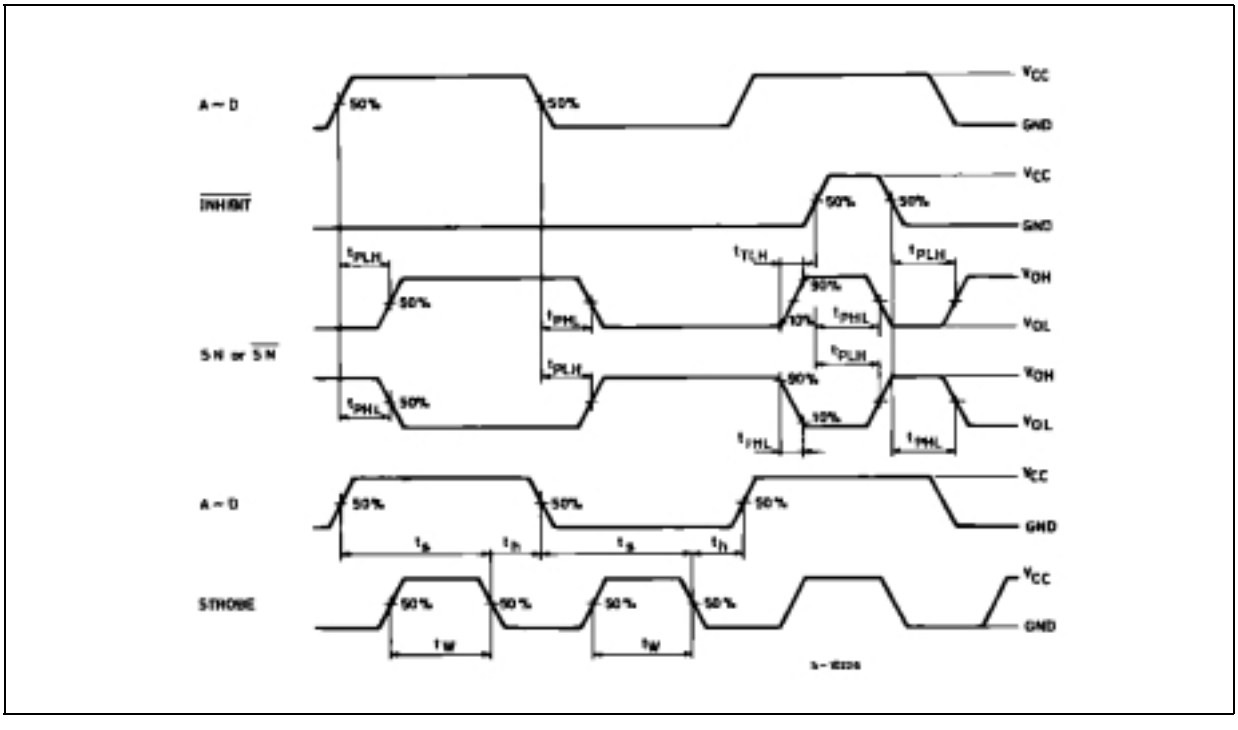
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

Figure 4: Test Circuit



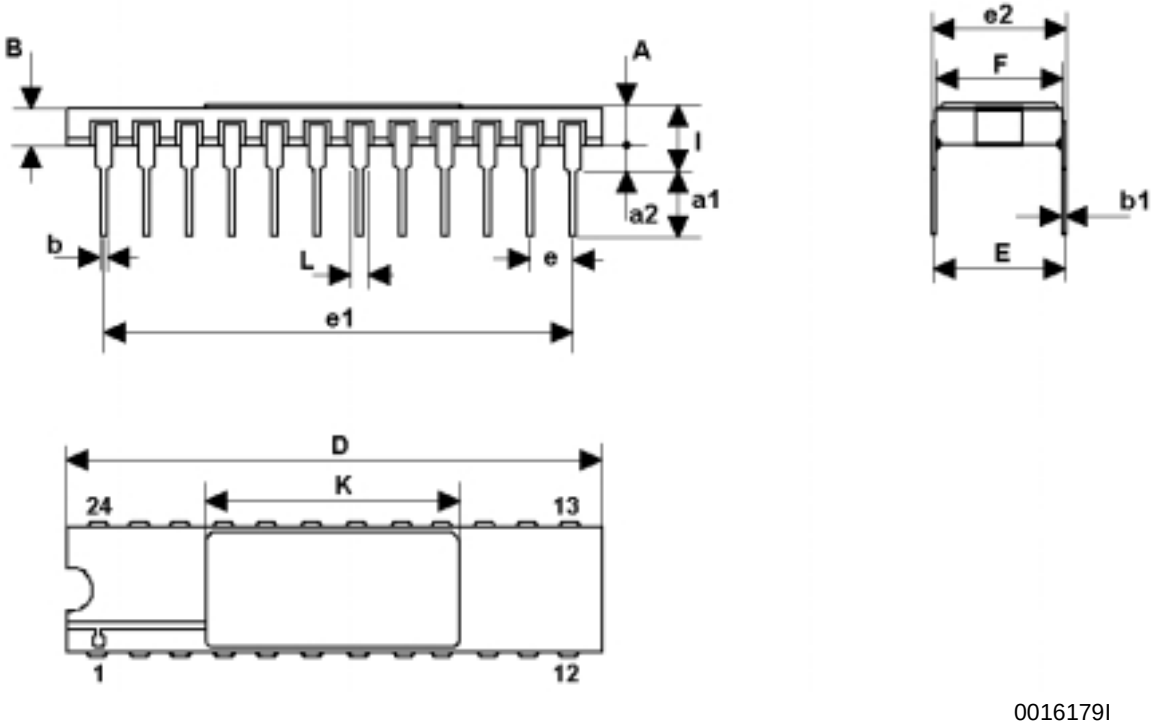
C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5: Switching Characteristics Test Waveform (f=1MHz; 50% duty cycle)



DILC-24 (0.3”) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	2.1		2.72	0.083		0.107
a1	2.7	3.0	3.3	0.106	0.118	0.130
a2	1.016	1.27	1.524	0.40	0.50	0.60
B	1.93	2.16	2.39	0.076	0.085	0.094
b	0.40	0.45	0.50	0.016	0.018	0.020
b1	0.20	0.254	0.30	0.008	0.010	0.012
D	30.17	30.48	30.78	1.188	1.200	1.212
E	7.36	7.62	7.87	0.290	0.300	0.310
e		2.54			0.100	
e1	27.81		28.07	1.095		1.105
e2	7.62	7.87	8.12	0.300	0.310	0.320
F	7.24		7.75	0.285		0.305
I			4.24			0.167
K	14.22		14.48	0.560		0.570
L	1.22	1.27	1.32	0.048	0.050	0.052



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FPC-24 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	10.70	11.0	11.30	0.421	0.433	0.445
B	15.3	15.49	15.70	0.602	0.610	0.618
C	1.45		1.9	0.057		0.075
D	0.23	0.254	0.3	0.009	0.010	0.012
E	13.84	13.97	14.10	0.545	0.550	0.555
F	1.22	1.27	1.32	0.048	0.050	0.052
G	0.45	0.508	0.55	0.018	0.020	0.022
H	7.25		8.25	0.285		0.325
L	25.0		28.0	0.984		1.102
M	0.45	0.508	0.55	0.018	0.020	0.022
N		7.01			0.276	

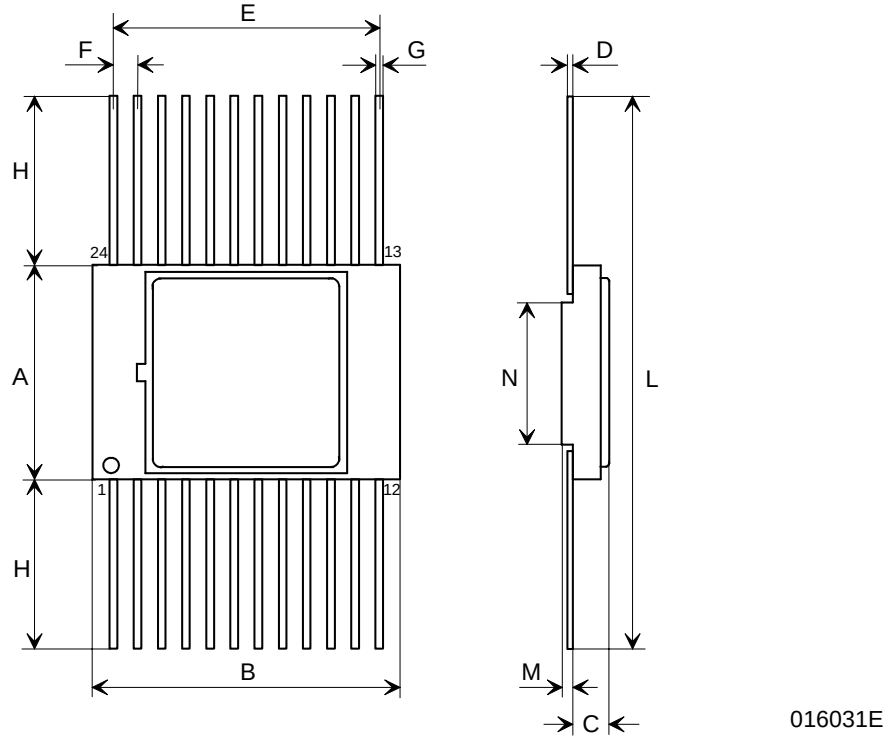

Table 8: Revision History

Date	Revision	Description of Changes
14-May-2004	1	First Release