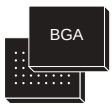
M58LT128GST
M58LT128GSB

128Mbit (8Mb x16, Multiple Bank, Multi-Level, Burst) 1.8V Supply Secure Flash Memories

PRELIMINARY DATA

Features Summary

- SUPPLY VOLTAGE
  - V_{DD} = 1.7 to 2.0V for program, erase and read
  - V_{DDQ} = 2.7 to 3.6V for I/O Buffers
  - V_{PP} = 9V for fast program
- SYNCHRONOUS / ASYNCHRONOUS READ
  - Random Access: 110ns
  - Asynchronous Page Read: 25ns.
  - Synchronous Burst Read: 52MHz
- SYNCHRONOUS BURST READ SUSPEND
- PROGRAMMING TIME
  - 10µs typical Word program time using Buffer Enhanced Factory Program command
- MEMORY ORGANIZATION
  - Multiple Bank Memory Array: 8 Mbit Banks
  - Parameter Blocks (Top or Bottom location)
- DUAL OPERATIONS
  - program/erase in one Bank while read in others
  - No delay between read and write operations
- HARDWARE PROTECTION
  - All Blocks Write Protected when $V_{PP} \leq V_{PPLK}$
- SECURITY
  - Software Security Features
  - 64-bit Unique Device Identifier
  - 2112 bits of User-Programmable OTP memory
- COMMON FLASH INTERFACE (CFI)



TBGA64 (ZA)
10 x 13mm

- 100,000 PROGRAM/ERASE CYCLES per BLOCK
- ELECTRONIC SIGNATURE
  - Manufacturer Code: 20h
  - Device Code:
    M58LT128GST: 88C6h
    M58LT128GSB: 88C7h
- ECOPACK® PACKAGE AVAILABLE

Contents

List of tables

List of figures

1 Summary description

The M58LT128GST and M58LT128GSB are 128 Mbit (8 Mbit x16) non-volatile Secure Flash memories.

The devices may be erased electrically at block level and programmed in-system on a Word-by-Word basis using a 1.7 to 2.0V V_{DD} supply for the circuitry and a 2.7 to 3.6V V_{DDQ} supply for the Input/Output pins. An optional 9V V_{PP} power supply is provided to speed up factory programming.

The devices feature an asymmetrical block architecture and are based on a multi-level cell technology. The memory array is organized as 131 blocks, and is divided into 8 Mbit banks. There are 15 banks each containing 8 main blocks of 64 KWords, and one parameter bank containing 4 parameter blocks of 16 KWords and 7 main blocks of 64 KWords.

The Multiple Bank Architecture allows Dual Operations, while programming or erasing in one bank, read operations are possible in other banks. Only one bank at a time is allowed to be in program or erase mode. It is possible to perform burst reads that cross bank boundaries. The bank architecture is summarized in *Table 2*, and the memory maps are shown in *Figure 3*. The Parameter Blocks are located at the top of the memory address space for the M58LT128GST, and at the bottom for the M58LT128GSB.

Each block can be erased separately. Erase can be suspended, in order to perform a program or read operation in any other block, and then resumed. Program can be suspended to read data at any memory location except for the one being programmed, and then resumed. Each block can be programmed and erased over 100,000 cycles using the supply voltage V_{DD}. There is a Buffer Enhanced Factory programming command available to speed up programming.

Program and erase commands are written to the Command Interface of the memory. An internal Program/Erase Controller takes care of the timings necessary for program and erase operations. The end of a program or erase operation can be detected and any error conditions identified in the Status Register. The command set required to control the memory is consistent with JEDEC standards.

The device supports Synchronous Burst Read and Asynchronous Read and Page Read from all blocks of the memory array; at power-up the device is configured for Asynchronous Read. In Synchronous Burst Read mode, data is output on each clock cycle at frequencies of up to 52MHz. The Synchronous Burst Read operation can be suspended and resumed.

The device features an Automatic Standby mode. When the bus is inactive during Asynchronous Read operations, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value and the outputs are still driven.

The M58LT128GST and M58LT128GSB are equipped with several features to increase data protection:

- Hardware Protection: all blocks are protected from program and erase operations when the $V_{PP} \leq V_{PPLK}$.
- A full set of Software Security Features described in a dedicated Application Note. Please contact STMicroelectronics for further details.
- 64-bit Unique Device Identifier
- 2112 bits of User-Programmable OTP memory

The device includes 17 Protection Registers and 2 Protection Register locks, one for the first Protection Register and the other for the 16 One-Time-Programmable (OTP) Protection Registers of 128 bits each. The first Protection Register is divided into two segments: a 64 bit segment containing a unique device number written by ST, and a 64 bit segment One-Time-Programmable (OTP) by the user. The user programmable segment can be permanently protected. *Figure 4* shows the Protection Register Memory Map.

The devices are offered in TBGA64 10 x 13mm, 1mm pitch.

In order to meet environmental requirements, ST offers the M58LT128GST and M58LT128GSB in ECOPACK® package. ECOPACK package is Lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

The memories are supplied with all the bits erased (set to '1').

Figure 1. Logic Diagram

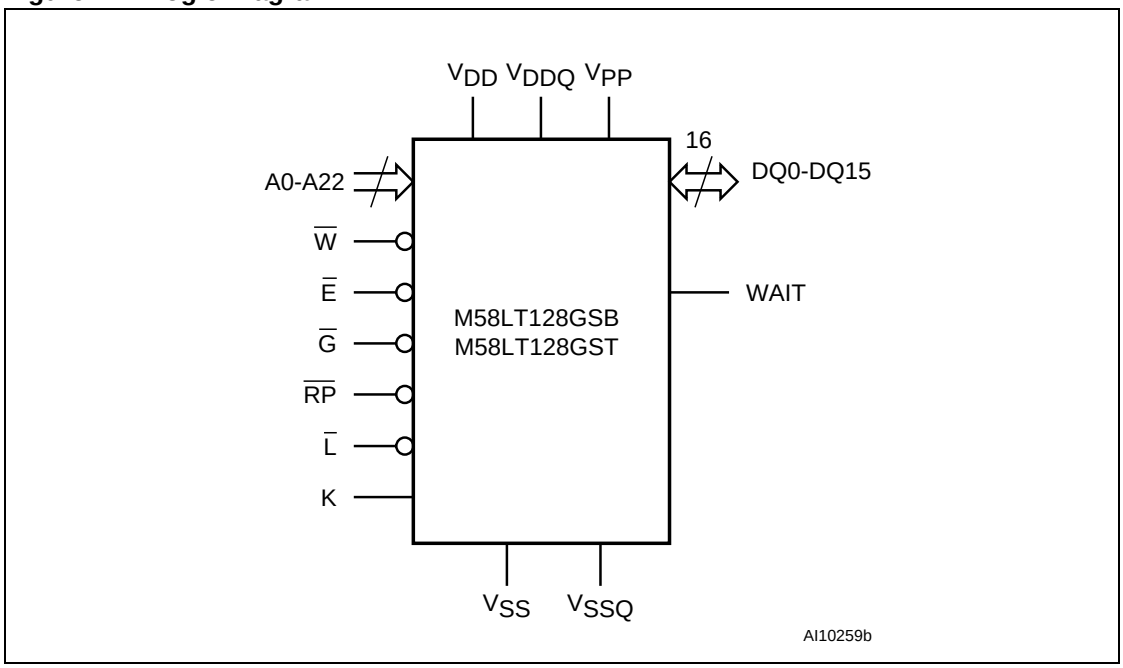


Table 1. Signal Names

A0-A22	Address Inputs
DQ0-DQ15	Data Input/Outputs, Command Inputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{RP}$	Reset
K	Clock
$\overline{L}$	Latch Enable
WAIT	Wait
V_{DD}	Supply Voltage
V_{DDQ}	Supply Voltage for Input/Output Buffers
V_{PP}	Optional Supply Voltage for Fast Program & Erase and Write Protect
V_{SS}	Ground
V_{SSQ}	Ground Input/Output Supply
NC	Not Connected Internally

Figure 2. TBGA64 Connections (Top view through package)

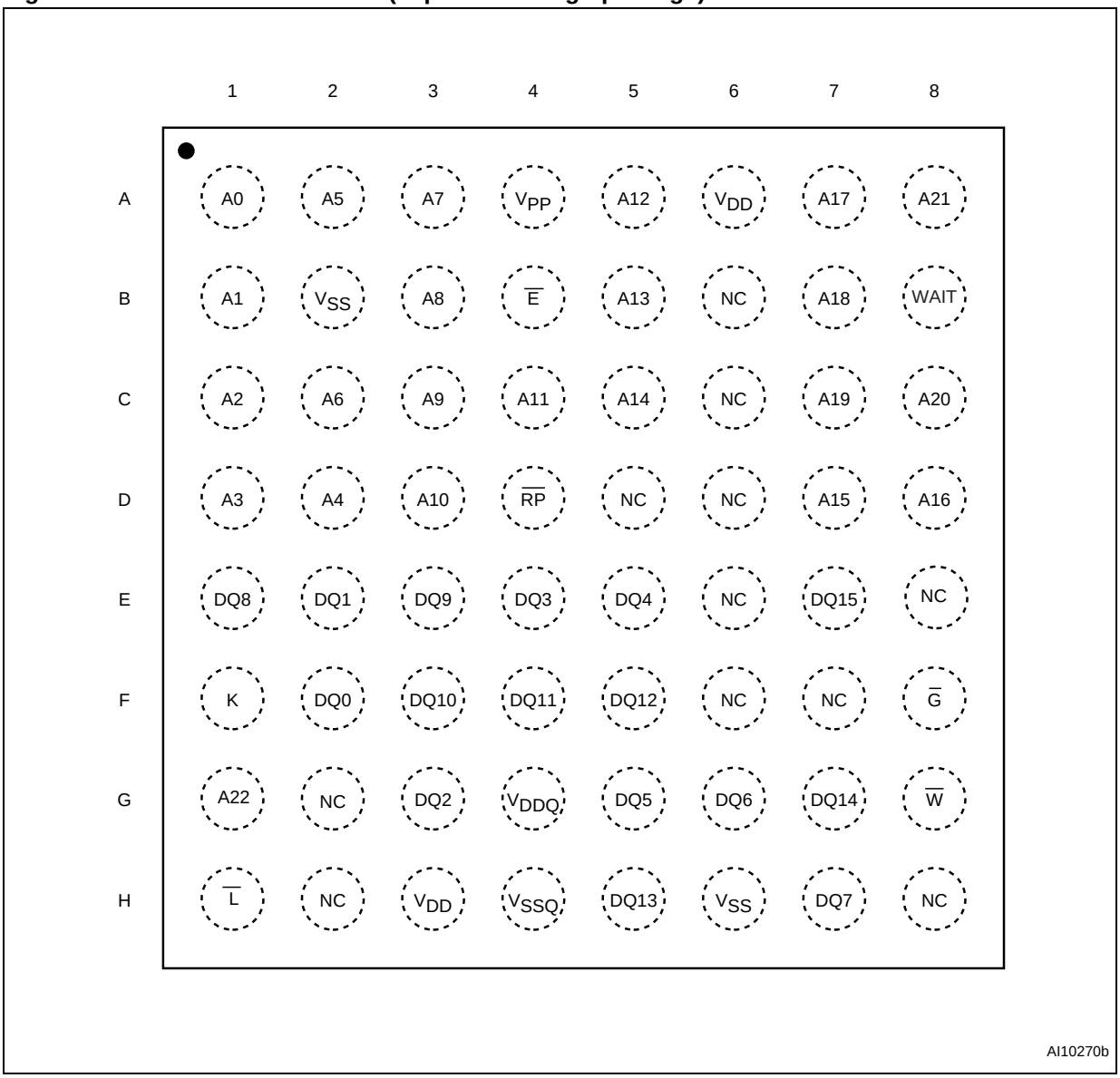
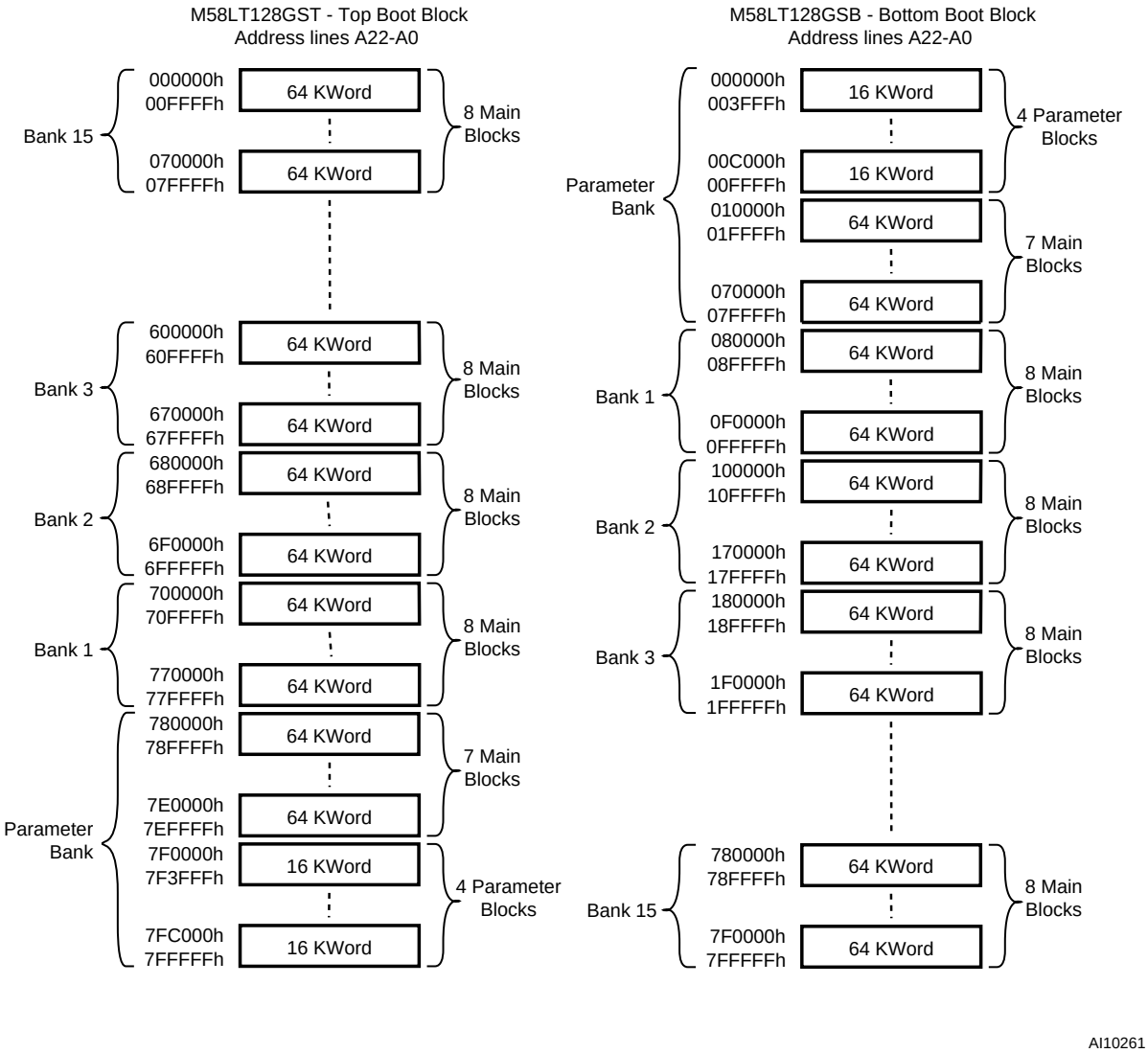


Table 2. Bank Architecture

Number	Bank Size	Parameter Blocks	Main Blocks
Parameter Bank	8 Mbits	4 blocks of 16 KWords	7 blocks of 64 KWords
Bank 1	8 Mbits	-	8 blocks of 64 KWords
Bank 2	8 Mbits	-	8 blocks of 64 KWords
Bank 3	8 Mbits	-	8 blocks of 64 KWords
⋮	⋮	⋮	⋮
Bank 14	8 Mbits	-	8 blocks of 64 KWords
Bank 15	8 Mbits	-	8 blocks of 64 KWords

Figure 3. Memory Map



2 Signal descriptions

See *Figure 1: Logic Diagram* and *Table 1: Signal Names*, for a brief overview of the signals connected to this device.

2.1 Address Inputs (A0-A22)

The Address Inputs select the cells in the memory array to access during Bus Read operations. During Bus Write operations they control the commands sent to the Command Interface of the Program/Erase Controller.

2.2 Data Input/Output (DQ0-DQ15)

The Data I/O output the data stored at the selected address during a Bus Read operation or input a command or the data to be programmed during a Bus Write operation.

2.3 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is at $V_{IL}$and Reset is at V_{IH} the device is in active mode. When Chip Enable is at V_{IH} the memory is deselected, the outputs are high impedance and the power consumption is reduced to the stand-by level.

2.4 Output Enable ($\overline{G}$)

The Output Enable input controls data outputs during the Bus Read operation of the memory.

2.5 Write Enable ($\overline{W}$)

The Write Enable input controls the Bus Write operation of the memory's Command Interface. The data and address inputs are latched on the rising edge of Chip Enable or Write Enable whichever occurs first.

2.6 Reset ($\overline{RP}$)

The Reset input provides a hardware reset of the memory. When Reset is at V_{IL}, the memory is in reset mode: the outputs are high impedance and the current consumption is reduced to the Reset Supply Current I_{DD2}. Refer to *Table 20: DC Characteristics - Currents*, for the value of I_{DD2}. After Reset all blocks are in the Protected state and the Configuration Register is reset. When Reset is at V_{IH}, the device is in normal operation. Exiting reset mode the device enters asynchronous read mode, but a negative transition of Chip Enable or Latch Enable is required to ensure valid data outputs.

The Reset pin can be interfaced with 3V logic without any additional circuitry. It can be tied to V_{RPH} (refer to *Table 21: DC Characteristics - Voltages*).

2.7 Latch Enable ($\overline{L}$)

Latch Enable latches the A0-A22 address bits on its rising edge. The address latch is transparent when Latch Enable is at V_{IL} and it is inhibited when Latch Enable is at V_{IH}.

2.8 Clock (K)

The clock input synchronizes the memory to the microcontroller during synchronous read operations; the address is latched on a Clock edge (rising or falling, according to the configuration settings) when Latch Enable is at V_{IL}. Clock is ignored during asynchronous read and in write operations.

2.9 Wait (WAIT)

Wait is an output signal used during synchronous read to indicate whether the data on the output bus are valid. This output is high impedance when Chip Enable is at V_{IH} or Reset is at V_{IL}. It can be configured to be active during the wait cycle or one clock cycle in advance. The WAIT signal is forced deasserted when Output Enable is at V_{IH}.

2.10 V_{DD} Supply Voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (Read, Program and Erase).

2.10.1 V_{DDQ} Supply Voltage

V_{DDQ} provides the power supply to the I/O pins and enables all Outputs to be powered independently from V_{DD}. V_{DDQ} can be tied to V_{DD} or can use a separate supply.

2.11 V_{PP} Program Supply Voltage

The V_{PP} pin is both a power supply and a write protect pin. The functions are selected by the voltage range applied to the pin.

When V_{PP} is lower than V_{PPLK}, it is seen as a write protect pin protecting the whole memory array. Program and erase operations on all blocks are ignored while V_{PP} is Low.

When V_{PP} is Higher than V_{PP1}, the memory reverts to the previous protection state of the memory array. Program and erase operations can now modify the data in any block (refer to *Table 21: DC Characteristics - Voltages* for V_{PPLK} and V_{PP1} values). V_{PP} is only sampled at the beginning of a program or erase; a change in its value after the operation has started does not have any effect and program or erase operations continue.

If V_{PP} is in the range of V_{PPH} it acts as a power supply pin. In this condition V_{PP} must be stable until the Program/Erase algorithm is completed.

The V_{PP} pin must not be left floating or unconnected or the device may become unreliable. A 0.1µF capacitor should be connected between the V_{PP} pin and the V_{SS} Ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during Unlock Bypass Program, I_{PP}.

2.12 V_{SS} Ground

V_{SS} ground is the reference for the core supply. It must be connected to the system ground.

2.13 V_{SSQ} Ground

V_{SSQ} ground is the reference for the input/output circuitry driven by V_{DDQ}. V_{SSQ} must be connected to V_{SS}

Note: Each device in a system should have V_{DD}, V_{DDQ} and V_{PP} decoupled with a 0.1µF ceramic capacitor close to the pin (high frequency, inherently low inductance capacitors should be as close as possible to the package). See *Figure 8: AC Measurement Load Circuit*. The PCB track widths should be sufficient to carry the required V_{PP} program and erase currents.

3 Bus operations

There are six standard bus operations that control the device. These are Bus Read, Bus Write, Address Latch, Output Disable, Standby and Reset. See *Table 3: Bus Operations*, for a summary.

Typically glitches of less than 5ns on Chip Enable or Write Enable are ignored by the memory and do not affect Bus Write operations.

3.1 Bus Read

Bus Read operations are used to output the contents of the Memory Array, the Electronic Signature, the Status Register and the Common Flash Interface. Both Chip Enable and Output Enable must be at V_{IL} in order to perform a read operation. The Chip Enable input should be used to enable the device. Output Enable should be used to gate data onto the output. The data read depends on the previous command written to the memory (see Command Interface section). See *Figure 9*, *Figure 11* and *Figure 12* Read AC Waveforms, and *Table 22* and *Table 23* Read AC Characteristics, for details of when the output becomes valid.

3.2 Bus Write

Bus Write operations write Commands to the memory or latch Input Data to be programmed. A bus write operation is initiated when Chip Enable and Write Enable are at V_{IL} with Output Enable at V_{IH}. Commands, Input Data and Addresses are latched on the rising edge of Write Enable or Chip Enable, whichever occurs first. The addresses can also be latched prior to the write operation by toggling Latch Enable. In this case the Latch Enable should be tied to V_{IH} during the bus write operation. See *Figure 15* and *Figure 16*, Write AC Waveforms, and *Table 24* and *Table 25*, Write AC Characteristics, for details of the timing requirements.

3.3 Address Latch

Address latch operations input valid addresses. Both Chip enable and Latch Enable must be at V_{IL} during address latch operations. The addresses are latched on the rising edge of Latch Enable.

3.4 Output Disable

The outputs are high impedance when the Output Enable is at V_{IH}.

3.5 Standby

Standby disables most of the internal circuitry allowing a substantial reduction of the current consumption. The memory is in standby when Chip Enable and Reset are at V_{IH}. The power consumption is reduced to the standby level I_{DD3} and the outputs are set to high impedance, independently from the Output Enable or Write Enable inputs. If Chip Enable switches to V_{IH} during a program or erase operation, the device enters Standby mode when finished.

3.6 Reset

During Reset mode the memory is deselected and the outputs are high impedance. The memory is in Reset mode when Reset is at V_{IL}. The power consumption is reduced to the Reset level, independently from the Chip Enable, Output Enable or Write Enable inputs. If Reset is pulled to V_{SS} during a Program or Erase, this operation is aborted and the memory content is no longer valid.

Table 3. Bus Operations

Operation(1)	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{L}$	$\overline{RP}$	WAIT(2)	DQ15-DQ0
Bus Read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}		Data Output
Bus Write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_{IH}		Data Input
Address Latch	V_{IL}	V_{IH}	X	V_{IL}	V_{IH}		Address Input
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_{IH}		Hi-Z
Standby	V_{IH}	X	X	X	V_{IH}	Hi-Z	Hi-Z
Reset	X	X	X	X	V_{IL}	Hi-Z	Hi-Z

1. X = Don't care.
2. WAIT signal polarity is configured using the Set Configuration Register command.

4 Command Interface

All Bus Write operations to the memory are interpreted by the Command Interface. Commands consist of one or more sequential Bus Write operations. An internal Program/Erase Controller handles all timings and verifies the correct execution of the program and erase commands. The Program/Erase Controller provides a Status Register whose output may be read at any time to monitor the progress or the result of the operation.

The Command Interface is reset to read mode when power is first applied, when exiting from Reset or whenever V_{DD} is lower than V_{LKO}. Command sequences must be followed exactly. Any invalid combination of commands will be ignored.

Refer to *Table 4: Command Codes*, *Table 5: Standard Commands*, *Table 6: Factory Program Command*, and *Appendix D: Command Interface state tables*, for a summary of the Command Interface.

Note: The security features are described in a dedicated Application Note. Please contact STMicroelectronics for further details.

Table 4. Command Codes

Hex Code	Command
03h	Set Configuration Register Confirm
10h	Alternative Program Setup
20h	Block Erase Setup
40h	Program Setup
50h	Clear Status Register
70h	Read Status Register
80h	Buffer Enhanced Factory Program
90h	Read Electronic Signature
98h	Read CFI Query
B0h	Program/Erase Suspend
C0h	Program Register Program
D0h	Program/Erase Resume, Block Erase Confirm, or Buffer Program Confirm
E8h	Buffer Program
FFh	Read Array

4.1 Read Array command

The Read Array command returns the addressed bank to Read Array mode.

One Bus Write cycle is required to issue the Read Array command. Once a bank is in Read Array mode, subsequent read operations will output the data from the memory array.

A Read Array command can be issued to any banks while programming or erasing in another bank.

If the Read Array command is issued to a bank currently executing a program or erase operation, the bank will return to Read Array mode but the program or erase operation will continue, however the data output from the bank is not guaranteed until the program or erase operation has finished. The read modes of other banks are not affected.

4.2 Read Status Register command

The device contains a Status Register that is used to monitor program or erase operations.

The Read Status Register command is used to read the contents of the Status Register for the addressed bank.

One Bus Write cycle is required to issue the Read Status Register command. Once a bank is in Read Status Register mode, subsequent read operations will output the contents of the Status Register.

The Status Register data is latched on the falling edge of the Chip Enable or Output Enable signals. Either Chip Enable or Output Enable must be toggled to update the Status Register data

The Read Status Register command can be issued at any time, even during program or erase operations. The Read Status Register command will only change the read mode of the addressed bank. The read modes of other banks are not affected. Only Asynchronous Read and Single Synchronous Read operations should be used to read the Status Register. A Read Array command is required to return the bank to Read Array mode.

See *Table 9* for the description of the Status Register Bits.

4.3 Read Electronic Signature command

The Read Electronic Signature command is used to read the Manufacturer and Device Codes, the Protection Status of the addressed bank, the Configuration Register and the Protection Register.

One Bus Write cycle is required to issue the Read Electronic Signature command. Once a bank is in Read Electronic Signature mode, subsequent read operations in the same bank will output the Manufacturer Code, the Device Code, the Protection Status of the addressed bank, or the Configuration Register (see *Table 7*).

The Read Electronic Signature command can be issued at any time, even during program or erase operations, except during Protection Register Program operations. Dual operations between the Parameter bank and the Electronic Signature location are not allowed (see *Table 15: Dual Operation Limitations* for details).

If a Read Electronic Signature command is issued to a bank that is executing a program or erase operation the bank will go into Read Electronic Signature mode. Subsequent Bus Read

cycles will output the Electronic Signature data and the Program/Erase controller will continue to program or erase in the background.

The Read Electronic Signature command will only change the read mode of the addressed bank. The read modes of other banks are not affected. Only Asynchronous Read and Single Synchronous Read operations should be used to read the Electronic Signature. A Read Array command is required to return the bank to Read Array mode.

4.4 Read CFI Query command

The Read CFI Query command is used to read data from the Common Flash Interface (CFI).

One Bus Write cycle is required to issue the Read CFI Query command. Once a bank is in Read CFI Query mode, subsequent Bus Read operations in the same bank read from the Common Flash Interface.

The Read CFI Query command can be issued at any time, even during program or erase operations.

If a Read CFI Query command is issued to a bank that is executing a program or erase operation the bank will go into Read CFI Query mode. Subsequent Bus Read cycles will output the CFI data and the Program/Erase controller will continue to program or erase in the background.

The Read CFI Query command will only change the read mode of the addressed bank. The read modes of other banks are not affected. Only Asynchronous Read and Single Synchronous Read operations should be used to read from the CFI. A Read Array command is required to return the bank to Read Array mode. Dual operations between the Parameter Bank and the CFI memory space are not allowed (see *Table 15: Dual Operation Limitations* for details).

See *Appendix B: Common Flash Interface*, *Table 36*, *Table 37*, *Table 38*, *Table 39*, *Table 40*, *Table 42*, *Table 43*, *Table 44* and *Table 45* for details on the information contained in the Common Flash Interface memory area.

4.5 Clear Status Register command

The Clear Status Register command can be used to reset (set to ‘0’) all error bits (SR1, 3, 4 and 5) in the Status Register.

One Bus Write cycle is required to issue the Clear Status Register command. The Clear Status Register command does not affect the read mode of the bank.

The error bits in the Status Register do not automatically return to ‘0’ when a new command is issued. The error bits in the Status Register should be cleared before attempting a new program or erase command.

4.6 Block Erase command

The Block Erase command is used to erase a block. It sets all the bits within the selected block to '1'. All previous data in the block is lost.

If the block is protected then the erase operation will abort, the data in the block will not be changed and the Status Register will output the error.

Two Bus Write cycles are required to issue the command.

1. The first bus cycle sets up the Block Erase command.
2. The second latches the block address and starts the Program/Erase Controller.

If the second bus cycle is not the Block Erase Confirm code, Status Register bits SR4 and SR5 are set and the command is aborted.

Once the command is issued the bank enters Read Status Register mode and any read operation within the addressed bank will output the contents of the Status Register. A Read Array command is required to return the bank to Read Array mode.

During Block Erase operations the bank containing the block being erased will only accept the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend command, all other commands will be ignored.

The Block Erase operation aborts if Reset, $\overline{RP}$, goes to V_{IL}. As data integrity cannot be guaranteed when the Block Erase operation is aborted, the block must be erased again.

Refer to Dual Operations section for detailed information about simultaneous operations allowed in banks not being erased.

Typical Erase times are given in *Table 16: Program/Erase Times and Endurance Cycles*.

See *Appendix C*, *Figure 22: Block Erase Flowchart and Pseudo Code*, for a suggested flowchart for using the Block Erase command.

4.7 Program command

The program command is used to program a single Word to the memory array.

Two Bus Write cycles are required to issue the Program Command.

1. The first bus cycle sets up the Program command.
2. The second latches the address and data to be programmed and starts the Program/ Erase Controller.

Once the programming has started, read operations in the bank being programmed output the Status Register content.

During a Program operation, the bank containing the Word being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend command, all other commands will be ignored. A Read Array command is required to return the bank to Read Array mode.

Refer to Dual Operations section for detailed information about simultaneous operations allowed in banks not being programmed.

Typical Program times are given in *Table 16: Program/Erase Times and Endurance Cycles*.

The Program operation aborts if Reset, $\overline{RP}$, goes to V_{IL}. As data integrity cannot be guaranteed when the Program operation is aborted, the Word must be reprogrammed.

See *Appendix C*, *Figure 19: Program Flowchart and Pseudo Code*, for the flowchart for using the Program command.

4.8 Buffer Program command

The Buffer Program Command makes use of the device's 32-Word Write Buffer to speed up programming. Up to 32 Words can be loaded into the Write Buffer. The Buffer Program command dramatically reduces in-system programming time compared to the standard non-buffered Program command.

Four successive steps are required to issue the Buffer Program command.

1. The first Bus Write cycle sets up the Buffer Program command. The setup code can be addressed to any location within the targeted block.
   After the first Bus Write cycle, read operations in the bank will output the contents of the Status Register. Status Register bit SR7 should be read to check that the buffer is available (SR7 = 1). If the buffer is not available (SR7 = 0), re-issue the Buffer Program command to update the Status Register contents.
2. The second Bus Write cycle sets up the number of Words to be programmed. Value n is written to the same block address, where n+1 is the number of Words to be programmed.
3. Use n+1 Bus Write cycles to load the address and data for each Word into the Write Buffer. Addresses must lie within the range from the start address to the start address + n. Optimum performance is obtained when the start address corresponds to a 32 Word boundary. If the start address is not aligned to a 32 word boundary, the total programming time is doubled
4. The final Bus Write cycle confirms the Buffer Program command and starts the program operation.

All the addresses used in the Buffer Program operation must lie within the same block.

Invalid address combinations or failing to follow the correct sequence of Bus Write cycles will set an error in the Status Register and abort the operation without affecting the data in the memory array.

If the Status Register bits SR4 and SR5 are set to '1', the Buffer Program Command is not accepted. Clear the Status Register before re-issuing the command.

If the block being programmed is protected an error will be set in the Status Register and the operation will abort without affecting the data in the memory array.

During Buffer Program operations the bank being programmed will only accept the Read Array, Read Status Register, Read Electronic Signature, Read CFI Query and the Program/Erase Suspend command, all other commands will be ignored.

Refer to Dual Operations section for detailed information about simultaneous operations allowed in banks not being programmed.

See *Appendix C*, *Figure 20: Buffer Program Flowchart and Pseudo Code*, for a suggested flowchart on using the Buffer Program command.

4.9 Buffer Enhanced Factory Program command

The Buffer Enhanced Factory Program command has been specially developed to speed up programming in manufacturing environments where the programming time is critical.

It is used to program one or more Write Buffer(s) of 32 Words to a block. Once the device enters Buffer Enhanced Factory Program mode, the Write Buffer can be reloaded any number of times as long as the address remains within the same block. Only one block can be programmed at a time.

The use of the Buffer Enhanced Factory Program command requires certain operating conditions:

- The targeted block must be unprotected. if it is protected, the user must return the device to read mode.
- V_{PP} must be set to V_{PPH}.
- V_{DD} must be within operating range.
- Ambient temperature T_A must be 30°C ± 10°C.
- The start address must be aligned with the start of a 32 Word buffer boundary.
- The address must remain the Start Address throughout programming.

Dual operations are not supported during the Buffer Enhanced Factory Program operation and the command cannot be suspended.

The Buffer Enhanced Factory Program Command consists of three phases: the Setup Phase, the Program and Verify Phase, and the Exit Phase, See *Appendix C*, *Figure 25: Buffer Enhanced Factory Program Flowchart and Pseudo Code*, for a suggested flowchart on using the Buffer Program command and to *Table 6: Factory Program Command* for details on the Buffer Enhanced Factory Program command.

4.9.1 Setup phase

The Buffer Enhanced Factory Program command requires two Bus Write cycles to initiate the command.

1. The first Bus Write cycle sets up the Buffer Enhanced Factory Program command.
2. The second Bus Write cycle confirms the command.

After the confirm command is issued, read operations output the contents of the Status Register. The read Status Register command must not be issued as it will be interpreted as data to program.

The Status Register P/E.C. Bit SR7 should be read to check that the P/E.C. is ready to proceed to the next phase.

If an error is detected, SR4 goes high (set to ‘1’) and the Buffer Enhanced Factory Program operation is terminated. See Status Register section for details on the error.

4.9.2 Program and Verify phase

The Program and Verify Phase requires 32 cycles to program the 32 Words to the Write Buffer. The data is stored sequentially, starting at the first address of the Write Buffer, until the Write Buffer is full (32 Words). To program less than 32 Words, the remaining Words should be programmed with FFFFh.

Three successive steps are required to issue and execute the Program and Verify Phase of the command.

1. Use one Bus Write operation to latch the Start Address and the first Word to be programmed. The Status Register Bank Write Status bit SR0 should be read to check that the P/E.C. is ready for the next Word.
2. Each subsequent Word to be programmed is latched with a new Bus Write operation. The address must remain the Start Address as the P/E.C. increments the address location.If any address that is not in the same block as the Start Address is given, the Program and Verify Phase terminates. Status Register bit SR0 should be read between each Bus Write cycle to check that the P/E.C. is ready for the next Word.
3. Once the Write Buffer is full, the data is programmed sequentially to the memory array. After the program operation the device automatically verifies the data and reprograms if necessary.
   The Program and Verify phase can be repeated, without re-issuing the command, to program additional 32 Word locations as long as the address remains in the same block.
4. Finally, after all Words, or the entire block have been programmed, write one Bus Write operation to any address outside the block containing the Start Address, to terminate Program and Verify Phase.

Status Register bit SR0 must be checked to determine whether the program operation is finished. The Status Register may be checked for errors at any time but it must be checked after the entire block has been programmed.

4.9.3 Exit phase

Status Register P/E.C. bit SR7 set to ‘1’ indicates that the device has exited the Buffer Enhanced Factory Program operation and returned to Read Status Register mode. A full Status Register check should be done to ensure that the block has been successfully programmed. See the section on the Status Register for more details.

For optimum performance the Buffer Enhanced Factory Program command should be limited to a maximum of 100 program/erase cycles per block. If this limit is exceeded the internal algorithm will continue to work properly but some degradation in performance is possible. Typical program times are given in *Table 16*

See *Appendix C*, *Figure 25: Buffer Enhanced Factory Program Flowchart and Pseudo Code*, for a suggested flowchart on using the Buffer Enhanced Factory Program command.

4.10 Program/Erase Suspend command

The Program/Erase Suspend command is used to pause a Program or Block Erase operation. The command can be addressed to any bank.

The Program/Erase Resume command is required to restart the suspended operation.

One bus write cycle is required to issue the Program/Erase Suspend command. Once the Program/Erase Controller has paused bits SR7, SR6 and/ or SR2 of the Status Register will be set to '1'.

The following commands are accepted during Program/Erase Suspend:

- Program/Erase Resume
- Read Array (data from erase-suspended block or program-suspended Word is not valid)
- Read Status Register
- Read Electronic Signature
- Read CFI Query.

In addition, if the suspended operation was a Block Erase then the following commands are also accepted:

- Clear Status Register
- Program (except in erase-suspended block)
- Buffer Program (except in erase suspended blocks)

It is possible to accumulate multiple suspend operations. For example: suspend an erase operation, start a program operation, suspend the program operation, then read the array.

If a Program command is issued during a Block Erase Suspend, the erase operation cannot be resumed until the program operation has completed.

The Program/Erase Suspend command does not change the read mode of the banks. If the suspended bank was in Read Status Register, Read Electronic signature or Read CFI Query mode the bank remains in that mode and outputs the corresponding data.

Refer to Dual Operations section for detailed information about simultaneous operations allowed during Program/Erase Suspend.

During a Program/Erase Suspend, the device can be placed in standby mode by taking Chip Enable to V_{IH}. Program/erase is aborted if Reset, $\overline{RP}$, goes to V_{IL}.

See *Appendix C*, *Figure 21: Program Suspend & Resume Flowchart and Pseudo Code*, and *Figure 23: Erase Suspend & Resume Flowchart and Pseudo Code*, for flowcharts for using the Program/Erase Suspend command.

4.11 Program/Erase Resume command

The Program/Erase Resume command is used to restart the program or erase operation suspended by the Program/Erase Suspend command. One Bus Write cycle is required to issue the command. The command can be issued to any address.

The Program/Erase Resume command does not change the read mode of the banks. If the suspended bank was in Read Status Register, Read Electronic signature or Read CFI Query mode the bank remains in that mode and outputs the corresponding data.

If a Program command is issued during a Block Erase Suspend, then the erase cannot be resumed until the program operation has completed.

See *Appendix C*, *Figure 21: Program Suspend & Resume Flowchart and Pseudo Code*, and *Figure 23: Erase Suspend & Resume Flowchart and Pseudo Code*, for flowcharts for using the Program/Erase Resume command.

4.11.1 Protection Register Program command

The Protection Register Program command is used to program the user One-Time-Programmable (OTP) segments of the Protection Register and the two Protection Register Locks.

The device features 16 OTP segments of 128 bits and one OTP segment of 64 bits, as shown in *Figure 4: Protection Register Map*. The segments are programmed one Word at a time. When shipped all bits in the segment are set to '1'. The user can only program the bits to '0'.

Two Bus Write cycles are required to issue the Protection Register Program command.

1. The first bus cycle sets up the Protection
2. Register Program command.
3. The second latches the address and data to be programmed to the Protection Register and starts the Program/Erase Controller.

Read operations to the bank being programmed output the Status Register content after the program operation has started.

Attempting to program a previously protected Protection Register will result in a Status Register error.

The Protection Register Program cannot be suspended. Dual operations between the Parameter Bank and the Protection Register memory space are not allowed (see *Table 15: Dual Operation Limitations* for details).

The two Protection Register Locks are used to protect the OTP segments from further modification. The protection of the OTP segments is not reversible. Refer to *Figure 4: Protection Register Map*, and *Table 8: Protection Register Lock Bits*, for details on the Lock bits.

See *Appendix C*, *Figure 24: Protection Register Program Flowchart and Pseudo Code*, for a flowchart for using the Protection Register Program command.

4.12 Set Configuration Register command

The Set Configuration Register command is used to write a new value to the Configuration Register.

Two Bus Write cycles are required to issue the Set Configuration Register command.

1. The first cycle sets up the Set Configuration Register command and the address corresponding to the Configuration Register content.
2. The second cycle writes the Configuration Register data and the confirm command.

The Configuration Register data must be written as an address during the bus write cycles, that is DQ0 = CR0, DQ1 = CR1, …, DQ15 = CR15. Addresses A0-A22 are ignored.

Read operations output the array content after the Set Configuration Register command is issued.

The Read Electronic Signature command is required to read the updated contents of the Configuration Register.

Table 5. Standard Commands

Commands	Cycles	Bus Operations(1)					
		1st Cycle			2nd Cycle		
		Op.	Add	Data	Op.	Add	Data
Read Array	1+	Write	BKA	FFh	Read	WA	RD
Read Status Register	1+	Write	X	70h	Read	BKA(2)	SRD
Read Electronic Signature	1+	Write	X	90h	Read	BKA(2)	ESD
Read CFI Query	1+	Write	BKA	98h	Read	BKA(2)	QD
Clear Status Register	1	Write	BKA	50h			
Block Erase	2	Write	BKA or BA(3)	20h	Write	BA	D0h
Program	2	Write	BKA or WA(3)	40h or 10h	Write	WA	PD
Buffer Program	n+4	Write	BA	E8h	Write	BA	n
		Write	PA_1	PD_1	Write	PA_2	PD_2
		Write	PA_{n+1}(4)	PD_{n+1}(4)	Write	X	D0h
Program/Erase Suspend	1	Write	X	B0h			
Protection Register Program	2	Write	PRA	C0h	Write	PRA	PRD
Program/Erase Resume	1	Write	X	D0h			
Set Configuration Register	2	Write	CRD	60h	Write	CRD	03h

1. X = Don't Care, WA=Word Address in targeted bank, RD=Read Data, SRD=Status Register Data, ESD=Electronic Signature Data, QD=Query Data, BA=Block Address, BKA= Bank Address, PD=Program Data, PRA = Protection Register Address, PRD = Protection Register Data, CRD=Configuration Register Data.
2. Must be same bank as in the first cycle. The signature addresses are listed in *Table 7*
3. Any address within the bank can be used.
4. n+1 is the number of Words to be programmed.

Table 6. Factory Program Command

Command	Phase	Cycles	Bus Write Operations(1)										
			1st		2nd		3rd			Final -1		Final	
			Add	Data	Add	Data	Add	Data		Add	Data	Add	Data
Buffer Enhanced Factory Program	Setup	2	BKA or $WA^{(2)}$	80h	WA_1	D0h							
	Program/ Verify(3)	≥32	WA_1	PD_1	WA_1	PD_2	WA_1	PD_3		WA_1	PD_{31}	WA_1	PD_{32}
	Exit	1	NOT BA_1(4)	X									

1. WA=Word Address in targeted bank, BKA= Bank Address, PD=Program Data, BA=Block Address, X = Don't Care.
2. Any address within the bank can be used.
3. The Program/Verify phase can be executed any number of times as long as the data is to be programmed to the same block.
4. WA_1 is the Start Address, NOT BA_1 = Not Block Address of WA_1.

Table 7. Electronic Signature Codes

Code		Address (h)	Data (h)
Manufacturer Code		Bank Address + 00	0020
Device Code	Top	Bank Address + 01	88C6h (M58LT128GST)
	Bottom	Bank Address + 01	88C7h (M58LT128GSB)
Die Revision Code		Block Address + 03	DRC(1)
Configuration Register		Bank Address + 05	CR(1)
Protection Register PR0	ST Factory Default	Bank Address + 80	bit 0 = '0'
	OTP Area Permanently Locked		bit 1 = '0'
Protection Register PR0		Bank Address + 81 Bank Address + 84	Unique Device Number
		Bank Address + 85 Bank Address + 88	OTP Area
Protection Register PR1 through PR16 Lock		Bank Address + 89	PRLD
Protection Registers PR1-PR16		Bank Address + 8A Bank Address + 109	OTP Area

1. CR = Configuration Register, DRC = Die Revision Code.

Figure 4. Protection Register Map

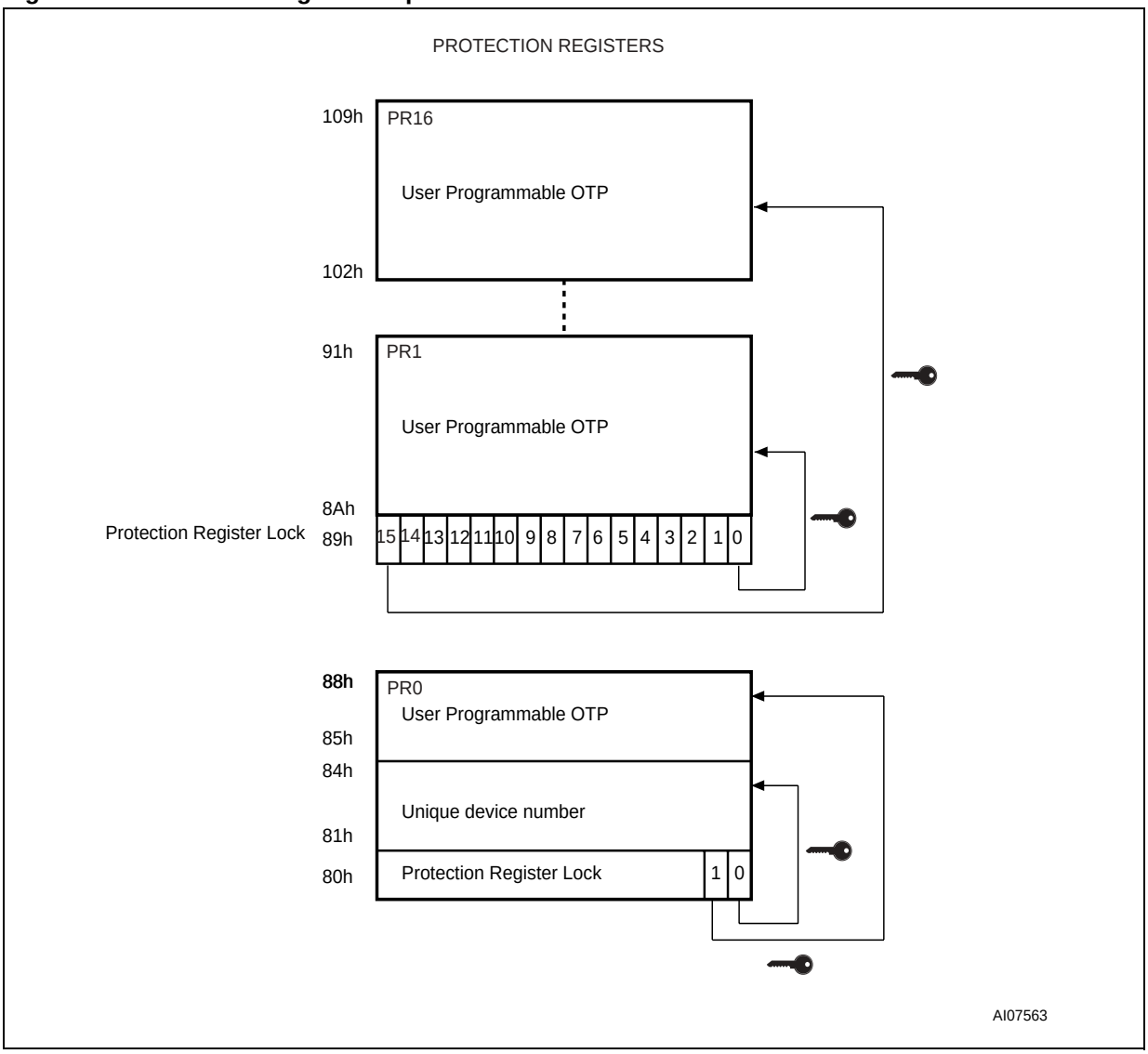


Table 8. Protection Register Lock Bits

Lock			Description
Number	**Address**	**Bits**	
Protection Register Lock 1	80h	Bit 0	Read-only bit preprogrammed to ‘0’ protect Unique Device Number (address 81h to 84h in PR0)
		Bit 1	protects 64bits of OTP segment (address 85h to 88h in PR0) when set to ‘0’ Default Value is ‘1’
Protection Register Lock 2	89h	Bit 0	protects 128bits of OTP segment PR1
		Bit 1	protects 128bits of OTP segment PR2
		Bit 2	protects 128bits of OTP segment PR3
		- - -	- - -
		Bit 13	protects 128bits of OTP segment PR14
		Bit 14	protects 128bits of OTP segment PR15
		Bit 15	protects 128bits of OTP segment PR16

5 Status Register

The Status Register provides information on the current or previous program or erase operations. Issue a Read Status Register command to read the contents of the Status Register, refer to Read Status Register Command section for more details. To output the contents, the Status Register is latched and updated on the falling edge of the Chip Enable or Output Enable signals and can be read until Chip Enable or Output Enable returns to V_{IH}. The Status Register can only be read using single Asynchronous or Single Synchronous reads. Bus Read operations from any address within the bank, always read the Status Register during program and erase operations.

The various bits convey information about the status and any errors of the operation. Bits SR7, SR6, SR2 and SR0 give information on the status of the device and are set and reset by the device. Bits SR5, SR4, SR3 and SR1 give information on errors, they are set by the device but must be reset by issuing a Clear Status Register command or a hardware reset. If an error bit is set to ‘1’ the Status Register should be reset before issuing another command.

Refer to *Table 9: Status Register Bits* in conjunction with the following text descriptions.

5.1 Program/Erase Controller Status Bit (SR7)

The Program/Erase Controller Status bit indicates whether the Program/Erase Controller is active or inactive in any bank.

When the Program/Erase Controller Status bit is Low (set to ‘0’), the Program/Erase Controller is active; when the bit is High (set to ‘1’), the Program/Erase Controller is inactive, and the device is ready to process a new command.

The Program/Erase Controller Status bit is Low immediately after a Program/Erase Suspend command is issued until the Program/Erase Controller pauses. After the Program/Erase Controller pauses the bit is High.

5.2 Erase Suspend Status Bit (SR6)

The Erase Suspend Status bit indicates that an erase operation has been suspended in the addressed block. When the Erase Suspend Status bit is High (set to ‘1’), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

The Erase Suspend Status bit should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive). SR6 is set within the Erase Suspend Latency time of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Erase Suspend Status bit returns Low.

5.3 Erase Status Bit (SR5)

The Erase Status bit is used to identify if there was an error during a block or bank erase operation.

When the Erase Status bit is High (set to ‘1’), the Program/Erase Controller has applied the maximum number of pulses to the block or bank and still failed to verify that it has erased correctly.

The Erase Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

Once set High, the Erase Status bit must be set Low by a Clear Status Register command or a hardware reset before a new erase command is issued, otherwise the new command will appear to fail.

5.4 Program Status Bit (SR4)

The Program Status bit is used to identify if there was an error during a program operation.

The Program Status bit should be read once the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Program Status bit is High (set to ‘1’), the Program/Erase Controller has applied the maximum number of pulses to the Word and still failed to verify that it has programmed correctly.

Attempting to program a '1' to an already programmed bit while $V_{PP} = V_{PPH}$ will also set the Program Status bit High. If V_{PP} is different from V_{PPH}, SR4 remains Low (set to '0') and the attempt is not shown.

Once set High, the Program Status bit must be set Low by a Clear Status Register command or a hardware reset before a new program command is issued, otherwise the new command will appear to fail.

5.5 V_{PP} Status Bit (SR3)

The V_{PP} Status bit is used to identify an invalid voltage on the V_{PP} pin during program and erase operations. The V_{PP} pin is only sampled at the beginning of a program or erase operation. Program and erase operations are not guaranteed if V_{PP} becomes invalid during an operation.

When the V_{PP} Status bit is Low (set to ‘0’), the voltage on the V_{PP} pin was sampled at a valid voltage.

when the V_{PP} Status bit is High (set to ‘1’), the V_{PP} pin has a voltage that is below the V_{PP} Lockout Voltage, V_{PPLK}, the memory is protected and program and erase operations cannot be performed.

Once set High, the V_{PP} Status bit must be set Low by a Clear Status Register command or a hardware reset before a new program or erase command is issued, otherwise the new command will appear to fail.

5.6 Program Suspend Status Bit (SR2)

The Program Suspend Status bit indicates that a program operation has been suspended in the addressed block. The Program Suspend Status bit should only be considered valid when the Program/Erase Controller Status bit is High (Program/Erase Controller inactive).

When the Program Suspend Status bit is High (set to ‘1’), a Program/Erase Suspend command has been issued and the memory is waiting for a Program/Erase Resume command.

SR2 is set within the Program Suspend Latency time of the Program/Erase Suspend command being issued therefore the memory may still complete the operation rather than entering the Suspend mode.

When a Program/Erase Resume command is issued the Program Suspend Status bit returns Low.

SR1. Reserved.

5.7 Bank Write/Multiple Word Program Status Bit (SR0)

The Bank Write Status bit indicates whether the addressed bank is programming or erasing. In Buffer Enhanced Factory Program mode the Multiple Word Program bit shows if the device is ready to accept a new Word to be programmed to the memory array.

The Bank Write Status bit should only be considered valid when the Program/Erase Controller Status SR7 is Low (set to ‘0’).

When both the Program/Erase Controller Status bit and the Bank Write Status bit are Low (set to ‘0’), the addressed bank is executing a program or erase operation. When the Program/Erase Controller Status bit is Low (set to ‘0’) and the Bank Write Status bit is High (set to ‘1’), a program or erase operation is being executed in a bank other than the one being addressed.

In Buffer Enhanced Factory Program mode if Multiple Word Program Status bit is Low (set to ‘0’), the device is ready for the next Word, if the Multiple Word Program Status bit is High (set to ‘1’) the device is not ready for the next Word.

For further details on how to use the Status Register, see the Flowcharts and Pseudo codes provided in *Appendix C*.

Table 9. Status Register Bits

Bit	Name	Type	Logic Level	Definition	
SR7	P/E.C. Status	Status	'1'	Ready	
			'0'	Busy	
SR6	Erase Suspend Status	Status	'1'	Erase Suspended	
			'0'	Erase In progress or Completed	
SR5	Erase Status	Error	'1'	Erase Error	
			'0'	Erase Success	
SR4	Program Status	Error	'1'	Program Error	
			'0'	Program Success	
SR3	V_{PP} Status	Error	'1'	V_{PP} Invalid, Abort	
			'0'	V_{PP} OK	
SR2	Program Suspend Status	Status	'1'	Program Suspended	
			'0'	Program In Progress or Completed	
SR1	Reserved				
SR0	Bank Write Status	Status	'1'	SR7 = '1'	Not Allowed
				SR7 = '0'	Program or erase operation in a bank other than the addressed bank
			'0'	SR7 = '1'	No Program or erase operation in the device
				SR7 = '0'	Program or erase operation in addressed bank
	Multiple Word Program Status (Enhanced Factory Program mode)	Status	'1'	SR7 = '1'	Not Allowed
				SR7 = '0'	the device is NOT ready for the next Word
			'0'	SR7 = '1'	the device is exiting from BEFP
				SR7 = '0'	the device is ready for the next Word

1. Logic level '1' is High, '0' is Low.

6 Configuration Register

The Configuration Register is used to configure the type of bus access that the memory will perform. Refer to Read Modes section for details on read operations.

The Configuration Register is set through the Command Interface using the Set Configuration Register command. After a reset or power-up the device is configured for asynchronous read (CR15 = 1). The Configuration Register bits are described in *Table 10* They specify the selection of the burst length, burst type, burst X latency and the read operation. Refer to *Figure 5* and *Figure 6* for examples of synchronous burst configurations.

6.1 Read Select Bit (CR15)

The Read Select bit, CR15, is used to switch between Asynchronous and Synchronous Read operations.

When the Read Select bit is set to '1', read operations are asynchronous; when the Read Select bit is set to '0', read operations are synchronous.

Synchronous Burst Read is supported in both parameter and main blocks and can be performed across banks.

On reset or power-up the Read Select bit is set to '1' for asynchronous access.

6.2 X-Latency Bits (CR13-CR11)

The X-Latency bits are used during Synchronous Read operations to set the number of clock cycles between the address being latched and the first data becoming available. For correct operation the X-Latency bits can only assume the values in *Table 10: Configuration Register*.

The correspondence between X-Latency settings and the maximum sustainable frequency must be calculated taking into account some system parameters. Two conditions must be satisfied:

1. Depending on whether t_{AVK_CPU} or t_{DELAY} is supplied either one of the following two equations must be satisfied:
   $(n + 1)\ t_K \geq t_{AVQV} - t_{AVK\_CPU} + t_{QVK\_CPU}$
   $(n + 2)\ t_K \geq t_{AVQV} + t_{DELAY} + t_{QVK\_CPU}$
2. and also
   $t_K > t_{KQV} + t_{QVK\_CPU}$

where

- n is the chosen X-Latency configuration code
- t_K is the clock period
- t_{AVK_CPU} is clock to address valid, $\overline{L}$ Low, or $\overline{E}$ Low, whichever occurs last
- t_{DELAY} is address valid, $\overline{L}$ Low, or $\overline{E}$ Low to clock, whichever occurs last
- t_{QVK_CPU} is the data setup time required by the system CPU,
- t_{KQV} is the clock to data valid time
- t_{AVQV} is the random access time of the device.

Refer to *Figure 5: X-Latency and Data Output Configuration Example*.

6.3 Wait Polarity Bit (CR10)

The Wait Polarity bit is used to set the polarity of the Wait signal used in Synchronous Burst Read mode. During Synchronous Burst Read mode the Wait signal indicates whether the data output are valid or a WAIT state must be inserted.

When the Wait Polarity bit is set to '0' the Wait signal is active Low. When the Wait Polarity bit is set to '1' the Wait signal is active High.

6.4 Data Output Configuration Bit (CR9)

The Data Output Configuration bit is used to configure the output to remain valid for either one or two clock cycles during synchronous mode.

When the Data Output Configuration Bit is '0' the output data is valid for one clock cycle, when the Data Output Configuration Bit is '1' the output data is valid for two clock cycles.

The Data Output Configuration must be configured using the following condition:

- $t_K > t_{KQV} + t_{QVK\_CPU}$

where

- t_K is the clock period
- t_{QVK_CPU} is the data setup time required by the system CPU
- t_{KQV} is the clock to data valid time.

If this condition is not satisfied, the Data Output Configuration bit should be set to '1' (two clock cycles). Refer to *Figure 5: X-Latency and Data Output Configuration Example*.

6.5 Wait Configuration Bit (CR8)

The Wait Configuration bit is used to control the timing of the Wait output pin, WAIT, in Synchronous Burst Read mode.

When WAIT is asserted, Data is Not Valid and when WAIT is deasserted, Data is Valid.

When the Wait Configuration bit is Low (set to '0') the Wait output pin is asserted during the WAIT state. When the Wait Configuration bit is High (set to '1'), the Wait output pin is asserted one data cycle before the WAIT state.

6.6 Burst Type Bit (CR7)

The Burst Type bit determines the sequence of addresses read during Synchronous Burst Reads.

The Burst Type bit is High (set to '1'), as the memory outputs from sequential addresses only.

See *Table 11: Burst Type Definition*, for the sequence of addresses output from a given starting address in sequential mode.

6.7 Valid Clock Edge Bit (CR6)

The Valid Clock Edge bit, CR6, is used to configure the active edge of the Clock, K, during synchronous read operations. When the Valid Clock Edge bit is Low (set to ’0’) the falling edge of the Clock is the active edge. When the Valid Clock Edge bit is High (set to ’1’) the rising edge of the Clock is the active edge.

6.8 Wrap Burst Bit (CR3)

The Wrap Burst bit, CR3, is used to select between wrap and no wrap. Synchronous burst reads can be confined inside the 4, 8 or 16 Word boundary (wrap) or overcome the boundary (no wrap).

When the Wrap Burst bit is Low (set to ‘0’) the burst read wraps. When it is High (set to ‘1’) the burst read does not wrap.

6.9 Burst length Bits (CR2-CR0)

The Burst Length bits are used to set the number of Words to be output during a Synchronous Burst Read operation as result of a single address latch cycle.

They can be set for 4 Words, 8 Words, 16 Words or continuous burst, where all the Words are read sequentially. In continuous burst mode the burst sequence can cross bank boundaries.

In continuous burst mode, in 4, 8 or 16 Words no-wrap, depending on the starting address, the device asserts the WAIT signal to indicate that a delay is necessary before the data is output.

If the starting address is aligned to an 8 Word boundary no WAIT states are needed and the WAIT output is not asserted.

If the starting address is not aligned to the 8 Word boundary, WAIT will be asserted when the burst sequence crosses the first 16 Word boundary to indicate that the device needs an internal delay to read the successive Words in the array.

In the worst case, the number of WAIT states is one clock cycle less than the latency setting. The exact number is reported in *Table 12: Wait at the Boundary*.

WAIT will be asserted only once during a continuous burst access. See also *Table 11: Burst Type Definition*.

CR14, CR5 and **CR4** are reserved for future use.

Table 10. Configuration Register

Bit	Description	Value	Description
CR15	Read Select	0	Synchronous Read
		1	Asynchronous Read (Default at power-on)
CR14	Reserved		
CR13-CR11	X-Latency	010	2 clock latency(1)
		011	3 clock latency
		100	4 clock latency
		101	5 clock latency
		110	6 clock latency
		111	7 clock latency (default)
		Other configurations reserved	
CR10	Wait Polarity	0	WAIT is active Low (default)
		1	WAIT is active High
CR9	Data Output Configuration	0	Data held for one clock cycle
		1	Data held for two clock cycles (default)(1)
CR8	Wait Configuration	0	WAIT is active during WAIT state (default)
		1	WAIT is active one data cycle before WAIT state(1)
CR7	Burst Type	0	Reserved
		1	Sequential (default)
CR6	Valid Clock Edge	0	Falling Clock edge
		1	Rising Clock edge (default)
CR5-CR4	Reserved		
CR3	Wrap Burst	0	Wrap
		1	No Wrap (default)
CR2-CR0	Burst Length	001	4 Words
		010	8 Words
		011	16 Words
		111	Continuous (default)

1. The combination X-Latency=2, Data held for two clock cycles and Wait active one data cycle before the WAIT state is not supported.

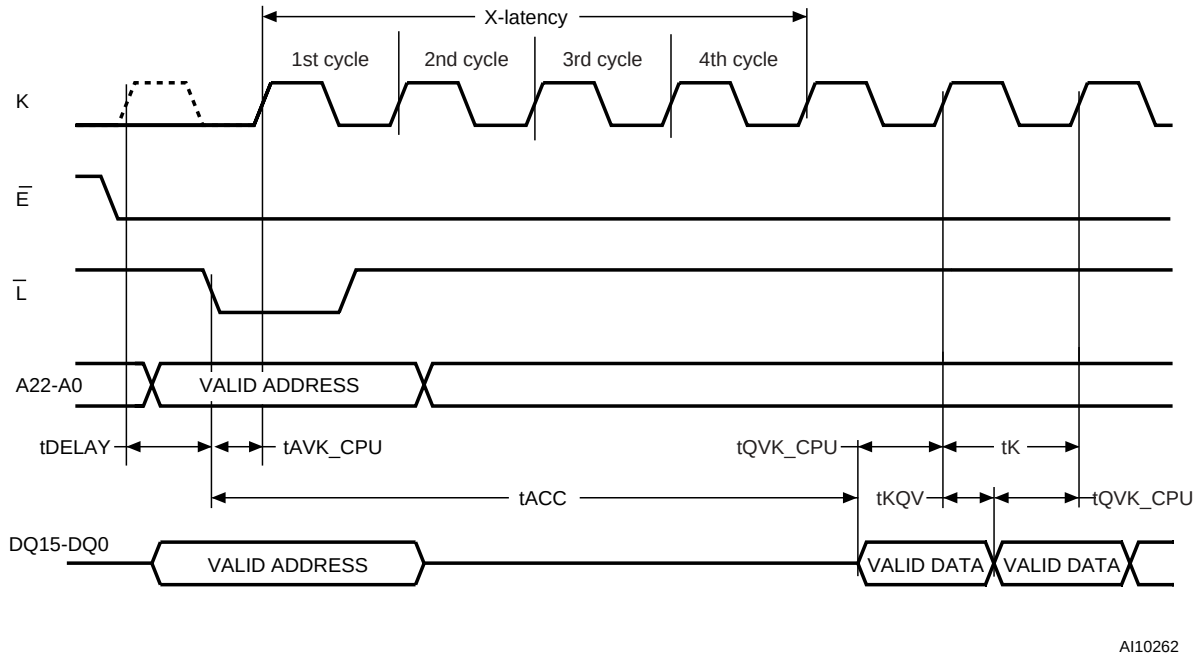
Table 11. Burst Type Definition

Mode	Start Add.	Sequential			Continuous Burst
		4 Words	8 Words	16 Words	
Wrap	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-3-4-5-6...
	1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-4-5-6-7...
	2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-5-6-7-8...
	3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-6-7-8-9...
	...				
	7	7-4-5-6	7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-10-11-12-13...
	...				
	12	12-13-14-15	12-13-14-15-8-9-10-11	12-13-14-15-0-1-2-3-4-5-6-7-8-9-10-11	12-13-14-15-16-17...
	13	13-14-15-12	13-14-15-8-9-10-11-12	13-14-15-0-1-2-3-4-5-6-7-8-9-10-11-12	13-14-15-16-17-18...
	14	14-15-12-13	14-15-8-9-10-11-12-13	14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-17-18-19...
	15	15-12-13-14	15-8-9-10-11-12-13-14	15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-18-19-20...
No-wrap	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	Same as for Wrap (Wrap /No Wrap has no effect on Continuous Burst)
	1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8--9-10-11-12-13-14-15-16	
	2	2-3-4-5	2-3-4-5-6-7-8-9...	2-3-4-5--6-7-8-9-10-11-12-13-14-15-16-17	
	3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	
	...				
	7	7-8-9-10	7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-15-16-17-18-19-20-21-22	
	...				
	12	12-13-14-15	12-13-14-15-16-17-18-19	12-13-14-15-16-17-18-19-20-21-22-23-24-25-26-27	
	13	13-14-15-16	13-14-15-16-17-18-19-20	13-14-15-16-17-18-19-20-21-22-23-24-25-26-27-28	
	14	14-15-16-17	14-15-16-17-18-19-20-21	14-15-16-17-18-19-20-21-22-23-24-25-26-27-28-29	
	15	15-16-17-18	15-16-17-18-19-20-21-22	15-16-17-18-19-20-21-22-23-24-25-26-27-28-29-30	

Table 12. Wait at the Boundary

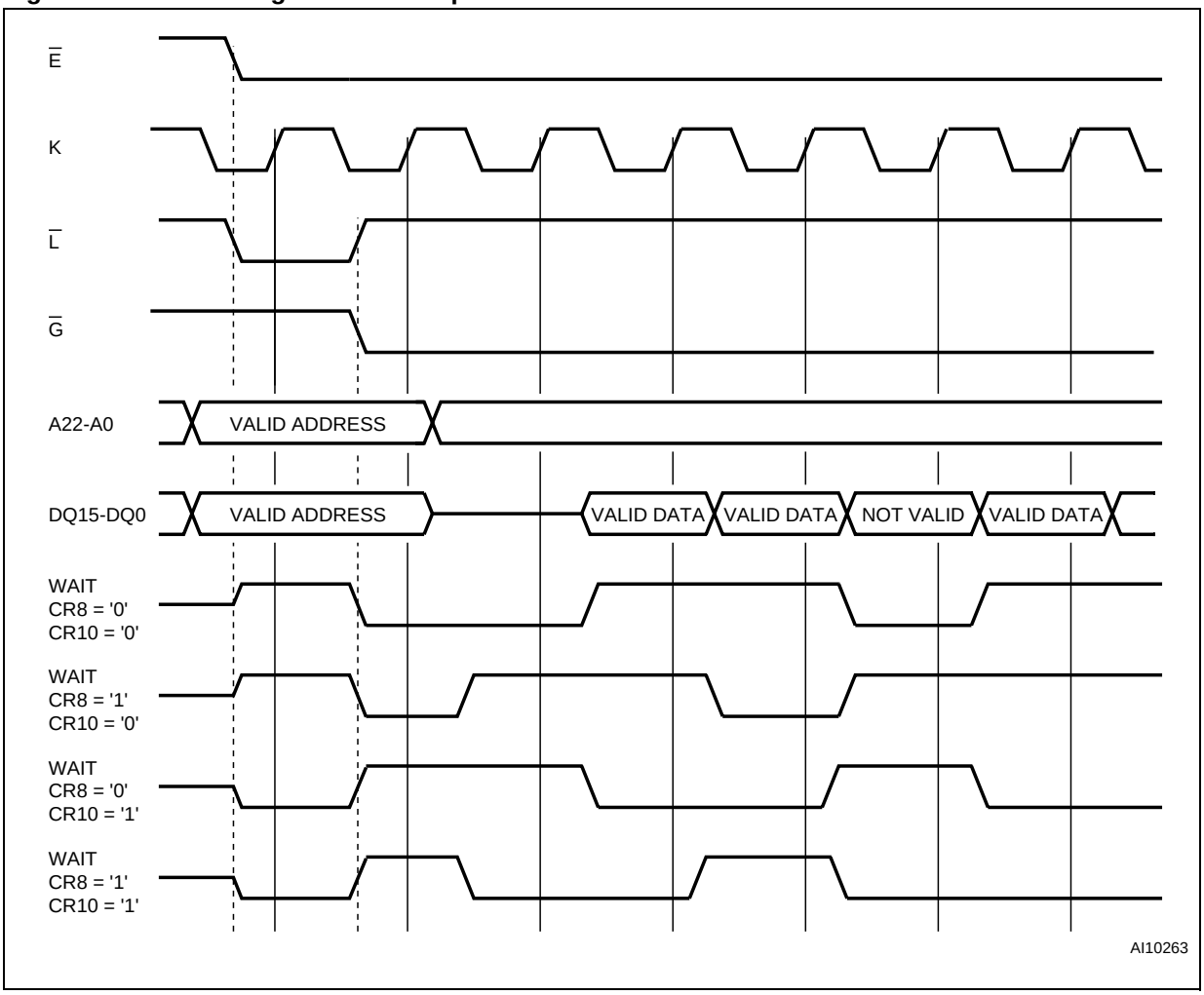
Start Address	Number of WAIT states					
	X-Latency = 7	X-Latency = 6	X-Latency = 5	X-Latency = 4	X-Latency = 3	X-Latency = 2
0	0	0	0	0	0	0
1	0	0	0	0	0	0
2	1	0	0	0	0	0
3	2	1	0	0	0	0
4	3	2	1	0	0	0
5	4	3	2	1	0	0
6	5	4	3	2	1	0
7	6	5	4	3	2	1

Figure 5. X-Latency and Data Output Configuration Example



1. The settings shown are X-latency = 4, Data Output held for one clock cycle.

Figure 6. Wait Configuration Example



7 Read modes

Read operations can be performed in two different ways depending on the settings in the Configuration Register. If the clock signal is ‘don’t care’ for the data output, the read operation is asynchronous; if the data output is synchronized with clock, the read operation is synchronous.

The read mode and format of the data output are determined by the Configuration Register. (See Configuration Register section for details). All banks support both asynchronous and synchronous read operations.

7.1 Asynchronous Read modes

In Asynchronous Read operations the clock signal is ‘don’t care’. The device outputs the data corresponding to the address latched, that is the memory array, Status Register, Common Flash Interface or Electronic Signature depending on the command issued. CR15 in the Configuration Register must be set to ‘1’ for asynchronous operations. In Asynchronous Read mode, the WAIT signal is always deasserted.

The device features an Automatic Standby mode. During Asynchronous Read operations, after a bus inactivity of 150ns, the device automatically switches to the Automatic Standby mode. In this condition the power consumption is reduced to the standby value and the outputs are still driven.

Asynchronous Read operations can be performed in two different ways, Asynchronous Random Read and Asynchronous Page Read.

7.1.1 Asynchronous Random Read

Asynchronous Random Read operations are controlled by the Latch Enable, $\overline{L}$, signal.

A valid bus operation involves setting the desired address on the Address Inputs, setting Chip Enable and Latch Enable Low, V_{IL}, and keeping Write Enable High, V_{IH}. The address is latched on the rising edge of Latch Enable, $\overline{L}$, before the value is output on the data bus. Once latched, the Address Inputs can change. Set Output Enable Low, V_{IL}, to read the data on the Data Inputs/Outputs.

See *Table 22: Asynchronous Read AC Characteristics*, and *Figure 9: Asynchronous Random Access Read AC Waveforms* for details.

7.1.2 Asynchronous Page Read

Only Asynchronous Page Read takes full advantage of the internal page storage so different timings are applied. In Asynchronous Page Read mode, a Page of data is internally read and stored in a Page Buffer. The Page size is 8 Words and is addressed by address inputs A0, A1 and A2.

The first read operation within the Page has the normal access time (t_{AVQV}), subsequent reads within the same Page have much shorter access times (t_{AVQV1}). If the Page changes then the normal longer timings apply again.

See *Table 22: Asynchronous Read AC Characteristics*, *Figure 10: Asynchronous Page Read AC Waveforms* for details.

7.2 Synchronous Burst Read modes

In Synchronous Burst Read mode the data is output in bursts synchronized with the clock. It is possible to perform burst reads across bank boundaries.

Synchronous Burst Read mode can only be used to read the memory array. For other read operations, such as Read Status Register, Read CFI and Read Electronic Signature, Single Synchronous Read or Asynchronous Random Access Read must be used.

In Synchronous Burst Read mode the flow of the data output depends on parameters that are configured in the Configuration Register.

A burst sequence starts at the first clock edge (rising or falling depending on Valid Clock Edge bit CR6 in the Configuration Register) after the falling edge of Latch Enable or Chip Enable, whichever occurs last. Addresses are internally incremented and data is output on each data cycle after a delay which depends on the X latency bits CR13-CR11 of the Configuration Register.

The number of Words to be output during a Synchronous Burst Read operation can be configured as 4 Words, 8 Words, 16 Words or Continuous (Burst Length bits CR2-CR0). The data can be configured to remain valid for one or two clock cycles (Data Output Configuration bit CR9).

The order of the data output can be modified through the Wrap Burst bit in the Configuration Register. The burst sequence is sequential and can be confined inside the 4, 8 or 16 Word boundary (Wrap) or overcome the boundary (No Wrap).

The WAIT signal may be asserted to indicate to the system that an output delay will occur. This delay will depend on the starting address of the burst sequence and on the burst configuration.

WAIT is asserted during the X latency, the WAIT state and at the end of a 4, 8 and 16 Word burst. It is only deasserted when output data are valid or when $\overline{G}$ is at V_{IH}. In Continuous Burst Read mode a WAIT state will occur when crossing the first 16 Word boundary. If the starting address is aligned to the Burst Length (4, 8 or 16 Words) the wrapped configuration has no impact on the output sequence.

The WAIT signal can be configured to be active Low or active High by setting CR10 in the Configuration Register.

See *Table 23: Synchronous Read AC Characteristics*, and *Figure 11: Synchronous Burst Read AC Waveforms*, for details.

7.2.1 Synchronous Burst Read Suspend

A Synchronous Burst Read operation can be suspended, freeing the data bus for other higher priority devices. It can be suspended during the initial access latency time (before data is output) in which case the initial latency time can be reduced to zero, or after the device has output data. When the Synchronous Burst Read operation is suspended, internal array sensing continues and any previously latched internal data is retained. A burst sequence can be suspended and resumed as often as required as long as the operating conditions of the device are met.

A Synchronous Burst Read operation is suspended when Chip Enable, $\overline{E}$, is Low and the current address has been latched (on a Latch Enable rising edge or on a valid clock edge). The Clock signal is then halted at V_{IH} or at V_{IL}, and Output Enable, $\overline{G}$, goes High.

When Output Enable, $\overline{G}$, becomes Low again and the Clock signal restarts, the Synchronous Burst Read operation is resumed exactly where it stopped.

WAIT being gated by $\overline{E}$, it will remain active and will not revert to high impedance when $\overline{G}$ goes High. So if two or more devices are connected to the system's READY signal, to prevent bus contention the WAIT signal of the M58LT128GST and M58LT128GSB should not be directly connected to the system's READY signal.

WAIT will revert to high-impedance when Output Enable, $\overline{G}$, or Chip Enable, $\overline{E}$, goes High.

See *Table 23: Synchronous Read AC Characteristics*, and *Figure 13: Synchronous Burst Read Suspend AC Waveforms*, for details.

7.2.2 Single Synchronous Read mode

Single Synchronous Read operations are similar to Synchronous Burst Read operations except that the memory outputs the same data to the end of the operation.

Synchronous Single Reads are used to read the Electronic Signature, Status Register, CFI, Configuration Register Status, or Protection Register. When the addressed bank is in Read CFI, Read Status Register or Read Electronic Signature mode, the WAIT signal is deasserted when Output Enable, $\overline{G}$, is at V_{IH} or for the one clock cycle during which output data is valid. Otherwise, it is asserted.

See *Table 23: Synchronous Read AC Characteristics*, and *Figure 11: Synchronous Burst Read AC Waveforms*, for details.

8 Dual Operations and Multiple Bank architecture

The Multiple Bank Architecture of the M58LT128GST and M58LT128GSB gives greater flexibility for software developers to split the code and data spaces within the memory array. The Dual Operations feature simplifies the software management of the device by allowing code to be executed from one bank while another bank is being programmed or erased.

The Dual Operations feature means that while programming or erasing in one bank, read operations are possible in another bank with zero latency (only one bank at a time is allowed to be in program or erase mode).

If a read operation is required in a bank, which is programming or erasing, the program or erase operation can be suspended.

Also if the suspended operation was erase then a program command can be issued to another block, so the device can have one block in Erase Suspend mode, one programming and other banks in read mode.

Bus Read operations are allowed in another bank between setup and confirm cycles of program or erase operations.

By using a combination of these features, read operations are possible at any moment in the M58LT128GST and M58LT128GSB devices.

Dual operations between the Parameter Bank and either of the CFI, or the Electronic Signature memory space are not allowed. *Table 15* shows which dual operations are allowed or not between the CFI, the Electronic Signature locations and the memory array.

Table 13 and *Table 14* show the dual operations possible in other banks and in the same bank.

Table 13. Dual Operations Allowed In Other Banks

Status of bank	Commands allowed in another bank							
	Read Array	Read Status Register	Read CFI Query	Read Electronic Signature	Program, Buffer Program	Block Erase	Program/ Erase Suspend	Program/ Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Programming	Yes	Yes	Yes	Yes	–	–	Yes	–
Erasing	Yes	Yes	Yes	Yes	–	–	Yes	–
Program Suspended	Yes	Yes	Yes	Yes	–	–	–	Yes
Erase Suspended	Yes	Yes	Yes	Yes	Yes	–	–	Yes

Table 14. Dual Operations Allowed In Same Bank

Status of bank	Commands allowed in same bank							
	Read Array	Read Status Register	Read CFI Query	Read Electronic Signature	Program, Buffer Program	Block Erase	Program/ Erase Suspend	Program/ Erase Resume
Idle	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Programming	–(1)	Yes	Yes	Yes	–	–	Yes	–
Erasing	–(1)	Yes	Yes	Yes	–	–	Yes	–
Program Suspended	Yes(2)	Yes	Yes	Yes	–	–	–	Yes
Erase Suspended	Yes(2)	Yes	Yes	Yes	Yes(2)	–	–	Yes

1. The Read Array command is accepted but the data output is not guaranteed until the Program or Erase has completed.
2. Not allowed in the Word that is being erased or programmed.

Table 15. Dual Operation Limitations

Current Status		Commands allowed			
		Read CFI / Electronic Signature	Read Parameter Blocks	Read Main Blocks	
				Located in Parameter Bank	Not Located in Parameter Bank
Programming / Erasing Parameter Blocks		No	No	No	Yes
Programming / Erasing Main Blocks	Located in Parameter Bank	No	No	No	Yes
	Not Located in Parameter Bank	No	Yes	Yes	In Different Bank Only

9 Program and Erase times and Endurance cycles

The Program and Erase times and the number of Program/ Erase cycles per block are shown in *Table 16* Exact erase times may change depending on the memory array condition. The best case is when all the bits in the block are at '0' (pre-programmed). The worst case is when all the bits in the block are at '1' (not preprogrammed). Usually, the system overhead is negligible with respect to the erase time. In the M58LT128GST and M58LT128GSB the maximum number of Program/Erase cycles depends on the V_{PP} voltage supply used.

Table 16. Program/Erase Times and Endurance Cycles

Parameter			Condition(1)(2)	Min	Typ	Typical after 100kW/E Cycles	Max	Unit
$V_{PP} = V_{DD}$	Erase	Parameter Block (16 KWord)			0.4	1	2.5	s
		Main Block (64 KWord)	Preprogrammed		1	3	4	s
			Not Preprogrammed		1.2		4	s
	Program(3)	SIngle Cell	Word Program		30		60	µs
			Buffer Program		30		60	µs
		Single Word	Word Program		90		180	µs
			Buffer Program		90		180	µs
		Buffer (32 Words) (Buffer Program)			440		880	µs
		Main Block (64 KWord)			880			ms
	Suspend Latency	Program			20		25	µs
		Erase			20		25	µs
	Program/Erase Cycles (per Block)	Main Blocks		100,000				cycles
		Parameter Blocks		100,000				cycles

Parameter			Condition[1][2]	Min	Typ	Typical after 100kW/E Cycles	Max	Unit
$V_{PP} = V_{PPH}$	Erase	Parameter Block (16 KWord)			0.4		2.5	s
		Main Block (64 KWord)			1		4	s
	Program[3]	Single Cell	Word Program		30		60	µs
		Single Word	Word Program		85		170	µs
			Buffer Enhanced Factory Program[4]		10			µs
		Buffer (32 Words)	Buffer Program		340		680	µs
			Buffer Enhanced Factory Program		320			µs
		Main Block (64 KWords)	Buffer Program		640			ms
			Buffer Enhanced Factory Program		640			ms
		Bank (16 Mbits)	Buffer Program		10			s
			Buffer Enhanced Factory Program		10			s
	Program/Erase Cycles (per Block)	Main Blocks					1000	cycles
		Parameter Blocks					2500	cycles

1. T_A = –25 to 85°C; V_{DD} = 1.7V to 2V; V_{DDQ} = 2.7 to 3.6V.
2. Values are liable to change with the external system-level overhead (command sequence and Status Register polling execution).
3. Excludes the time needed to execute the command sequence.
4. This is an average value on the entire device.

10 Maximum Rating

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 17. Absolute Maximum Ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_A	Ambient Operating Temperature	–25	85	°C
T_{BIAS}	Temperature Under Bias	–25	85	°C
T_{STG}	Storage Temperature	–65	125	°C
V_{IO}	Input or Output Voltage	–0.5	4.2	V
V_{DD}	Supply Voltage	–0.2	2.5	V
V_{DDQ}	Input/Output Supply Voltage	–0.6	5	V
V_{PP}	Program Voltage	–0.2	10	V
I_O	Output Short Circuit Current		100	mA
t_{VPPH}	Time for V_{PP} at V_{PPH}		100	hours

11 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics Tables that follow, are derived from tests performed under the Measurement Conditions summarized in *Table 18: Operating and AC Measurement Conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 18. Operating and AC Measurement Conditions

Parameter	M58LT128GST, M58LT128GSB		Units
	110		
	Min	Max	
V_{DD} Supply Voltage	1.7	2.0	V
V_{DDQ} Supply Voltage	2.7	3.6	V
V_{PP} Supply Voltage (Factory environment)	8.5	9.5	V
V_{PP} Supply Voltage (Application environment)	–0.4	V_{DDQ}+0.4	V
Ambient Operating Temperature	–25	85	°C
Load Capacitance (C_L)	30		pF
Input Rise and Fall Times		5	ns
Input Pulse Voltages	0 to V_{DDQ}		V
Input and Output Timing Ref. Voltages	$V_{DDQ}/2$		V

Figure 7. AC Measurement I/O Waveform

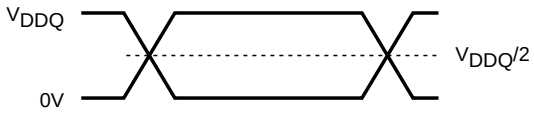


Figure 8. AC Measurement Load Circuit

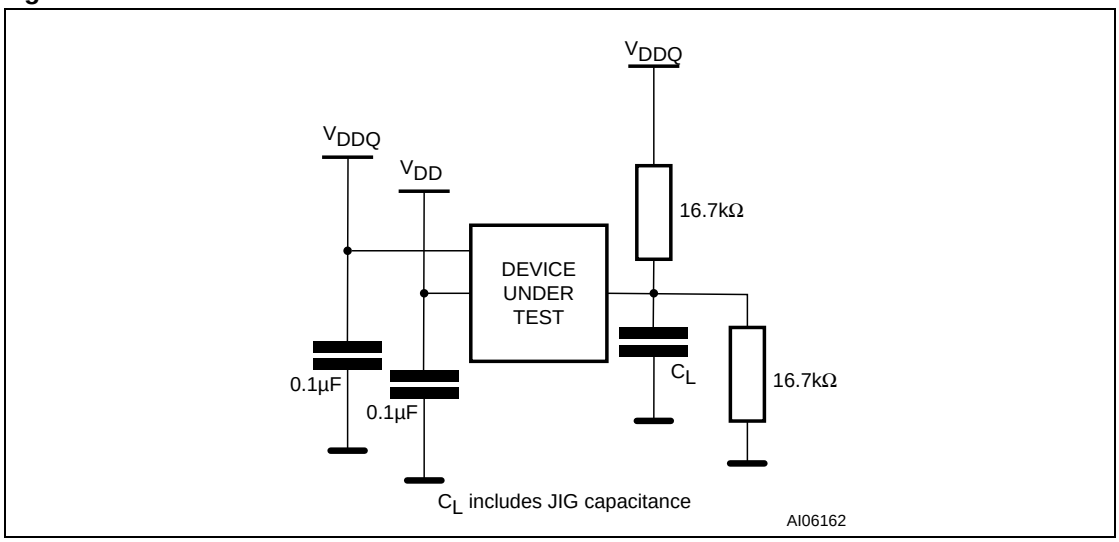


Table 19. Capacitance

Symbol	Parameter	Test Condition	Min(1)	Max(1)	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

1. Sampled only, not 100% tested.

Table 20. DC Characteristics - Currents

Symbol	Parameter	Test Condition	Typ	Max	Unit
I_{LI}	Input Leakage Current	$0V \le V_{IN} \le V_{DDQ}$		±1	µA
I_{LO}	Output Leakage Current	$0V \le V_{OUT} \le V_{DDQ}$		±1	µA
I_{DD1}	Supply Current Asynchronous Read (f=5MHz)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	13	15	mA
	Supply Current Synchronous Read (f=52MHz)	4 Word	16	18	mA
		8 Word	18	20	mA
		16 Word	23	25	mA
		Continuous	25	27	mA
I_{DD2}	Supply Current (Reset)	$\overline{RP} = V_{SS} \pm 0.2V$	25	70	µA
I_{DD3}	Supply Current (Standby)	$\overline{E} = V_{DD} \pm 0.2V$	25	70	µA
I_{DD4}	Supply Current (Automatic Standby)	$\overline{E} = V_{IL}$, $\overline{G} = V_{IH}$	25	70	µA
I_{DD5} (1)	Supply Current (Program)	$V_{PP} = V_{PPH}$	8	15	mA
		$V_{PP} = V_{DD}$	10	20	mA
	Supply Current (Erase)	$V_{PP} = V_{PPH}$	8	15	mA
		$V_{PP} = V_{DD}$	10	20	mA
I_{DD6} (1)(2)	Supply Current (Dual Operations)	Program/Erase in one Bank, Asynchronous Read in another Bank	23	35	mA
		Program/Erase in one Bank, Synchronous Read (Continuous f=52MHz) in another Bank	35	47	mA
I_{DD7}(1)	Supply Current Program/ Erase Suspended (Standby)	$\overline{E} = V_{DD} \pm 0.2V$	25	70	µA
I_{PP1}(1)	V_{PP} Supply Current (Program)	$V_{PP} = V_{PPH}$	2	5	mA
		$V_{PP} = V_{DD}$	0.2	5	µA
	V_{PP} Supply Current (Erase)	$V_{PP} = V_{PPH}$	2	5	mA
		$V_{PP} = V_{DD}$	0.2	5	µA
I_{PP2}	V_{PP} Supply Current (Read)	$V_{PP} \le V_{DD}$	0.2	5	µA
I_{PP3}(1)	V_{PP} Supply Current (Standby)	$V_{PP} \le V_{DD}$	0.2	5	µA

1. Sampled only, not 100% tested.
2. V_{DD} Dual Operation current is the sum of read and program or erase currents.

Table 21. DC Characteristics - Voltages

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		0		0.4	V
V_{IH}	Input High Voltage		V_{DDQ} –0.4		V_{DDQ} + 0.4	V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.1	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{DDQ} –0.1			V
V_{PP1}	V_{PP} Program Voltage-Logic	Program, Erase	1.1	1.8	3.3	V
V_{PPH}	V_{PP} Program Voltage Factory	Program, Erase	8.5	9.0	9.5	V
V_{PPLK}	Program or Erase Lockout				0.4	V
V_{LKO}	V_{DD} Lock Voltage		1			V
V_{RPH}	$\overline{RP}$ pin Extended High Voltage				3.3	V

Figure 9. Asynchronous Random Access Read AC Waveforms

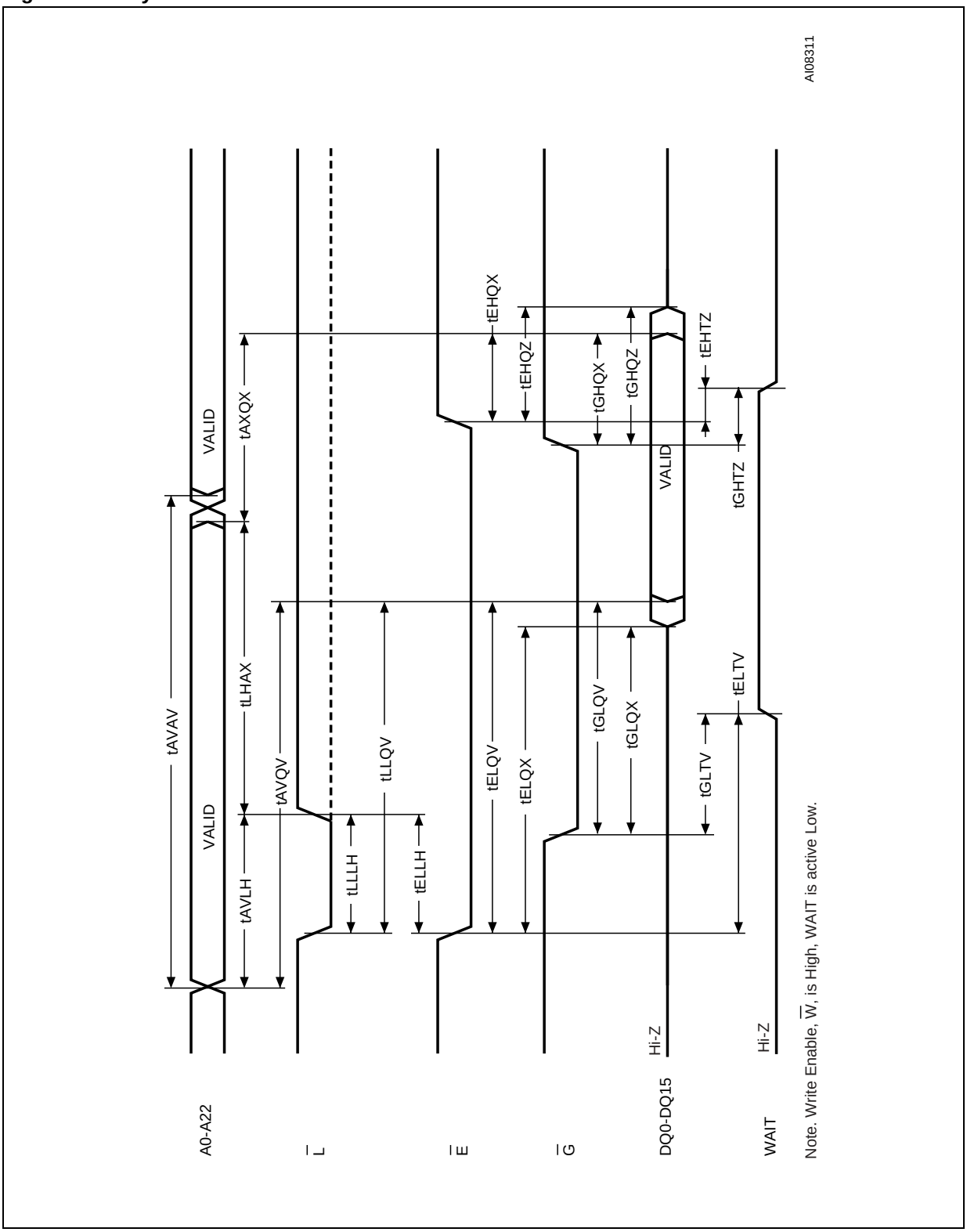


Figure 10. Asynchronous Page Read AC Waveforms

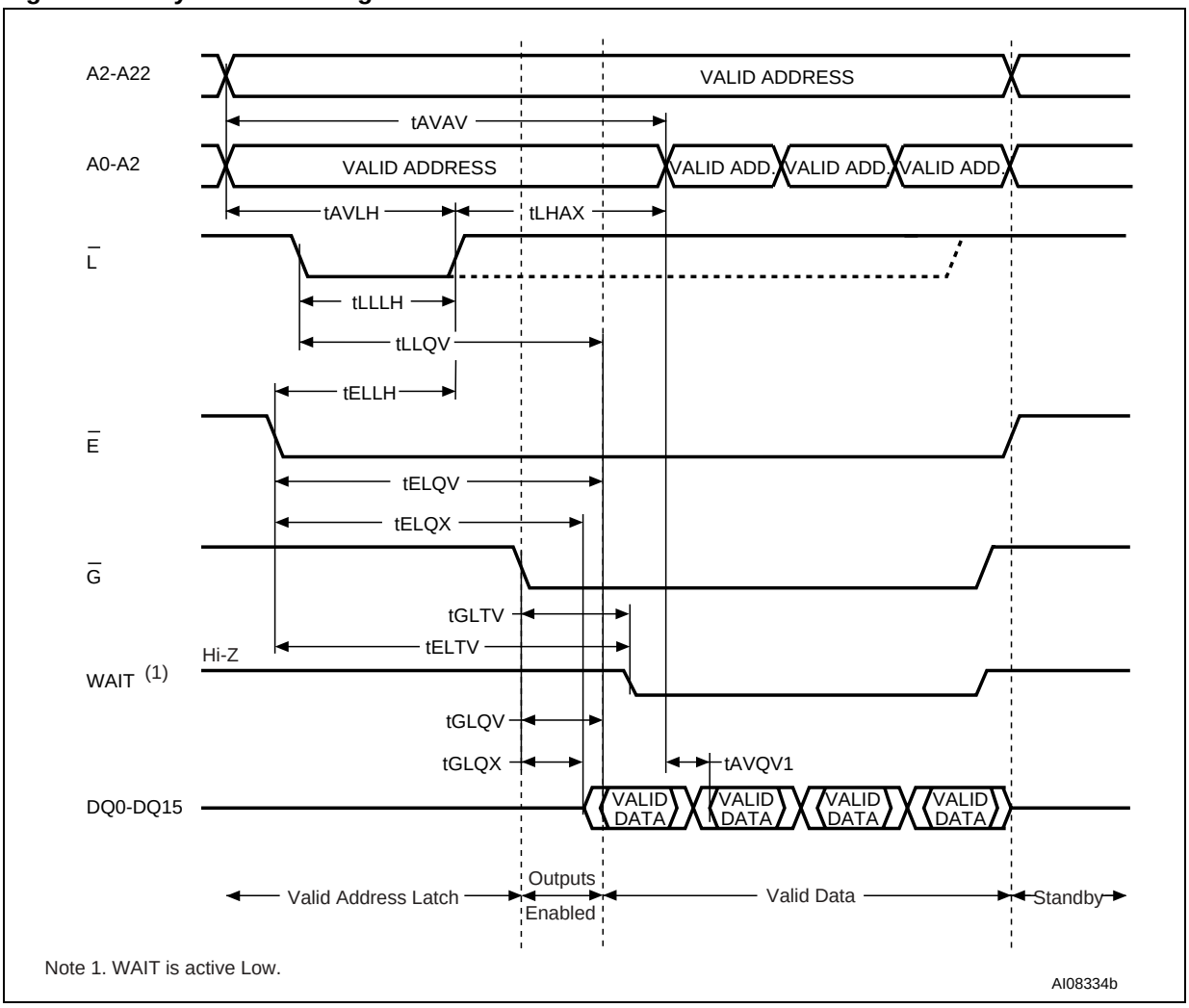
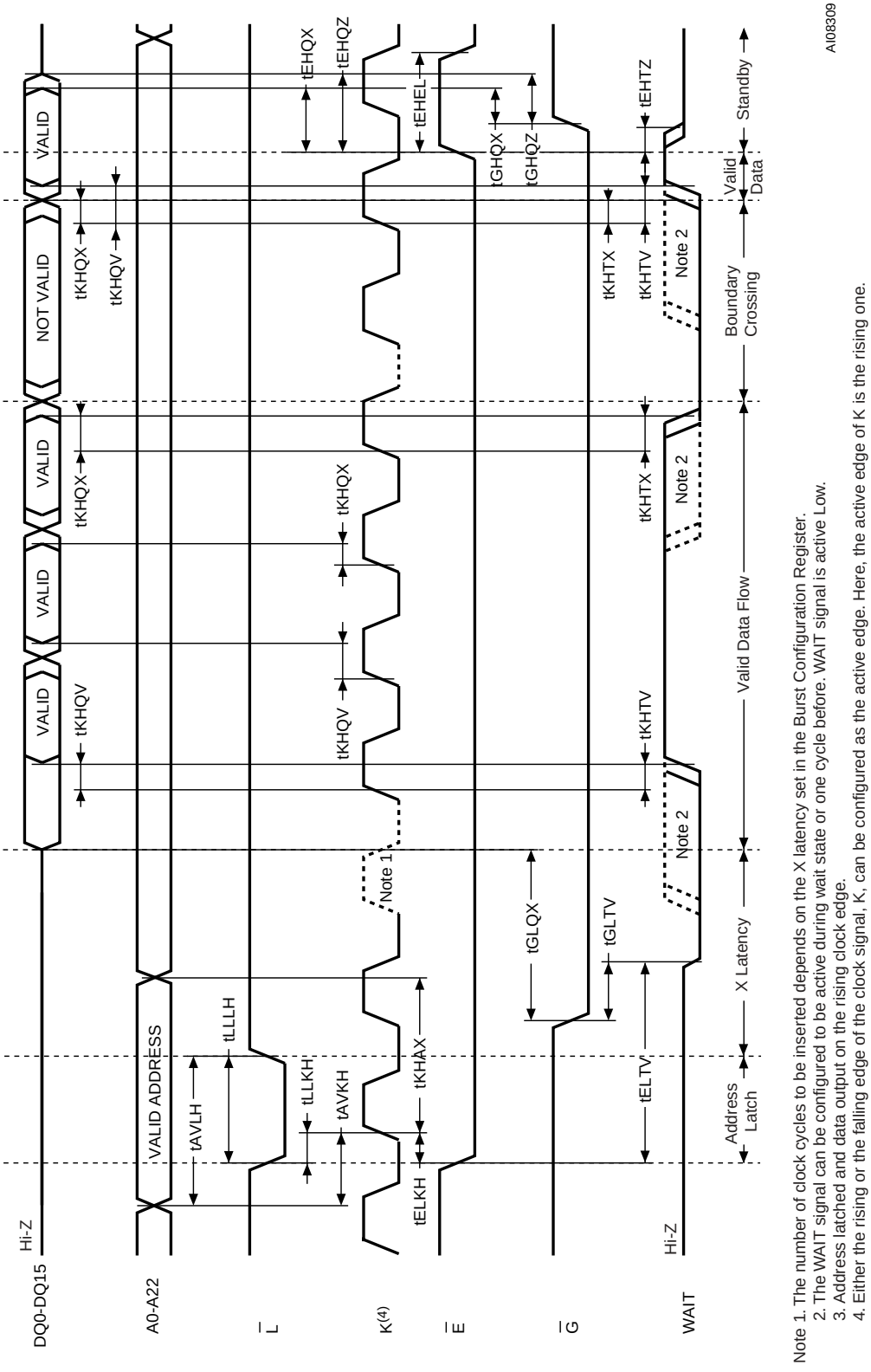


Table 22. Asynchronous Read AC Characteristics

Symbol		Alt	Parameter		M58LT128GST, M58LT128GSB	Unit
					110	
Read Timings	t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	Min	110	ns
	t_{AVQV}	t_{ACC}	Address Valid to Output Valid (Random)	Max	110	ns
	t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (Page)	Max	25	ns
	t_{AXQX}(1)	t_{OH}	Address Transition to Output Transition	Min	0	ns
	t_{ELTV}		Chip Enable Low to Wait Valid	Max	16	ns
	t_{ELQV}(2)	t_{CE}	Chip Enable Low to Output Valid	Max	110	ns
	t_{ELQX}(1)	t_{LZ}	Chip Enable Low to Output Transition	Max	0	ns
	t_{EHTZ}		Chip Enable High to Wait Hi-Z	Max	17	ns
	t_{EHQX}(1)	t_{OH}	Chip Enable High to Output Transition	Min	0	ns
	t_{EHQZ}(1)	t_{HZ}	Chip Enable High to Output Hi-Z	Max	17	ns
	t_{GLQV} (2)	t_{OE}	Output Enable Low to Output Valid	Max	30	ns
	t_{GLQX}(1)	t_{OLZ}	Output Enable Low to Output Transition	Min	0	ns
	t_{GLTV}		Output Enable Low to WAIT Valid	Max	17	ns
	t_{GHQX} (1)	t_{OH}	Output Enable High to Output Transition	Min	0	ns
	t_{GHQZ} (1)	t_{DF}	Output Enable High to Output Hi-Z	Max	17	ns
	t_{GHTZ}	t_{DF}	Output Enable High to WAIT Hi-Z	Max	17	ns
Latch Timings	t_{AVLH}	t_{AVADVH}	Address Valid to Latch Enable High	Min	11	ns
	t_{ELLH}	t_{ELADVH}	Chip Enable Low to Latch Enable High	Min	10	ns
	t_{LHAX}	t_{ADVHAX}	Latch Enable High to Address Transition	Min	9	ns
	t_{LLLH}	$t_{ADVLADVH}$	Latch Enable Pulse Width	Min	11	ns
	t_{LLQV}	t_{ADVLQV}	Latch Enable Low to Output Valid (Random)	Max	110	ns

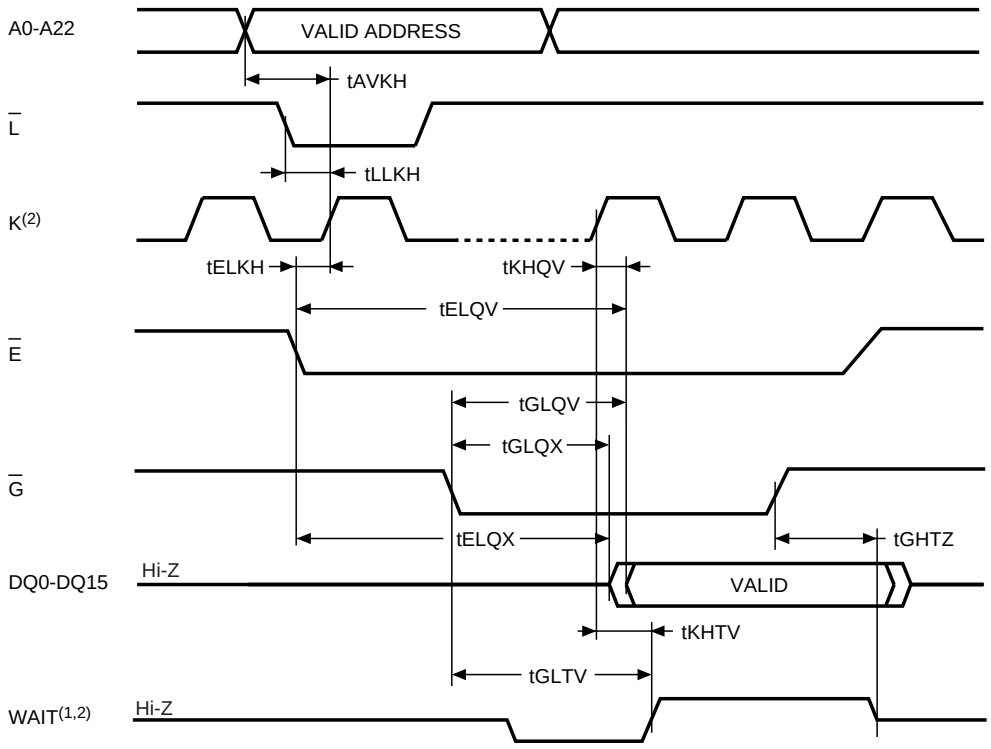
1. Sampled only, not 100% tested.
2. $\overline{G}$ may be delayed by up to t_{ELQV} - t_{GLQV} after the falling edge of $\overline{E}$ without increasing t_{ELQV}.

Figure 11. Synchronous Burst Read AC Waveforms



Note 1. The number of clock cycles to be inserted depends on the X latency set in the Burst Configuration Register.
2. The WAIT signal can be configured to be active during wait state or one cycle before. WAIT signal is active Low.
3. Address latched and data output on the rising clock edge.
4. Either the rising or the falling edge of the clock signal, K, can be configured as the active edge. Here, the active edge of K is the rising one.

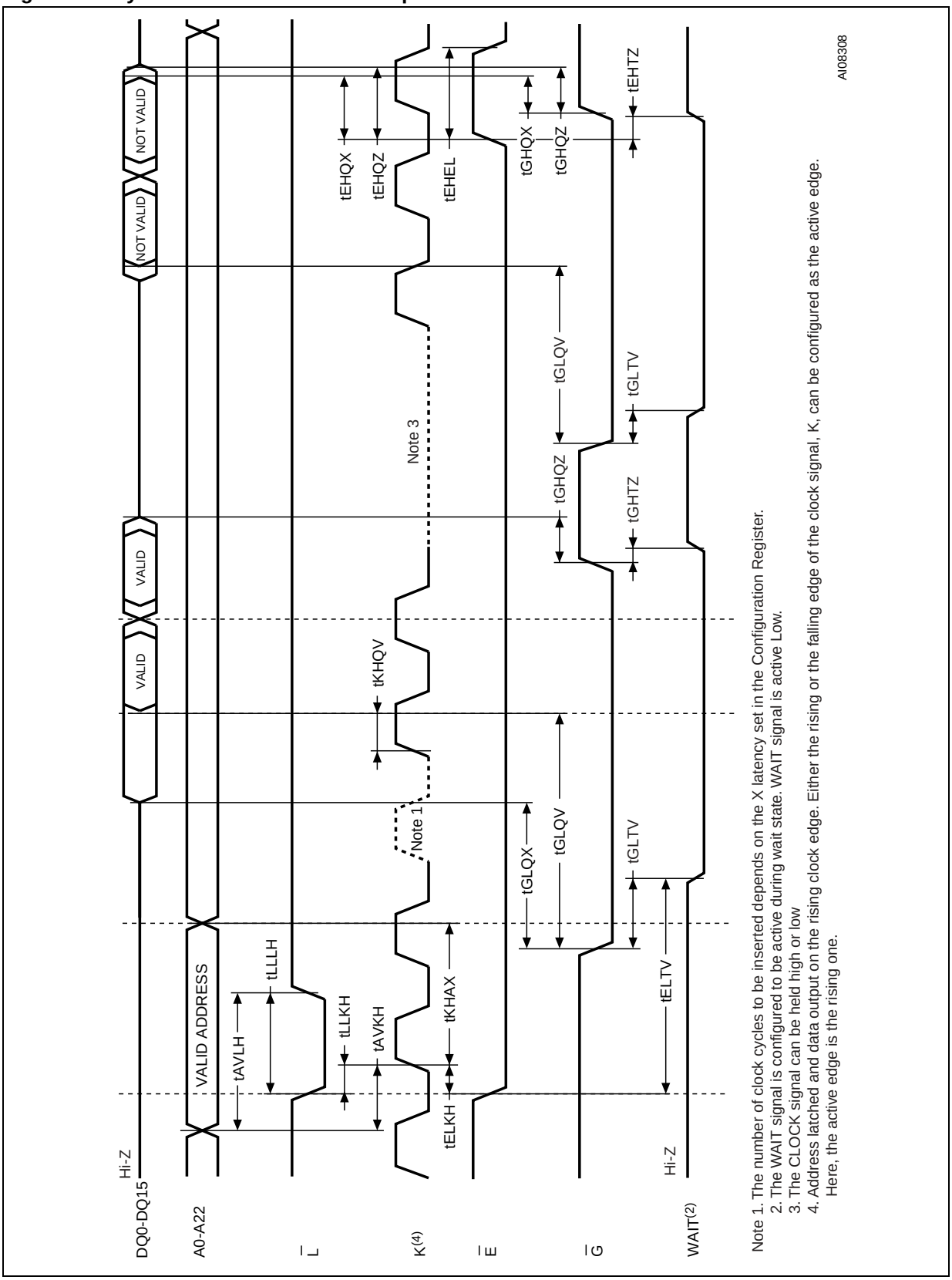
Figure 12. Single Synchronous Read AC Waveforms



Note 1. The WAIT signal is configured to be active during wait state. WAIT signal is active Low.
2. Address latched and data output on the rising clock edge. Either the rising or the falling edge of the clock signal, K, can be configured as the active edge. Here, the active edge is the rising one.

AI08312

Figure 13. Synchronous Burst Read Suspend AC Waveforms



Note 1. The number of clock cycles to be inserted depends on the X latency set in the Configuration Register.
2. The WAIT signal is configured to be active during wait state. WAIT signal is active Low.
3. The CLOCK signal can be held high or low
4. Address latched and data output on the rising clock edge. Either the rising or the falling edge of the clock signal, K, can be configured as the active edge. Here, the active edge is the rising one.

Figure 14. Clock input AC Waveform

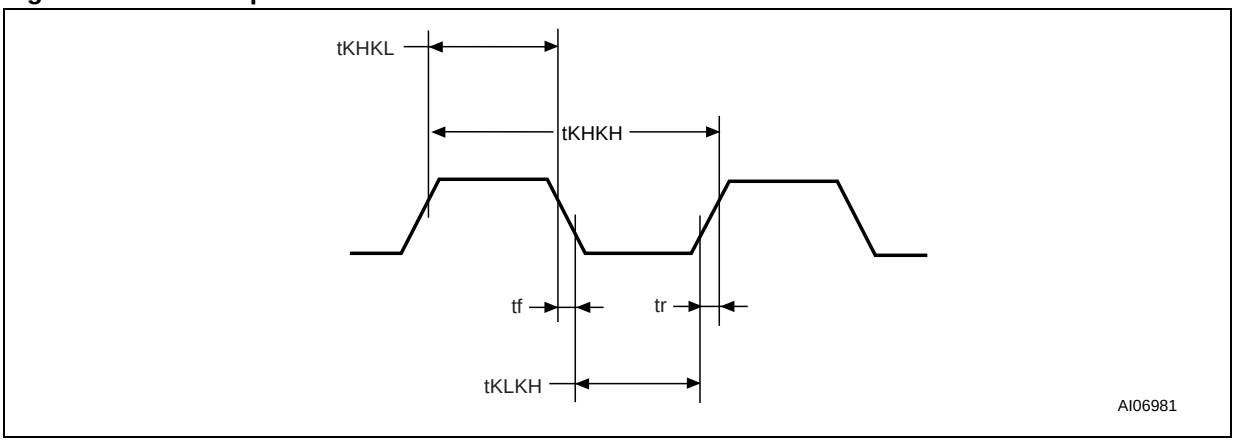


Table 23. Synchronous Read AC Characteristics

Symbol		Alt	Parameter[1]		M58LT128GST, M58LT128GSB	Unit
					110	
Synchronous Read Timings	t_{AVKH}	t_{AVCLKH}	Address Valid to Clock High	Min	11	ns
	t_{ELKH}	t_{ELCLKH}	Chip Enable Low to Clock High	Min	11	ns
	t_{ELTV}		Chip Enable Low to Wait Valid	Max	16	ns
	t_{EHEL}		Chip Enable Pulse Width (subsequent synchronous reads)	Min	17	ns
	t_{EHTZ}		Chip Enable High to Wait Hi-Z	Max	17	ns
	t_{GLTV}		Output Enable Low to Wait Valid	Max	17	ns
	t_{KHAX}	t_{CLKHAX}	Clock High to Address Transition	Min	10	ns
	t_{KHQV} t_{KHTV}	t_{CLKHQV}	Clock High to Output Valid Clock High to WAIT Valid	Max	17	ns
	t_{KHQX} t_{KHTX}	t_{CLKHQX}	Clock High to Output Transition Clock High to WAIT Transition	Min	3	ns
	t_{LLKH}	$t_{ADVLCLKH}$	Latch Enable Low to Clock High	Min	11	ns
	t_{GHTZ}	t_{DF}	Output Enable High to WAIT Hi-Z	Max	17	ns
Clock Specifications	t_{KHKH}	t_{CLK}	Clock Period (f=52MHz)	Min	19	ns
	t_{KHKL} t_{KLKH}		Clock High to Clock Low Clock Low to Clock High	Min	6	ns
	t_f, t_r		Clock Fall or Rise Time	Max	2	ns

1. Sampled only, not 100% tested.

For other timings please refer to *Table 22: Asynchronous Read AC Characteristics*.

Figure 15. Write AC Waveforms, Write Enable Controlled

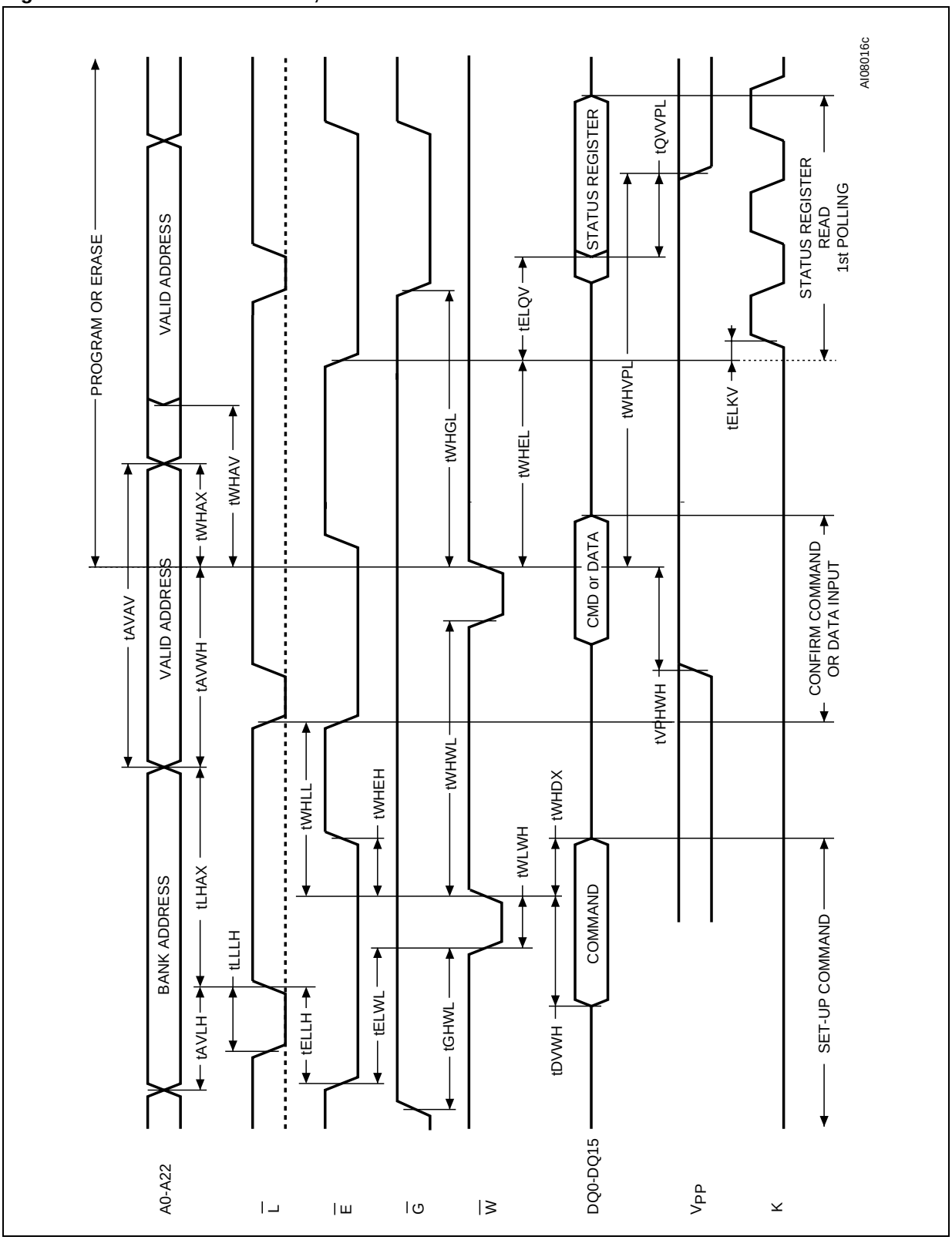


Table 24. Write AC Characteristics, Write Enable Controlled

Symbol		Alt	Parameter[1]		M58LT128GST, M58LT128GSB	Unit
					110	
Write Enable Controlled Timings	t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	110	ns
	t_{AVLH}		Address Valid to Latch Enable High	Min	11	ns
	t_{AVWH}[2]		Address Valid to Write Enable High	Min	50	ns
	t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Min	50	ns
	t_{ELLH}		Chip Enable Low to Latch Enable High	Min	11	ns
	t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	ns
	t_{ELQV}		Chip Enable Low to Output Valid	Min	110	ns
	t_{ELKV}		Chip Enable Low to Clock Valid	Min	9	ns
	t_{GHWL}		Output Enable High to Write Enable Low	Min	17	ns
	t_{LHAX}		Latch Enable High to Address Transition	Min	9	ns
	t_{LLLH}		Latch Enable Pulse Width	Min	11	ns
	t_{WHAV}[2]		Write Enable High to Address Valid	Min	0	ns
	t_{WHAX}[2]		Write Enable High to Address Transition	Min	0	ns
	t_{WHDX}	t_{DH}	Write Enable High to Input Transition	Min	0	ns
	t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	ns
	t_{WHEL}[3]		Write Enable High to Chip Enable Low	Min	25	ns
	t_{WHLL}		Write Enable High to Latch Enable Low	Min	0	ns
	t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	25	ns
	t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	50	ns
Protection Timings	t_{QVVPL}		Output (Status Register) Valid to V_{PP} Low	Min	0	ns
	t_{VPHWH}	t_{VPS}	V_{PP} High to Write Enable High	Min	200	ns
	t_{WHVPL}		Write Enable High to V_{PP} Low	Min	200	ns

1. Sampled only, not 100% tested.
2. These timings are meaningful only if Latch Enable, $\overline{L}$, is always kept Low, V_{IL}.
3. t_{WHEL} has the values shown when reading in the targeted bank. System designers should take this into account and may insert a software No-Op instruction to delay the first read in the same bank after issuing a command. If it is a Read Array operation in a different bank t_{WHEL} is 0ns.

Figure 16. Write AC Waveforms, Chip Enable Controlled

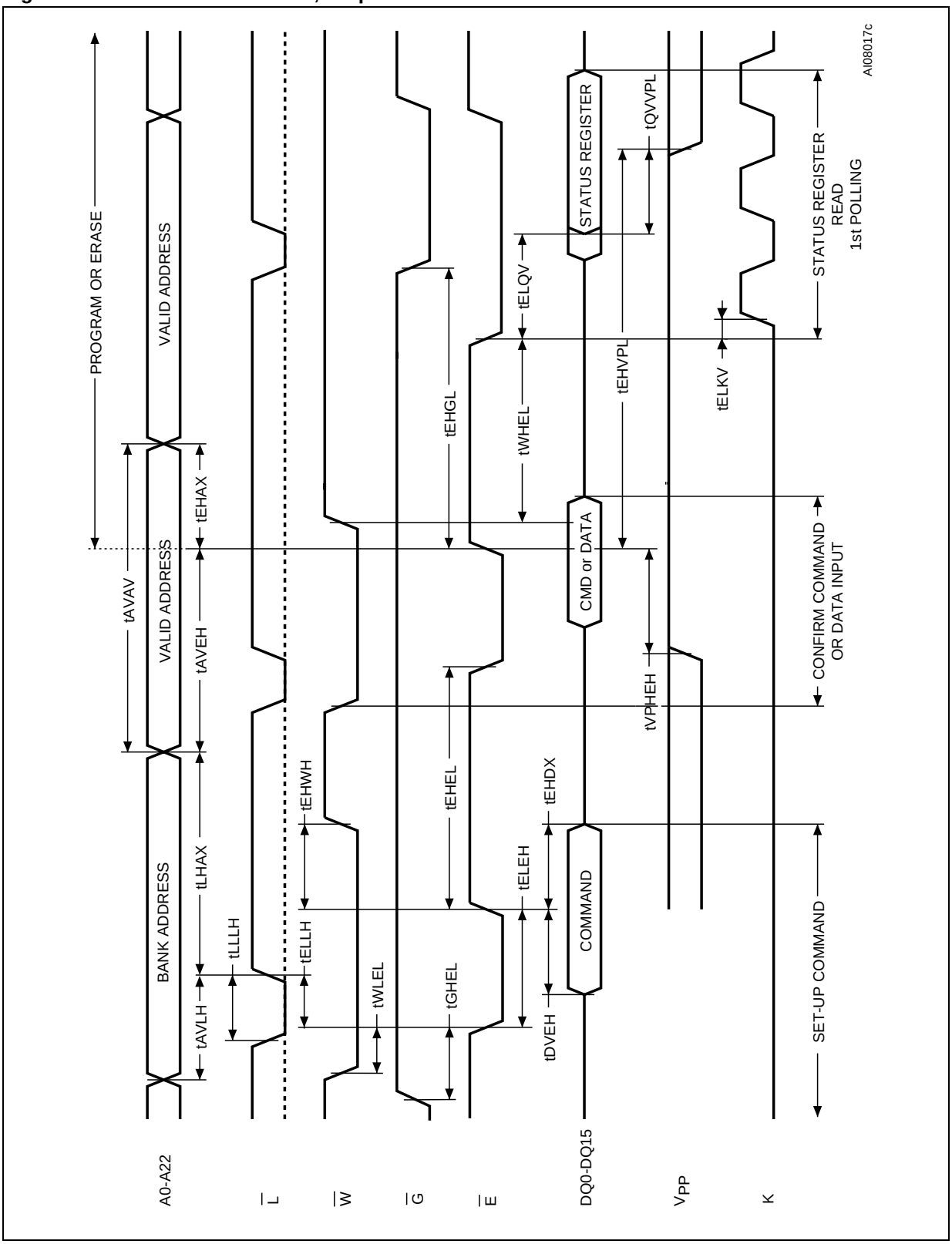


Table 25. Write AC Characteristics, Chip Enable Controlled

Symbol		Alt	Parameter[1]		M58LT128GST, M58LT128GSB	Unit
					110	
Chip Enable Controlled Timings	t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	110	ns
	t_{AVEH}		Address Valid to Chip Enable High	Min	50	ns
	t_{AVLH}		Address Valid to Latch Enable High	Min	11	ns
	t_{DVEH}	t_{DS}	Data Valid to Chip Enable High	Min	50	ns
	t_{EHAX}	t_{AH}	Chip Enable High to Address Transition	Min	0	ns
	t_{EHDX}	t_{DH}	Chip Enable High to Input Transition	Min	0	ns
	t_{EHEL}	t_{WPH}	Chip Enable High to Chip Enable Low	Min	25	ns
	t_{EHGL}		Chip Enable High to Output Enable Low	Min	0	ns
	t_{EHWH}	t_{CH}	Chip Enable High to Write Enable High	Min	0	ns
	t_{ELKV}		Chip Enable Low to Clock Valid	Min	7	ns
	t_{ELEH}	t_{WP}	Chip Enable Low to Chip Enable High	Min	50	ns
	t_{ELLH}		Chip Enable Low to Latch Enable High	Min	11	ns
	t_{ELQV}		Chip Enable Low to Output Valid	Min	110	ns
	t_{GHEL}		Output Enable High to Chip Enable Low	Min	17	ns
	t_{LHAX}		Latch Enable High to Address Transition	Min	9	ns
	t_{LLLH}		Latch Enable Pulse Width	Min	11	ns
	t_{WHEL}[2]		Write Enable High to Chip Enable Low	Min	25	ns
	t_{WLEL}	t_{CS}	Write Enable Low to Chip Enable Low	Min	0	ns
Protection Timings	t_{EHVPL}		Chip Enable High to V_{PP} Low	Min	200	ns
	t_{QVVPL}		Output (Status Register) Valid to V_{PP} Low	Min	0	ns
	t_{VPHEH}	t_{VPS}	V_{PP} High to Chip Enable High	Min	200	ns

1. Sampled only, not 100% tested.
2. t_{WHEL} has the values shown when reading in the targeted bank. System designers should take this into account and may insert a software No-Op instruction to delay the first read in the same bank after issuing a command. If it is a Read Array operation in a different bank t_{WHEL} is 0ns.

Figure 17. Reset and Power-up AC Waveforms

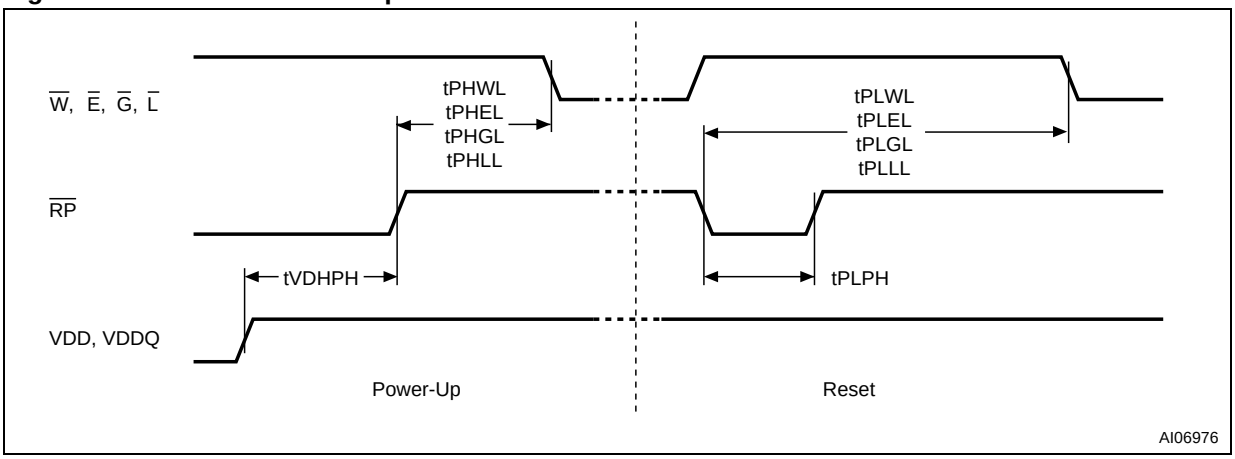


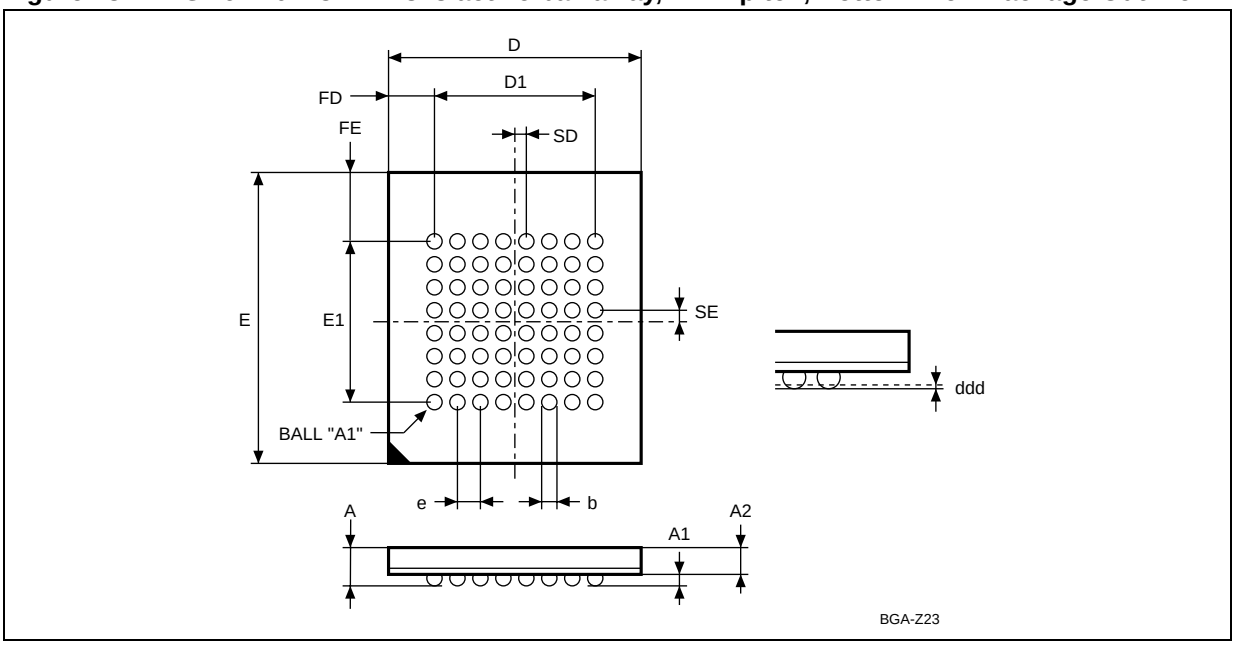
Table 26. Reset and Power-up AC Characteristics

Symbol	Parameter	Test Condition		110	Unit
t_{PLWL} t_{PLEL} t_{PLGL} t_{PLLL}	Reset Low to Write Enable Low, Chip Enable Low, Output Enable Low, Latch Enable Low	During Program	Min	25	µs
		During Erase	Min	25	µs
		Other Conditions	Min	110	ns
t_{PHWL} t_{PHEL} t_{PHGL} t_{PHLL}	Reset High to Write Enable Low Chip Enable Low Output Enable Low Latch Enable Low		Min	30	ns
t_{PLPH}(1)(2)	$\overline{RP}$ Pulse Width		Min	50	ns
t_{VDHPH}(3)	Supply Voltages High to Reset High		Min	100	µs

1. The device Reset is possible but not guaranteed if t_{PLPH} < 50ns.
2. Sampled only, not 100% tested.
3. It is important to assert $\overline{RP}$ in order to allow proper CPU initialization during Power-Up or Reset.

12 Package mechanical

Figure 18. TBGA64 10x13mm - 8x8 active ball array, 1mm pitch, Bottom View Package Outline



1. Drawing is not to scale.

Table 27. TBGA64 10x13mm - 8x8 active ball array, 1mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1	0.300	0.200	0.350	0.0118	0.0079	0.0138
A2	0.800			0.0315		
b		0.350	0.500		0.0138	0.0197
D	10.000	9.900	10.100	0.3937	0.3898	0.3976
D1	7.000	–	–	0.2756	–	–
ddd			0.100			0.0039
e	1.000	–	–	0.0394	–	–
E	13.000	12.900	13.100	0.5118	0.5079	0.5157
E1	7.000	–	–	0.2756	–	–
FD	1.500	–	–	0.0591	–	–
FE	3.000	–	–	0.1181	–	–
SD	0.500	–	–	0.0197	–	–
SE	0.500	–	–	0.0197	–	–

13 Part Numbering

Table 28. Ordering Information Scheme

Example: M58LT128GS T 1 ZA 5 E

Device Type
M58

Architecture
L = Multilevel, Multiple Bank, Burst Mode

Operating Voltage
T = V_{DD} = 1.7V to 2.0V, V_{DDQ} =2.7V to 3.6V

Density
128 = 128 Mbit (x16)

Technology
G = 0.13µm

Security
S = Security

Parameter Location
T = Top Boot
B = Bottom Boot

Speed
1 = 110ns

Package
ZA = TBGA64, 10 x 13mm, 1mm pitch

Temperature Range
5 = –25 to 85°C

Packing Option
Blank = Standard Packing
E = ECOPACK Package, Standard Packing
F =ECOPACK Package, 24mm Tape & Reel Packing

Table 29. Daisy Chain Ordering Scheme

Example: M58LT128GS -ZA E

Device Type
M58LT128GS

Daisy Chain
ZA = TBGA64, 10 x 13mm, 1mm pitch

Option
Blank = Standard Packing
E = ECOPACK Package, Standard Packing

Devices are shipped from the factory with the memory content bits erased to ’1’.

For a list of available options (Speed, Package, etc.) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Appendix A Block address tables

The following set of equations can be used to calculate a complete set of block addresses for the M58LT128GST and M58LT128GSB using the information contained in *Table 30* to *Table 35*.

To calculate the Block Base Address from the Block Number:

First it is necessary to calculate the Bank Number and the Block Number Offset. This can be achieved using the following formulas:

```
Bank_Number = (Block_Number – 3) / 16
Block_Number_Offset = Block_Number – 3 – (Bank_Number x 16)
```

If Bank_Number = 0, the Block Base Address can be directly read from *Table 30* and *Table 33* (Parameter Bank Block Addresses) in the Address Range column, in the row that corresponds to the given block number.

Otherwise:

```
Block_Base_Address = Bank_Base_Address + Block_Base_Address_Offset
```

To calculate the Bank Number and the Block Number from the Block Base Address:

If the address is in the range of the Parameter Bank, the Bank Number is 0 and the Block Number can be directly read from *Table 30* for the M58LT128GST and *Table 33* for the M58LT128GSB (Parameter Bank Block Addresses), in the Block Number column, in the row that corresponds to the address given. Otherwise, the Block Number can be calculated using the formulas below:

For the top configuration (M58LT128GST):

$$Block\_Number = ((NOT\ address) / 2^{16}) + 3$$

For the bottom configuration (M58LT128GSB):

$$Block\_Number = (address / 2^{16}) + 3$$

For both configurations the Bank Number and the Block Number Offset can be calculated using the following formulas:

```
Bank_Number = (Block_Number – 3) / 16
Block_Number_Offset = Block_Number –3 – (Bank_Number x 16)
```

Table 30. M58LT128GST - Parameter Bank Block Addresses

Block Number	Size (KWords)	Address Range
0	16	7FC000-7FFFFF
1	16	7F8000-7FBFFF
2	16	7F4000-7F7FFF
3	16	7F0000-7F3FFF
4	64	7E0000-7EFFFF
5	64	7D0000-7DFFFF
6	64	7C0000-7CFFFF
7	64	7B0000-7BFFFF
8	64	7A0000-7AFFFF
9	64	790000-79FFFF
10	64	780000-78FFFF

Table 31. M58LT128GST - Main Bank Base Addresses

Bank Number	Block Numbers	Bank Base Address
1	11-18	700000
2	19-26	680000
3	27-34	600000
4	35-42	580000
5	43-50	500000
6	51-58	480000
7	59-66	400000
8	67-74	380000
9	75-82	300000
10	83-90	280000
11	91-98	200000
12	99-106	180000
13	107-114	100000
14	115-122	080000
15	123-130	000000

1. There are two Bank Regions: Bank Region 1 contains all the banks that are made up of main blocks only; Bank Region 2 contains the banks that are made up of the parameter and main blocks (Parameter Bank).

Table 32. M58LT128GST - Block Addresses in Main Banks

Block Number Offset	Block Base Address Offset
0	070000
1	060000
2	050000
3	040000
4	030000
5	020000
6	010000
7	000000

Table 33. M58LT128GSB - Parameter Bank Block Addresses

Block Number	Size (KWords)	Address Range
10	64	070000-07FFFF
9	64	060000-06FFFF
8	64	050000-05FFFF
7	64	040000-04FFFF
6	64	030000-03FFFF
5	64	020000-02FFFF
4	64	010000-01FFFF
3	16	00C000-00FFFF
2	16	008000-00BFFF
1	16	004000-007FFF
0	16	000000-003FFF

Table 34. M58LT128GSB- Main Bank Base Addresses

Bank Number	Block Numbers	Bank Base Address
15	123-130	780000
14	115-122	700000
13	107-114	680000
12	99-106	600000
11	91-98	580000
10	83-90	500000
9	75-82	480000
8	67-74	400000
7	59-66	380000
6	51-58	300000
5	43-50	280000
4	35-42	200000
3	27-34	180000
2	19-26	100000
1	11-18	080000

1. There are two Bank Regions: Bank Region 2 contains all the banks that are made up of main blocks only; Bank Region 1 contains the banks that are made up of the parameter and main blocks (Parameter Bank).

Table 35. M58LT128GSB - Block Addresses in Main Banks

Block Number Offset	Block Base Address Offset
7	070000
6	060000
5	050000
4	040000
3	030000
2	020000
1	010000
0	000000

Appendix B Common Flash Interface

The Common Flash Interface is a JEDEC approved, standardized data structure that can be read from the Flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query Command is issued the device enters CFI Query mode and the data structure is read from the memory. *Table 36*, *Table 37*, *Table 38*, *Table 39*, *Table 40*, *Table 42*, *Table 43*, *Table 44* and *Table 45* show the addresses used to retrieve the data. The Query data is always presented on the lowest order data outputs (DQ0-DQ7), the other outputs (DQ8-DQ15) are set to 0.

The CFI data structure also contains a security area where a 64 bit unique security number is written (see *Figure 4: Protection Register Map*).This area can be accessed only in Read mode by the final user. It is impossible to change the security number after it has been written by ST. Issue a Read Array command to return to Read mode.

Table 36. Query Structure Overview

Offset	Sub-section Name	Description
000h	Reserved	Reserved for algorithm-specific information
010h	CFI Query Identification String	Command set ID and algorithm data offset
01Bh	System Interface Information	Device timing & voltage information
027h	Device Geometry Definition	Flash device layout
P	Primary Algorithm-specific Extended Query table	Additional information specific to the Primary Algorithm (optional)
A	Alternate Algorithm-specific Extended Query table	Additional information specific to the Alternate Algorithm (optional)
080h	Security Code Area	Lock Protection Register Unique device Number and User Programmable OTP

1. The Flash memory display the CFI data structure when CFI Query command is issued. In this table are listed the main sub-sections detailed in *Table 37*, *Table 38*, *Table 39* and *Table 40*. Query data is always presented on the lowest order data outputs.

Table 37. CFI Query Identification String

Offset	Sub-section Name	Description		Value
000h	0020h	Manufacturer Code		ST
001h	88C6h 88C7h	Device Code	M58LT128GST M58LT128GSB	Top Bottom
002h	reserved	Reserved		
003h	DRC	Die Revision Code		
004h-00Fh	reserved	Reserved		
010h	0051h	Query Unique ASCII String "QRY"		"Q"
011h	0052h			"R"
012h	0059h			"Y"
013h	0001h	Primary Algorithm Command Set and Control Interface ID code 16 bit ID code defining a specific algorithm		
014h	0000h			
015h	offset = P = 000Ah	Address for Primary Algorithm extended Query table (see *Table 40*)		p = 10Ah
016h	0001h			
017h	0000h	Alternate Vendor Command Set and Control Interface ID Code second vendor - specified algorithm supported		NA
018h	0000h			
019h	value = A = 0000h	Address for Alternate Algorithm extended Query table		NA
01Ah	0000h			

Table 38. CFI Query System Interface Information

Offset	Data	Description	Value
01Bh	0017h	V_{DD} Logic Supply Minimum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts	1.7V
01Ch	0020h	V_{DD} Logic Supply Maximum Program/Erase or Write voltage bit 7 to 4 BCD value in volts bit 3 to 0 BCD value in 100 millivolts	2V
01Dh	0085h	V_{PP} [Programming] Supply Minimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts	8.5V
01Eh	0095h	V_{PP} [Programming] Supply Maximum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 millivolts	9.5V
01Fh	0008h	Typical time-out per single byte/word program = 2^n µs	256µs
020h	0009h	Typical time-out for Buffer Program = 2^n µs	512µs
021h	000Ah	Typical time-out per individual block erase = 2^n ms	1s
022h	0000h	Typical time-out for full chip erase = 2^n ms	NA

Offset	Data	Description	Value
023h	0001h	Maximum time-out for word program = 2^n times typical	512µs
024h	0001h	Maximum time-out for Buffer Program = 2^n times typical	1024µs
025h	0002h	Maximum time-out per individual block erase = 2^n times typical	4s
026h	0000h	Maximum time-out for chip erase = 2^n times typical	NA

Table 39. Device Geometry Definition

Offset		Data	Description	Value
027h		0018h	Device Size = 2^n in number of bytes	16 MBytes
028h 029h		0001h 0000h	Flash Device Interface Code description	x16 Async.
02Ah 02Bh		0006h 0000h	Maximum number of bytes in multi-byte program or page = 2^n	64 Bytes
02Ch		0002h	Number of identical sized erase block regions within the device bit 7 to 0 = x = number of Erase Block Regions	2
TOP DEVICES	02Dh 02Eh	007Eh 0000h	Erase Block Region 1 Information Number of identical-size erase blocks = 007Eh+1	127
	02Fh 030h	0000h 0002h	Erase Block Region 1 Information Block size in Region 1 = 0200h * 256 Byte	128 KByte
	031h 032h	0003h 0000h	Erase Block Region 2 Information Number of identical-size erase blocks = 0003h+1	4
	033h 034h	0080h 0000h	Erase Block Region 2 Information Block size in Region 2 = 0080h * 256 Byte	32 KByte
	035h 038h	Reserved	Reserved for future erase block region information	NA
BOTTOM DEVICES	02Dh 02Eh	0003h 0000h	Erase Block Region 1 Information Number of identical-size erase block = 0003h+1	4
	02Fh 030h	0080h 0000h	Erase Block Region 1 Information Block size in Region 1 = 0080h * 256 bytes	32 KBytes
	031h 032h	007Eh 0000h	Erase Block Region 2 Information Number of identical-size erase block = 007Eh+1	127
	033h 034h	0000h 0002h	Erase Block Region 2 Information Block size in Region 2 = 0200h * 256 bytes	128 KBytes
	035h 038h	Reserved	Reserved for future erase block region information	NA

Table 40. Primary Algorithm-Specific Extended Query Table

Offset	Data	Description	Value
(P)h = 10Ah	0050h	Primary Algorithm extended Query table unique ASCII string “PRI”	"P"
	0052h		"R"
	0049h		"I"
(P+3)h =10Dh	0031h	Major version number, ASCII	"1"
(P+4)h = 10Eh	0033h	Minor version number, ASCII	"3"
(P+5)h = 10Fh	00E6h	Extended Query table contents for Primary Algorithm. Address (P+5)h contains less significant byte. bit 0 Chip Erase supported(1 = Yes, 0 = No) bit 1 Erase Suspend supported(1 = Yes, 0 = No) bit 2 Program Suspend supported(1 = Yes, 0 = No) bit 3 Reserved bit 5 Instant individual block locking supported(1 = Yes, 0 = No) bit 6 Protection bits supported(1 = Yes, 0 = No) bit 7 Page mode read supported(1 = Yes, 0 = No) bit 8 Synchronous read supported(1 = Yes, 0 = No) bit 9 Simultaneous operation supported(1 = Yes, 0 = No) bit 10 to 31 Reserved; undefined bits are ‘0’. If bit 31 is ’1’ then another 31 bit field of optional features follows at the end of the bit-30 field.	 No Yes Yes No No Yes Yes Yes Yes Yes
	0003h		
(P+7)h = 111h	0000h		
(P+8)h = 112h	0000h		
(P+9)h = 113h	0001h	Supported Functions after Suspend Read Array, Read Status Register and CFI Query bit 0 Program supported after Erase Suspend (1 = Yes, 0 = No) bit 7 to 1 Reserved; undefined bits are ‘0’	Yes
(P+A)h = 114h	0003h	Reserved	
(P+B)h = 115h	0000h		
(P+C)h = 116h	0018h	V_{DD} Logic Supply Optimum Program/Erase voltage (highest performance) bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	1.8V
(P+D)h = 117h	0090h	V_{PP} Supply Optimum Program/Erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	9V

Table 41. Protection Register Information

Offset	Data	Description	Value
(P+E)h = 118h	0002h	Number of protection register fields in JEDEC ID space. 0000h indicates that 256 fields are available.	2
(P+F)h = 119h	0080h	Protection Field 1: Protection Description	80h
(P+10)h = 11Ah	0000h	Bits 0-7 Lower byte of protection register address	00h
(P+11)h = 11Bh	0003h	Bits 8-15 Upper byte of protection register address Bits 16-23 2^n bytes in factory pre-programmed region	8 Bytes
(P+12)h = 11Ch	0003h	Bits 24-31 2^n bytes in user programmable region	8 Bytes
(P+13)h = 11Dh	0089h		89h
(P+14)h = 11Eh	0000h		00h
(P+15)h = 11Fh	0000h	Protection Register 2: Protection Description	00h
(P+16)h = 120h	0000h	Bits 0-31 protection register address Bits 32-39 n number of factory programmed regions (lower byte)	00h
(P+17)h = 121h	0000h	Bits 40-47 n number of factory programmed regions (upper byte)	0
(P+18)h = 122h	0000h	Bits 48-55 2^n bytes in factory programmable region	0
(P+19)h = 123h	0000h	Bits 56-63 n number of user programmable regions (lower byte)	0
(P+1A)h = 124h	0010h	Bits 64-71 n number of user programmable regions (upper byte) Bits 72-79 2^n bytes in user programmable region	16
(P+1B)h = 125h	0000h		0
(P+1C)h = 126h	0004h		16

Table 42. Burst Read Information

Offset	Data	Description	Value
(P+1D)h = 127h	0004h	Page-mode read capability bits 0-7 n' such that 2^n HEX value represents the number of read-page bytes. See offset 0028h for device word width to determine page-mode data output width.	16 Bytes
(P+1E)h = 128h	0004h	Number of synchronous mode read configuration fields that follow.	4
(P+1F)h = 129h	0001h	Synchronous mode read capability configuration 1 bit 3-7 Reserved bit 0-2 n' such that 2^{n+1} HEX value represents the maximum number of continuous synchronous reads when the device is configured for its maximum word width. A value of 07h indicates that the device is capable of continuous linear bursts that will output data until the internal burst counter reaches the end of the device's burstable address space. This field's 3-bit value can be written directly to the read configuration register bit 0-2 if the device is configured for its maximum word width. See offset 0028h for word width to determine the burst data output width.	4
(P+20)h = 12Ah	0002h	Synchronous mode read capability configuration 2	8
(P-21)h = 12Bh	0003h	Synchronous mode read capability configuration 3	16
(P+22)h = 12Ch	0007h	Synchronous mode read capability configuration 4	Cont.

Table 43. Bank and Erase Block Region Information

Flash memory (top)		Flash memory (bottom)		Description
Offset	Data	Offset	Data	
(P+23)h = 12Dh	02h	(P+23)h = 12Dh	02h	Number of Bank Regions within the device

1. The variable P is a pointer which is defined at CFI offset 015h.
2. Bank Regions. There are two Bank Regions, see *Table 30* to *Table 35*.

Table 44. Bank and Erase Block Region 1 Information

Flash memory (top)		Flash memory (bottom)		Description
Offset	Data	Offset	Data	
(P+24)h = 12Eh	0Fh	(P+24)h = 12Eh	01h	Number of identical banks within Bank Region 1
(P+25)h = 12Fh	00h	(P+25)h = 12Fh	00h	
(P+26)h = 130h	11h	(P+26)h = 130h	11h	Number of program or erase operations allowed in Bank Region 1: Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+27)h = 131h	00h	(P+27)h = 131h	00h	Number of program or erase operations allowed in other banks while a bank in same region is programming Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+28)h = 132h	00h	(P+28)h = 132h	00h	Number of program or erase operations allowed in other banks while a bank in this region is erasing Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+29)h = 133h	01h	(P+29)h = 133h	02h	Types of erase block regions in Bank Region 1 n = number of erase block regions with contiguous same-size erase blocks. Symmetrically blocked banks have one blocking region(2).
(P+2A)h = 134h	07h	(P+2A)h = 134h	03h	Bank Region 1 Erase Block Type 1 Information Bits 0-15: n+1 = number of identical-sized erase blocks Bits 16-31: n×256 = number of bytes in erase block region
(P+2B)h = 135h	00h	(P+2B)h = 135h	00h	
(P+2C)h = 136h	00h	(P+2C)h = 136h	80h	
(P+2D)h = 137h	02h	(P+2D)h = 137h	00h	
(P+2E)h = 138h	64h	(P+2E)h = 138h	64h	Bank Region 1 (Erase Block Type 1) Minimum block erase cycles × 1000
(P+2F)h = 139h	00h	(P+2F)h = 139h	00h	
(P+30)h = 13Ah	02h	(P+30)h = 13Ah	02h	Bank Region 1 (Erase Block Type 1): BIts per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for “internal ECC used” BIts 5-7: reserved
(P+31)h = 13Bh	03h	(P+31)h = 13Bh	03h	Bank Region 1 (Erase Block Type 1): Page mode and Synchronous mode capabilities Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved

Flash memory (top)		Flash memory (bottom)		Description
Offset	Data	Offset	Data	
		(P+32)h = 13Ch	06h	Bank Region 1 Erase Block Type 2 Information Bits 0-15: n+1 = number of identical-sized erase blocks Bits 16-31: n×256 = number of bytes in erase block region
		(P+33)h = 13Dh	00h	
		(P+34)h = 13Eh	00h	
		(P+35)h = 13Fh	02h	
		(P+36)h = 140h	64h	Bank Region 1 (Erase Block Type 2) Minimum block erase cycles × 1000
		(P+37)h = 141h	00h	
		(P+38)h = 142h	02h	Bank Regions 1 (Erase Block Type 2): BIts per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for “internal ECC used” BIts 5-7: reserved
		(P+39)h = 143h	03h	Bank Region 1 (Erase Block Type 2): Page mode and Synchronous mode capabilities Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved

1. The variable P is a pointer which is defined at CFI offset 015h.
2. Bank Regions. There are two Bank Regions, see *Table 30* to *Table 35*.

Table 45. Bank and Erase Block Region 2 Information

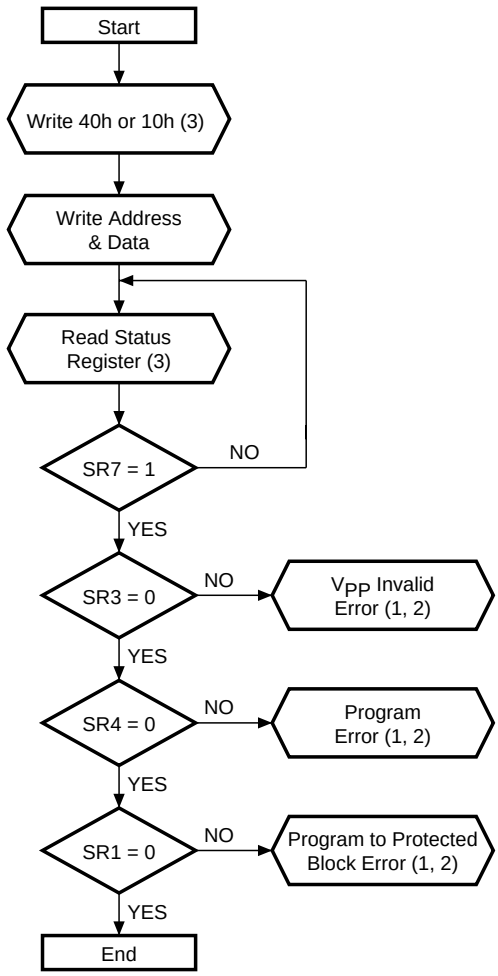
Flash memory (top)		Flash memory (bottom)		Description
Offset	Data	Offset	Data	
(P+32)h = 13Ch	01h	(P+3A)h = 144h	0Fh	Number of identical banks within Bank Region 2
(P+33)h = 13Dh	00h	(P+3B)h = 145h	00h	
(P+34)h = 13Eh	11h	(P+3C)h = 146h	11h	Number of program or erase operations allowed in Bank Region 2: Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+35)h = 13Fh	00h	(P+3D)h = 147h	00h	Number of program or erase operations allowed in other banks while a bank in this region is programming Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+36)h = 140h	00h	(P+3E)h = 148h	00h	Number of program or erase operations allowed in other banks while a bank in this region is erasing Bits 0-3: Number of simultaneous program operations Bits 4-7: Number of simultaneous erase operations
(P+37)h = 141h	02h	(P+3F)h = 149h	01h	Types of erase block regions in Bank Region 2 n = number of erase block regions with contiguous same-size erase blocks. Symmetrically blocked banks have one blocking region.(2)
(P+38)h = 142h	06h	(P+40)h = 14Ah	07h	Bank Region 2 Erase Block Type 1 Information Bits 0-15: n+1 = number of identical-sized erase blocks Bits 16-31: n×256 = number of bytes in erase block region
(P+39)h = 143h	00h	(P+41)h = 14Bh	00h	
(P+3A)h = 144h	00h	(P+42)h = 14Ch	00h	
(P+3B)h = 145h	02h	(P+43)h = 14Dh	02h	
(P+3C)h = 146h	64h	(P+44)h = 14Eh	64h	Bank Region 2 (Erase Block Type 1) Minimum block erase cycles × 1000
(P+3D)h = 147h	00h	(P+45)h = 14Fh	00h	
(P+3E)h = 148h	02h	(P+46)h = 150h	02h	Bank Region 2 (Erase Block Type 1): BIts per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for “internal ECC used” BIts 5-7: reserved
(P+3F)h = 149h	03h	(P+47)h = 151h	03h	Bank Region 2 (Erase Block Type 1):Page mode and Synchronous mode capabilities (defined in *Table 42*) Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved
(P+40)h = 14Ah	03h			Bank Region 2 Erase Block Type 2 Information Bits 0-15: n+1 = number of identical-sized erase blocks Bits 16-31: n×256 = number of bytes in erase block region
(P+41)h = 14Bh	00h			
(P+42)h = 14Ch	80h			
(P+43)h = 14Dh	00h			

Flash memory (top)		Flash memory (bottom)		Description
Offset	Data	Offset	Data	
(P+44)h = 14Eh	64h			Bank Region 2 (Erase Block Type 2) Minimum block erase cycles × 1000
(P+45)h = 14Fh	00h			
(P+46)h = 150h	02h			Bank Region 2 (Erase Block Type 2): BIts per cell, internal ECC Bits 0-3: bits per cell in erase region Bit 4: reserved for “internal ECC used” BIts 5-7: reserved
(P+47)h = 151h	03h			Bank Region 2 (Erase Block Type 2): Page mode and Synchronous mode capabilities (defined in *Table 42*) Bit 0: Page-mode reads permitted Bit 1: Synchronous reads permitted Bit 2: Synchronous writes permitted Bits 3-7: reserved
(P+48)h = 152h		(P+48)h = 152h		Feature Space definitions
(P+49)h = 153h		(P+43)h = 153h		Reserved

1. The variable P is a pointer which is defined at CFI offset 015h.
2. Bank Regions. There are two Bank Regions, see *Table 30* to *Table 32* for the M58LT128GST and *Table 33* to *Table 35* for the M58LT128GSB.

Appendix C Flowcharts and Pseudo Codes

Figure 19. Program Flowchart and Pseudo Code

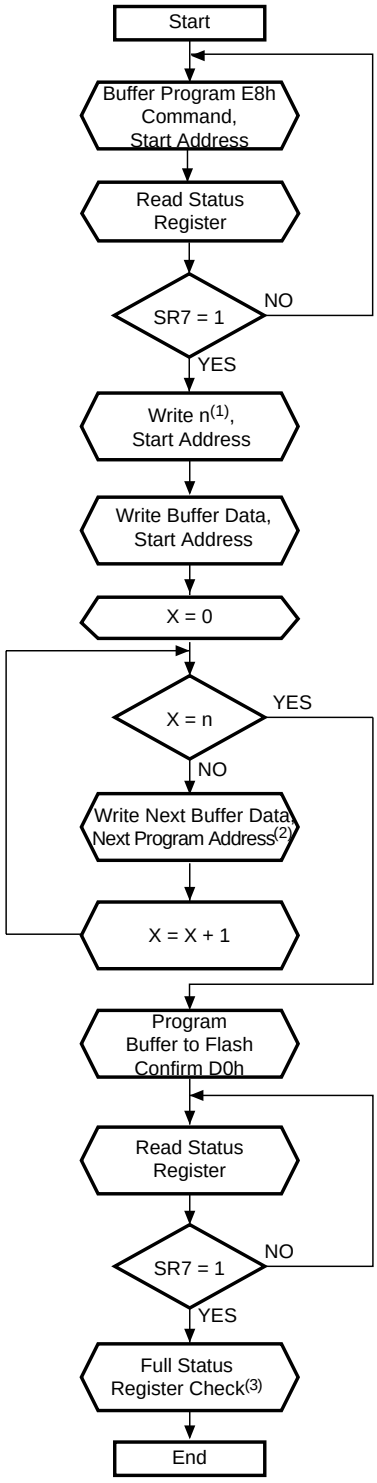



```
program_command (addressToProgram, dataToProgram) {:

        writeToFlash (addressToProgram, 0x40);
        /*writeToFlash (addressToProgram, 0x10);*/
                                        /*see note (3)*/

         writeToFlash (addressToProgram, dataToProgram) ;
         /*Memory enters read status state after
         the Program Command*/


      do {
         status_register=readFlash (addressToProgram);
                                        "see note (3)";
         /* E or G must be toggled*/



         } while (status_register.SR7== 0) ;

if  (status_register.SR3==1) /*VPP invalid error */
      error_handler ( ) ;

if  (status_register.SR4==1) /*program error */
      error_handler ( ) ;

if  (status_register.SR1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI06170b

1. Status check of SR1 (Protected Block), SR3 (V_{PP} Invalid) and SR4 (Program Error) can be made after each program operation or after a sequence.
2. If an error is found, the Status Register must be cleared before further Program/Erase Controller operations.
3. Any address within the bank can equally be used.

Figure 20. Buffer Program Flowchart and Pseudo Code

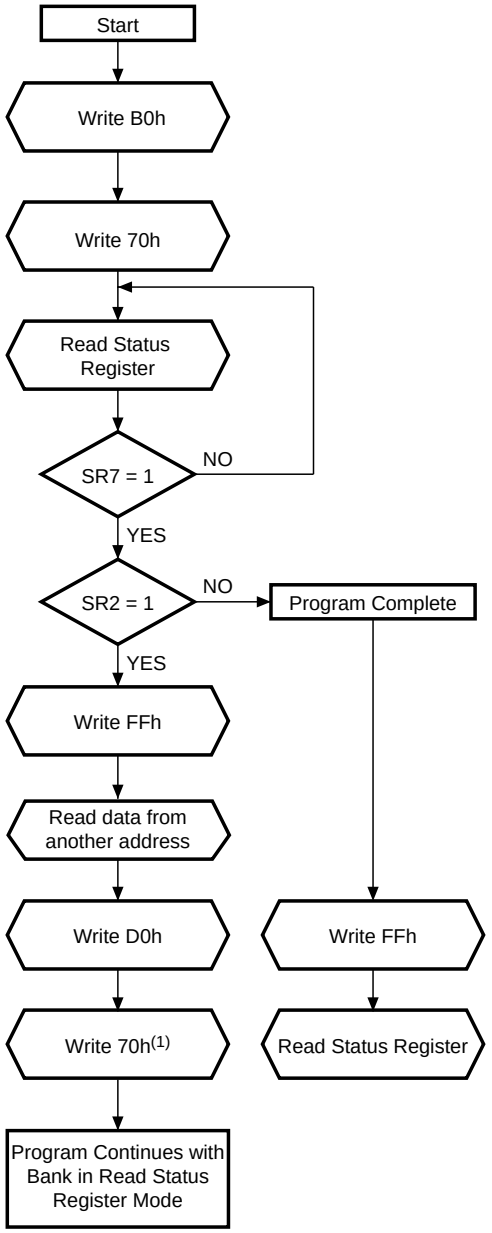



```
Buffer_Program_command (Start_Address,  n, buffer_Program[] )
 /* buffer_Program [] is an array structure used to store the address and
data to be programmed to the Flash memory (the address must be within
the segment Start Address and Start Address+n) */
{
 do {writeToFlash (Start_Address, 0xE8) ;

status_register=readFlash (Start_Address);

 } while (status_register.SR7==0);

 writeToFlash (Start_Address, n);

 writeToFlash (buffer_Program[0].address, buffer_Program[0].data);
/*buffer_Program[0].address is the start address*/

 x = 0;

 while (x<n)

 { writeToFlash (buffer_Program[x+1].address, buffer_Program[x+1].data);

       x++;

 }

 writeToFlash (Start_Address, 0xD0);

do {status_register=readFlash (Start_Address);

       } while (status_register.SR7==0);

full_status_register_check();

}
```

AI08913b

1. n + 1 is the number of data being programmed.
2. Next Program data is an element belonging to buffer_Program[].data; Next Program address is an element belonging to buffer_Program[].address.
3. Routine for Error Check by reading SR3, SR4 and SR1.

Figure 21. Program Suspend & Resume Flowchart and Pseudo Code

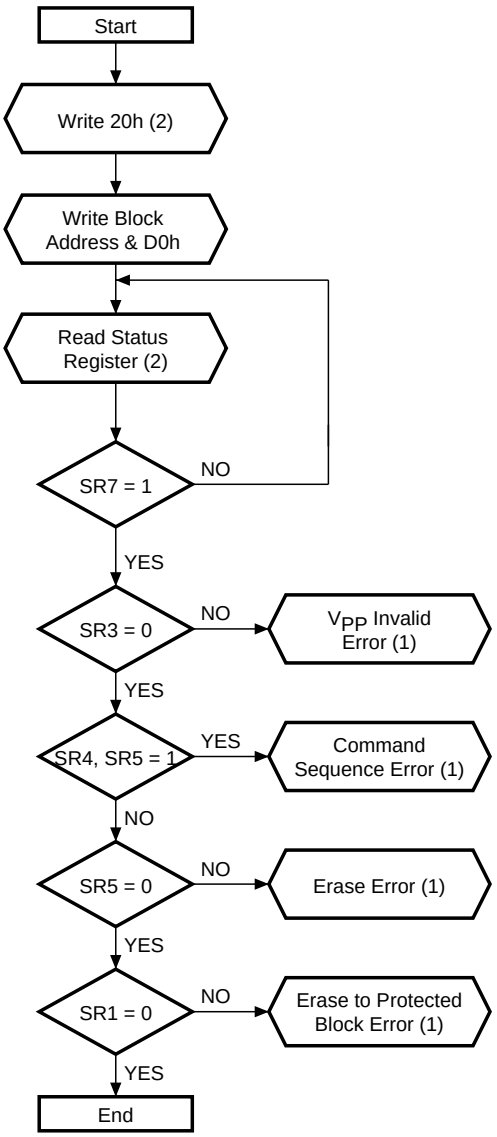



```
program_suspend_command  ( ) {
      writeToFlash (any_address, 0xB0) ;

      writeToFlash (bank_address, 0x70) ;
      /* read status register to check if
      program has already completed */


  do {
      status_register=readFlash (bank_address) ;
      /* E or G must be toggled*/



      } while (status_register.SR7== 0) ;


if  (status_register.SR2==0)  /*program completed */
      {  writeToFlash (bank_address, 0xFF)  ;
        read_data ( ) ; /*read data from another block*/
        /*The device returns to Read Array
        (as if program/erase suspend was not issued).*/


       }
else
      {  writeToFlash (bank_address, 0xFF)  ;
        read_data ( ); /*read data from another address*/
        writeToFlash (any_address, 0xD0) ;
        /*write 0xD0 to resume program*/


        writeToFlash (bank_address, 0x70) ;
        /*read status register to check if erase has completed */

       }
}
```

AI10117

1. The Read Status Register command (Write 70h) can be issued just before or just after the Program Resume command.

Figure 22. Block Erase Flowchart and Pseudo Code

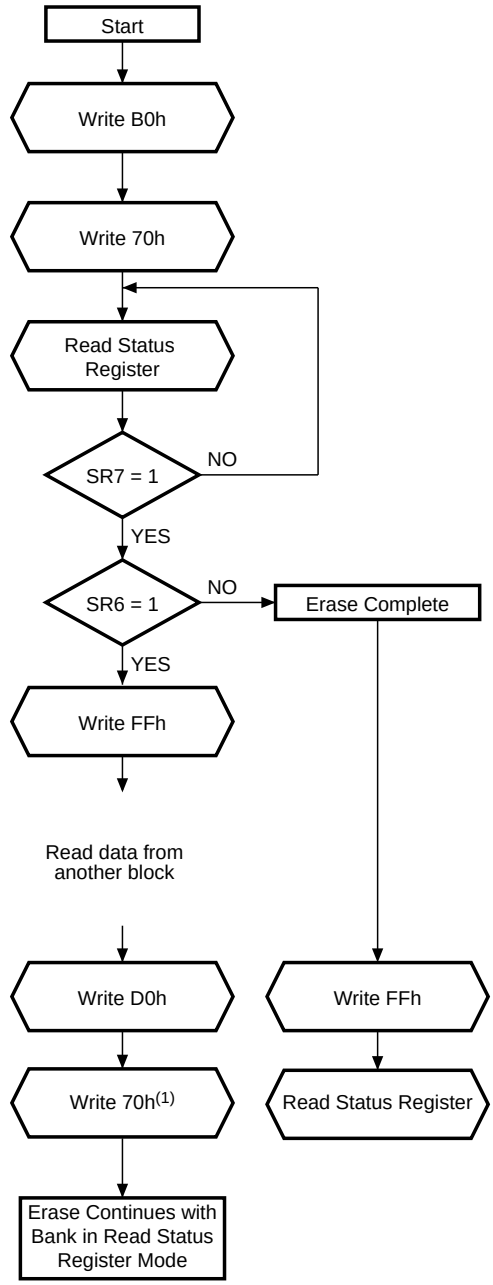



```
erase_command   ( blockToErase )  {
        writeToFlash (blockToErase, 0x20) ;
                                /*see note (2) */

        writeToFlash (blockToErase, 0xD0) ;
        /* only A12-A20 are significannt */
        /* Memory enters read status state after
        the Erase Command */

    do {
        status_register=readFlash (blockToErase) ;
                                        /* see note (2) */
        /* E or G must be toggled*/

        }  while (status_register.SR7== 0) ;

if  (status_register.SR3==1) /*VPP invalid error */
        error_handler ( ) ;

if  ( (status_register.SR4==1) && (status_register.SR5==1) )
/* command sequence error */
        error_handler ( ) ;

if  ( (status_register.SR5==1) )
/* erase error */
        error_handler ( ) ;

if  (status_register.SR1==1) /*program to protect block error */
        error_handler ( ) ;

}
```

AI06174b

1. If an error is found, the Status Register must be cleared before further Program/Erase operations.
2. Any address within the bank can equally be used.

Figure 23. Erase Suspend & Resume Flowchart and Pseudo Code

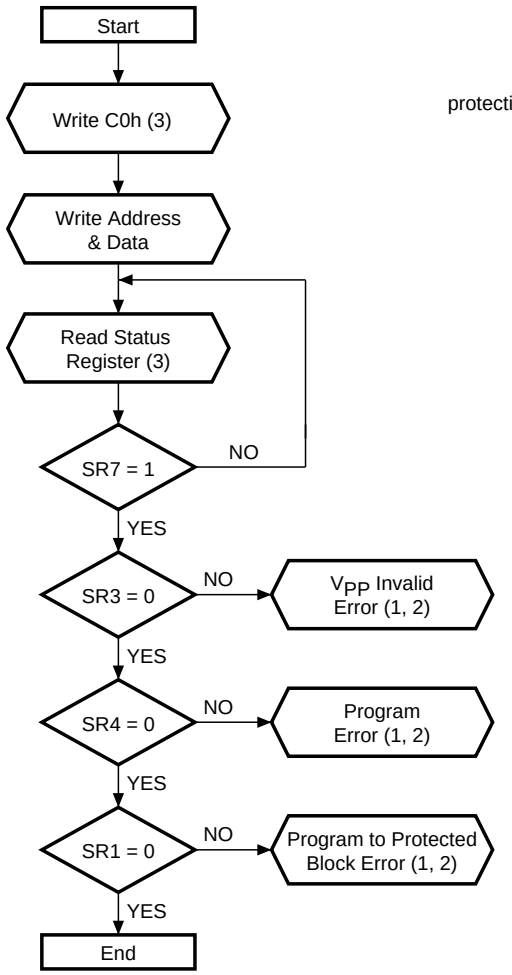



```
erase_suspend_command   ( ) {
      writeToFlash (bank_address, 0xB0) ;

      writeToFlash (bank_address, 0x70) ;
      /* read status register to check if
      erase has already completed */


   do {
       status_register=readFlash (bank_address) ;
       /* E or G must be toggled*/


      } while (status_register.SR7== 0) ;


if  (status_register.SR6==0)  /*erase completed */
      {  writeToFlash (bank_address, 0xFF)  ;


        read_data ( ) ;
        /*read data from another block*/
        /*The device returns to Read Array
        (as if program/erase suspend was not issued).*/


       }
else
      {  writeToFlash (bank_address, 0xFF)  ;
        read_program_data ( );
        /*read or program data from another address*/
        writeToFlash (bank_address, 0xD0) ;
        /*write 0xD0 to resume erase*/

        writeToFlash (bank_address, 0x70) ;
        /*read status register to check if erase has completed */
       }
}
```

AI10116

1. The Read Status Register command (Write 70h) can be issued just before or just after the Erase Resume command.

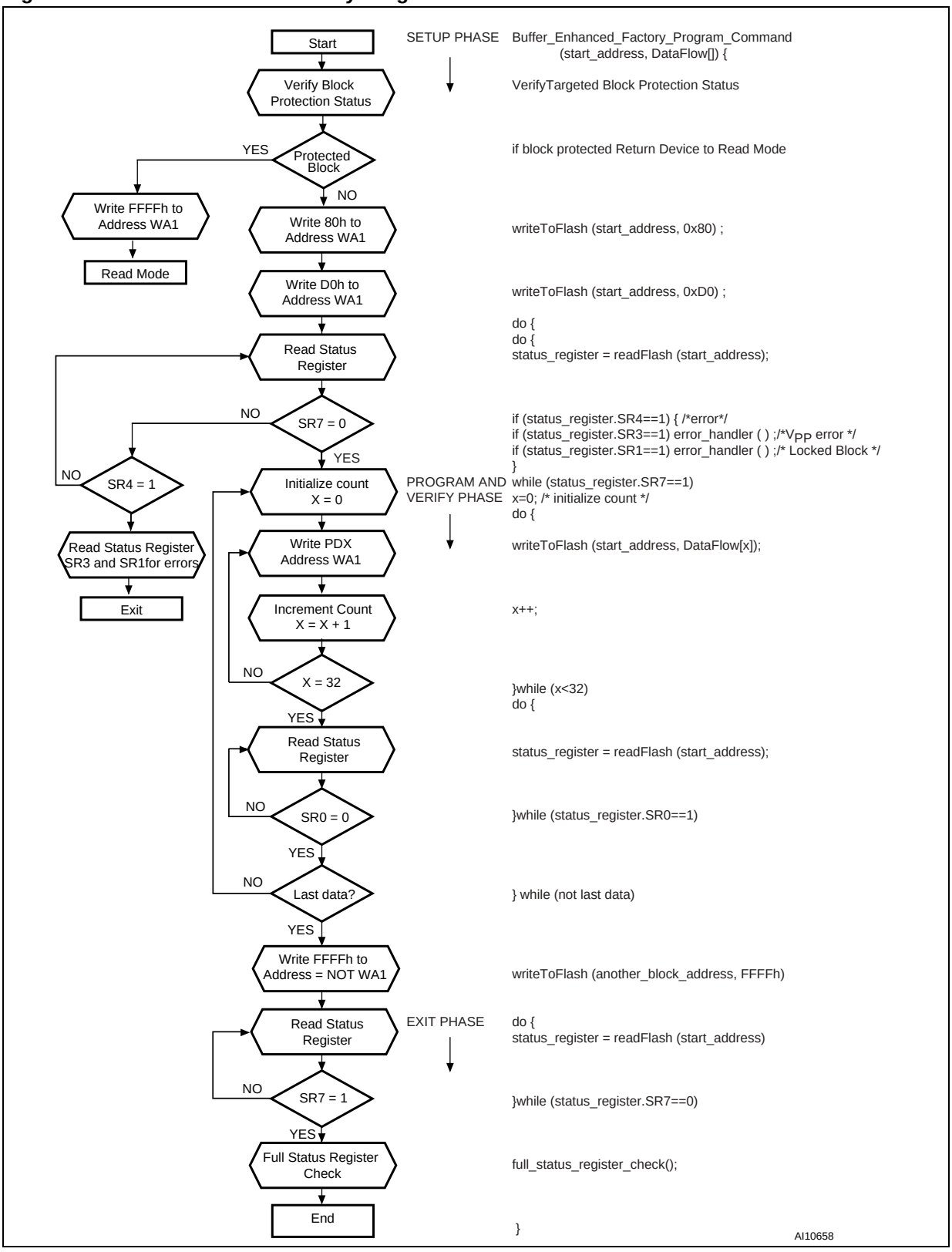
Figure 24. Protection Register Program Flowchart and Pseudo Code




```
protection_register_program_command (addressToProgram, dataToProgram) {:
                    writeToFlash (addressToProgram, 0xC0) ;
                                    /*see note (3) */

                    writeToFlash (addressToProgram, dataToProgram) ;
                    /*Memory enters read status state after
                    the Program Command*/

                  do {
                    status_register=readFlash (addressToProgram) ;
                                                  /* see note (3) */
                    /* E or G must be toggled*/

                    } while (status_register.SR7== 0) ;

if (status_register.SR3==1) /*VPP invalid error */
      error_handler ( ) ;

if (status_register.SR4==1) /*program error */
      error_handler ( ) ;

if (status_register.SR1==1) /*program to protect block error */
      error_handler ( ) ;

}
```

AI06177b

Figure 25. Buffer Enhanced Factory Program Flowchart and Pseudo Code



1. For how to check the targeted block protection status, refer to the Application Note concerning the device security features.

Appendix D Command Interface state tables

Table 46. Command Interface States - Modify Table, Next State

Current CI State		Command Input[1]									
		Read Array (FFh)[2]	Program Setup (10/40h) (3)(4)	Buffer Program (E8h)[3][4]	Block Erase, Setup (20h) (3)(4)	BEFP Setup (80h)	Erase Confirm P/E Resume, BEFP Confirm(D0h) (3)(4)	Buffer Program, Program/ Erase Suspend (B0h)	Read Status Register (70h)	Clear status Register (50h)[5]	Read Electronic Signature, Read CFI Query (90h, 98h)
Ready		Ready	Program Setup	Buffer Program Setup	Erase Setup	BEFP Setup	Ready				
Lock/CR Setup		Ready (Lock Error)					Ready	Ready (Lock Error)			
Program	Setup	Program Busy									
	Busy	Program Busy						Program Suspend	Program Busy		
	Suspend	Program Suspend					Program Busy	Program Suspend			
Buffer Program	Setup	Buffer Program Load 1 (give word count load (N-1));									
	Buffer Load 1	if N=0 go to Buffer Program Confirm. Else (N not =0) go to Buffer Program Load 2 (data load)									
	Buffer Load 2	Buffer Program Confirm when count =0; Else Buffer Program Load 2 (note: Buffer Program will fail at this point if any block address is different from the first address)									
	Confirm	Ready (error)					Buffer Program Busy	Ready (error)			
	Busy	Buffer Program Busy						Buffer Program Suspend	Buffer Program Busy		
	Suspend	Buffer Program Suspend					Buffer Program Busy	Buffer Program Suspend			
Erase	Setup	Ready (error)					Erase Busy	Ready (error)			
	Busy	Erase Busy						Erase Suspend	Erase Busy		
	Suspend	Erase Suspend	Program in Erase Suspend	Buffer Program Setup in Erase Suspend	Erase Suspend	Erase Busy		Erase Suspend			
Program in Erase Suspend	Setup	Program Busy in Erase Suspend									
	Busy	Program Busy in Erase Suspend						Program Suspend in Erase Suspend	Program Busy in Erase Suspend		
	Suspend	Program Suspend in Erase Suspend					Program Busy in Erase Suspend	Program Suspend in Erase Suspend			

Current CI State		Command Input(1)									
		Read Array (FFh)(2)	Program Setup (10/40h) (3)(4)	Buffer Program (E8h)(3)(4)	Block Erase, Setup (20h) (3)(4)	BEFP Setup (80h)	Erase Confirm P/E Resume, BEFP Confirm(D0h) (3)(4)	Buffer Program, Program/ Erase Suspend (B0h)	Read Status Register (70h)	Clear status Register (50h)(5)	Read Electronic Signature, Read CFI Query (90h, 98h)
Buffer Program in Erase Suspend	Setup	Buffer Program Load 1 in Erase Suspend (give word count load (N-1)); if N=0 go to Buffer Program confirm. Else (N not =0) go to Buffer Program Load 2									
	Buffer Load 1	Buffer Program Load 2 in Erase Suspend (data load)									
	Buffer Load 2	Buffer Program Confirm in Erase Suspend when count =0; Else Buffer Program Load 2 in Erase Suspend (note: Buffer Program will fail at this point if any block address is different from the first address)									
	Confirm	Ready (error)					Buffer Program Busy in Erase Suspend	Ready (error)			
	Busy	Buffer Program Busy in Erase Suspend						Buffer Program Suspend in Erase Suspend	Buffer Program Busy in Erase Suspend		
	Suspend	Buffer Program Suspend in Erase Suspend					Buffer Program Busy in Erase Suspend	Buffer Program Suspend in Erase Suspend			
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock Error)					Erase Suspend	Erase Suspend (Lock Error)			
Buffer EFP	Setup	Ready (error)					BEFP Busy	Ready (error)			
	Busy	BEFP Busy(6)									

1. CI = Command Interface, CR = Configuration Register, BEFP = Buffer Enhanced Factory Program, P/E. C. = Program/ Erase Controller.
2. At Power-Up, all banks are in Read Array mode. Issuing a Read Array command to a busy bank, results in undetermined data output.
3. The two cycle command should be issued to the same bank address.
4. If the P/E.C. is active, both cycles are ignored.
5. The Clear Status Register command clears the Status Register error bits except when the P/E.C. is busy or suspended.
6. BEFP is allowed only when Status Register bit SR0 is set to ‘0’. BEFP is busy if Block Address is first BEFP Address. Any other commands are treated as data.

Table 47. Command Interface States - Modify Table, Next Output State

Current CI State	Command Input[1][2]									
	Read Array (FFh)[3]	Program Setup (10/ 40h)[4][5]	Buffer Program (E8h)	Block Erase, Setup (20h)[4][5]	BEFP Setup (80h)	Erase Confirm P/E Resume, BEFP Confirm (D0h)[4][5]	Program/ Erase Suspend (B0h)	Read Status Register (70h)	Clear status Register (50h)	Read Electronic signature, Read CFI Query (90h, 98h)
Program Setup	Status Register									
Erase Setup										
Program in Erase Suspend										
BEFP Setup										
BEFP Busy										
Buffer Program Setup										
Buffer Program Load 1										
Buffer Program Load 2										
Buffer Program Confirm										
Buffer Program Setup in Erase Suspend										
Buffer Program Load 1 in Erase Suspend										
Buffer Program Load 2 in Erase Suspend										
Buffer Program Confirm in Erase Suspend										
Lock/CR Setup										
Lock/CR Setup in Erase Suspend										
Ready	Array	Status Register				Output Unchanged		Status Register	Output Unchanged	Electronic Signature/ CFI
Program Busy										
Erase Busy										
Buffer Program Busy										
Program/Erase Suspend										
Buffer Program Suspend										
Program Busy in Erase Suspend										
Buffer Program Busy in Erase Suspend										
Program Suspend in Erase Suspend										
Buffer Program Suspend in Erase Suspend										

1. The output state shows the type of data that appears at the outputs if the bank address is the same as the command address. A bank can be placed in Read Array, Read Status Register, Read Electronic Signature or Read CFI mode, depending on the command issued. Each bank remains in its last output state until a new command is issued to that bank. The next state does not depend on the bank output state.
2. CI = Command Interface, CR = Configuration Register, BEFP = Buffer Enhanced Factory Program, P/E. C. = Program/ Erase Controller.
3. At Power-Up, all banks are in Read Array mode. Issuing a Read Array command to a busy bank, results in undetermined data output.
4. The two cycle command should be issued to the same bank address.
5. If the P/E.C. is active, both cycles are ignored.

Table 48. Command Interface States - Lock Table, Next State

Current CI State		Command Input(1)(2)				
		Lock/CR Setup(60h)(2)	Set CR Confirm (03h)	Block Address (WA0) (XXXXh)(3)	Illegal Command(4)	WSM Operation Completed
Ready		Lock/CR Setup	Ready			N/A
Lock/CR Setup		Ready (Lock error)	Ready	Ready (Lock error)		N/A
Program	Setup	Program Busy				N/A
	Busy	Program Busy				Ready
	Suspend	Program Suspend				N/A
Buffer Program	Setup	Buffer Program Load 1 (give word count load (N-1)				N/A
	Buffer Load 1	Buffer Program Load 2(5)		Exit	see note(5)	N/A
	Buffer Load 2	Buffer Program Confirm when count =0; Else Buffer Program Load 2 (note: Buffer Program will fail at this point if any block address is different from the first address)				N/A
	Confirm	Ready (error)				N/A
	Busy	Buffer Program Busy				Ready
	Suspend	Buffer Program Suspend				N/A
Erase	Setup	Ready (error)				N/A
	Busy	Erase Busy				Ready
	Suspend	Lock/CR Setup in Erase Suspend	Erase Suspend			N/A
Program in Erase Suspend	Setup	Program Busy in Erase Suspend				N/A
	Busy	Program Busy in Erase Suspend				Erase Suspend
	Suspend	Program Suspend in Erase Suspend				N/A
Buffer Program in Erase Suspend	Setup	Buffer Program Load 1 in Erase Suspend (give word count load (N-1))				
	Buffer Load 1	Buffer Program Load 2 in Erase Suspend(6)		Exit	see note (6)	
	Buffer Load 2	Buffer Program Confirm in Erase Suspend when count =0; Else Buffer Program Load 2 in Erase Suspend (note: Buffer Program will fail at this point if any block address is different from the first address)				
	Confirm	Ready (error)				
	Busy	Buffer Program Busy in Erase Suspend				
	Suspend	Buffer Program Suspend in Erase Suspend				

Current CI State		Command Input(1)(2)				
		Lock/CR Setup(60h)(2)	Set CR Confirm (03h)	Block Address (WA0) (XXXXh)(3)	Illegal Command(4)	WSM Operation Completed
Lock/CR Setup in Erase Suspend		Erase Suspend (Lock error)	Erase Suspend	Erase Suspend (Lock error)		N/A
BEFP	Setup	Ready (error)				N/A
	Busy	BEFP Busy(7)		Exit	BEFP Busy(7)	N/A

1. CI = Command Interface, CR = Configuration Register, BEFP = Buffer Enhanced Factory Program, P/E. C. = Program/ Erase Controller, WA0 = Address in a block different from first BEFP address.
2. If the P/E.C. is active, both cycles are ignored.
3. BEFP Exit when Block Address is different from first Block Address and data are FFFFh.
4. Illegal commands are those not defined in the command set.
5. if N=0 go to Buffer Program Confirm. Else (N ≠ 0) go to Buffer Program Load 2 (data load).
6. if N=0 go to Buffer Program Confirm in Erase Suspend. Else (N ≠ 0) go to Buffer Program Load 2 in Erase Suspend.
7. BEFP is allowed only when Status Register bit SR0 is set to ‘0’. BEFP is busy if Block Address is first BEFP Address. Any other commands are treated as data.

Table 49. Command Interface States - Lock Table, Next Output State

<table>
<tr><th rowspan="2">Current CI State</th><th colspan="5">Command Input(1)(2)</th></tr>
<tr><th>Lock/CR Setup (60h)(3)</th><th>Set CR Confirm (03h)</th><th>BEFP Exit (FFFFh)(4)</th><th>Illegal Command(5)</th><th>WSM Operation Completed</th></tr>
<tr><td>Program Setup</td><td colspan="4" rowspan="11">Status Register</td><td rowspan="23">Output Unchanged</td></tr>
<tr><td>Erase Setup</td></tr>
<tr><td>Program in Erase Suspend</td></tr>
<tr><td>BEFP Setup</td></tr>
<tr><td>BEFP Busy</td></tr>
<tr><td>Buffer Program Setup</td></tr>
<tr><td>Buffer Program Load 1</td></tr>
<tr><td>Buffer Program Load 2</td></tr>
<tr><td>Buffer Program Confirm</td></tr>
<tr><td>Buffer Program Setup in Erase Suspend</td></tr>
<tr><td>Buffer Program Load 1 in Erase Suspend</td></tr>
<tr><td>Buffer Program Load 2 in Erase Suspend</td><td rowspan="12">Status Register</td><td rowspan="2">Array</td><td colspan="2" rowspan="2">Status Register</td></tr>
<tr><td>Buffer Program Confirm in Erase Suspend</td></tr>
<tr><td>Lock/CR Setup</td><td rowspan="11">Output Unchanged</td><td rowspan="11">Array</td><td rowspan="11">Output Unchanged</td></tr>
<tr><td>Lock/CR Setup in Erase Suspend</td></tr>
<tr><td>Ready</td></tr>
<tr><td>Program Busy</td></tr>
<tr><td>Erase Busy</td></tr>
<tr><td>Buffer Program Busy</td></tr>
<tr><td>Program/Erase Suspend</td></tr>
<tr><td>Buffer Program Suspend</td></tr>
<tr><td>Program Busy in Erase Suspend</td></tr>
<tr><td>Buffer Program Busy in Erase Suspend</td></tr>
<tr><td>Program Suspend in Erase Suspend</td></tr>
<tr><td>Buffer Program Suspend in Erase Suspend</td></tr>
</table>

1. The output state shows the type of data that appears at the outputs if the bank address is the same as the command address. A bank can be placed in Read Array, Read Status Register, Read Electronic Signature or Read CFI mode, depending on the command issued. Each bank remains in its last output state until a new command is issued to that bank. The next state does not depend on the bank's output state.

2. CI = Command Interface, CR = Configuration Register, BEFP = Buffer Enhanced Factory Program, P/E. C. = Program/ Erase Controller, WA0 = Address in a block different from first BEFP address.
3. If the P/E.C. is active, both cycles are ignored.
4. BEFP Exit when Block Address is different from first Block Address and data are FFFFh.
5. Illegal commands are those not defined in the command set.

14 Revision history

Table 50. Document Revision History

Date	Version	Revision Details
16-Nov-2004	0.1	First Issue.
10-Dec-2004	0.2	Asynchronous Page Read mode added in *Summary description*, *Section 3: Bus operations*. *Figure 10: Asynchronous Page Read AC Waveforms* updated and *Table 22: Asynchronous Read AC Characteristics* for t_{AVQV1}.
17-Jan-2004	0.3	$\overline{WP}$ and R pins removed from *Figure 1: Logic Diagram*. $\overline{WP}$ removed from *Figure 15: Write AC Waveforms, Write Enable Controlled* and *Figure 16: Write AC Waveforms, Chip Enable Controlled*.
20-Jun-2005	0.4	80ns speed class chagned into 85ns. DU pins changed into NC in *Figure 2: TBGA64 Connections (Top view through package)*. t_{WHQV} removed from *Figure 15*, *Figure 16*. *Table 22*, *Table 23* and *Table 26* updated. *Table 24* updated; t_{WHQV} removed and t_{AVWH}, t_{ELQV}, t_{ELKV}, t_{GHWL}, t_{WHAV}, and t_{WHAX} timings added. *Table 25* updated, t_{WHQV} removed, and t_{AVEH}, t_{EHAX}, t_{EHGL}, t_{ELKV}, and t_{GHEL} added.
21-Jun-2005	0.5	t_{GHTZ} added in*Table 22: Asynchronous Read AC Characteristics* and *Table 23: Synchronous Read AC Characteristics*.
29-Sep-2005	1.0	Burst frequency chagned from 54 to 52MHz. 85ns speed class removed. t_{AVQV1} changed to 25ns. V_{IO} maximum value updated in *Table 17: Absolute Maximum Ratings*. t_{AVLH} and t_{LLLH} updated in *Table 22: Asynchronous Read AC Characteristics*. t_{AVKH}, t_{ELKH} and t_{LLKH} updated in *Table 23: Synchronous Read AC Characteristics*. t_{AVLH}, t_{LLLH} and t_{ELLH} updated in *Table 24: Write AC Characteristics, Write Enable Controlled* and *Table 25: Write AC Characteristics, Chip Enable Controlled*.