

MITSUBISHI LSIs
M5M51008CP,FP,VP,RV,KV,KR -55H, -70H,
-55X, -70X

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008CP,FP,VP,RV,KV,KR are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance quadruple-polysilicon and double metal CMOS technology. The use of thin film transistor (TFT) load cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51008CVP,RV,KV,KR are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD). Two types of devices are available. M5M51008CVP,KV(normal lead bend type package), M5M51008CRV,KR(reverse lead bend type package).Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

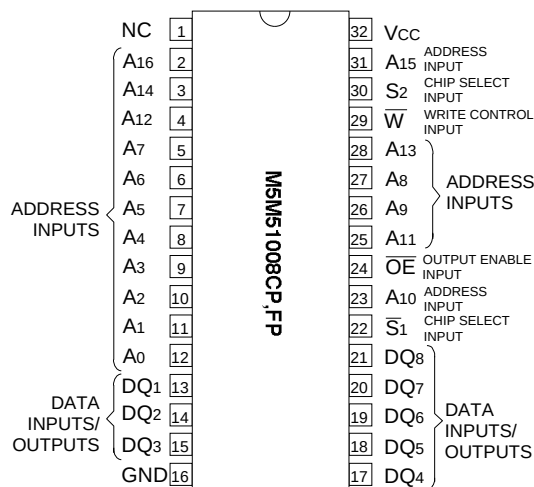
Type name	Access time (max)	Power supply current	
		Active (1MHz) (max)	stand-by (max)
M5M51008CP,FP,VP,RV,KV,KR-55H	55ns	15mA (1MHz)	20μA (V _{cc} =5.5V)
M5M51008CP,FP,VP,RV,KV,KR-70H	70ns		8μA (V _{cc} =5.5V) 0.1μA (V _{cc} =3.0V typ)
M5M51008CP,FP,VP,RV,KV,KR-55X	55ns		
M5M51008CP,FP,VP,RV,KV,KR-70X	70ns		

- Low stand-by current 0.1μA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S_1}, \overline{S_2}$
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- $\overline{OE}$ prevents data contention in the I/O bus
- Common data I/O
- Package
 - M5M51008CP32pin 600mil DIP
 - M5M51008CFP32pin 525mil SOP
 - M5M51008CVP,RV32pin 8 X 20 mm² TSOP
 - M5M51008CKV,KR32pin 8 X 13.4 mm² TSOP

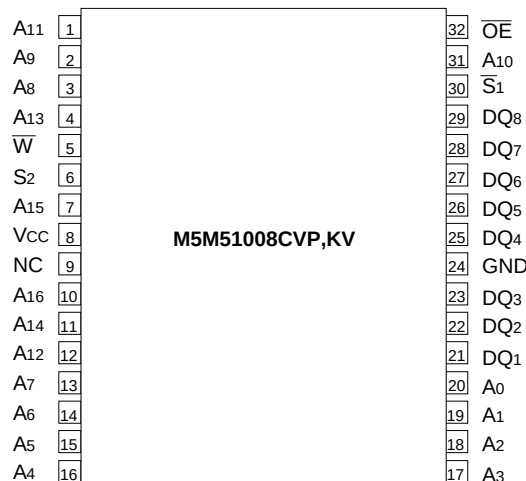
APPLICATION

Small capacity memory units

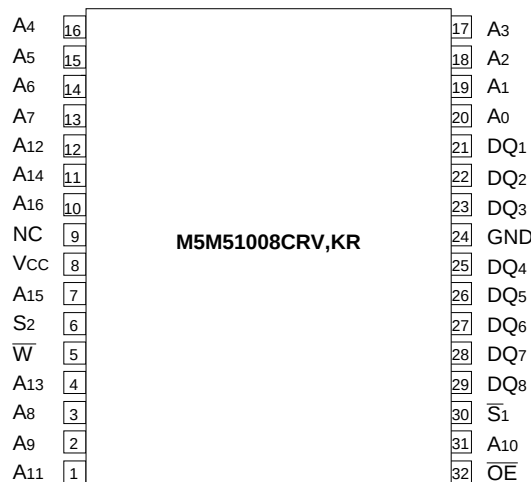
PIN CONFIGURATION (TOP VIEW)



Outline 32P4(P), 32P2M-A(FP)



Outline 32P3H-E(VP), 32P3K-B(KV)



Outline 32P3H-F(RV), 32P3K-C(KR)

NC : NO CONNECTION

A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S_1}$ and S_2 are in an active state ($\overline{S_1}=L, S_2=H$).

$\overline{S_1}$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	Icc
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

The block diagram illustrates the internal architecture of the 131072 Words X 8 Bits (512 Rows X 128 Columns X 16 Blocks) memory array. The central component is the memory array, which is connected to various control and data buffers.

Address Inputs: The address inputs are divided into three groups: A4-A13 (pins 8-16), A0-A3 (pins 12-17), and A10-A11 (pins 23-25). These inputs are connected to three Address Input Buffers (AIBs). The AIBs are connected to the Row Decoder, Column Decoder, and Block Decoder, which in turn control the memory array.

Control Inputs: The control inputs include the Write Control Input (W, pin 29), Chip Select Inputs (S1, pin 22; S2, pin 30), Output Enable Input (OE, pin 24), and Power (Vcc, pin 32; GND (0V), pin 16).

Data Inputs/Outputs: The data inputs/outputs are connected to the Data Input Buffer (DIB) and the Output Buffer (OB). The DIB is connected to the memory array and the OB. The OB is connected to the Sense Amplifier (SA) and the Data Input Buffer (DIB). The SA is connected to the memory array and the OB. The DIB is connected to the memory array and the OB.

Internal Components: The internal components include the Row Decoder, Column Decoder, Block Decoder, Clock Generator, Sense Amplifier (SA), and Data Input Buffer (DIB). The memory array is connected to the Row Decoder, Column Decoder, and Block Decoder. The Clock Generator is connected to the memory array and the DIB. The Sense Amplifier (SA) is connected to the memory array and the OB. The Data Input Buffer (DIB) is connected to the memory array and the OB.

* Pin numbers inside dotted line show those of TSOP

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage	With respect to GND	- 0.3*~7	V
V _I	Input voltage		- 0.3*~V _{CC} + 0.3	V
V _O	Output voltage		0~V _{CC}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0~70	°C
T _{stg}	Storage temperature		- 65~150	°C

* -3.0V in case of AC (Pulse width ≤ 50ns)

DC ELECTRICAL CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.2		V _{CC} + 0.3	V
V _{IL}	Low-level input voltage		-0.3*		0.8	V
V _{OH}	High-level output voltage	I _{OH} = -1.0mA	2.4			V
		I _{OH} = -0.1mA	V _{CC} - 0.5			V
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	V
I _I	Input current	V _I =0~V _{CC}			±1	μA
I _O	Output current in off-state	$\overline{S_1}$ =V _{IH} or S ₂ =V _{IL} or $\overline{OE}$ =V _{IH} V _{I/O} =0~V _{CC}			±1	μA
I _{CC1}	Active supply current (AC, MOS level)	$\overline{S_1}$ ≤ V _{CC} -0.2V, S ₂ ≥ V _{CC} -0.2V other inputs ≤ 0.2V or ≥ V _{CC} -0.2V Output-open(duty 100%)	55ns		80	mA
			70ns		70	
			1MHz		15	
I _{CC2}	Active supply current (AC, TTL level)	$\overline{S_1}$ =V _{IL} , S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} Output-open(duty 100%)	55ns		85	mA
			70ns		70	
			1MHz		15	
I _{CC3}	Stand-by current	1) S ₂ ≤ 0.2V, other inputs=0~V _{CC} 2) $\overline{S_1}$ ≥ V _{CC} -0.2V, S ₂ ≥ V _{CC} -0.2V, other inputs=0~V _{CC}	-H	~25°C	2	μA
				~40°C	6	
				~70°C	20	
			-X	~25°C	1	
				~40°C	3	
				~70°C	8	
I _{CC4}	Stand-by current	$\overline{S_1}$ =V _{IH} or S ₂ =V _{IL} , other inputs=0~V _{CC}			3	mA

* -3.0V in case of AC (Pulse width ≤ 50ns)

CAPACITANCE (T_a=0~70°C, V_{CC}=5V±10% unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _i	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			6	pF
C _o	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			10	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is V_{CC} = 5V, T_a = 25°C

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AC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, 5V±10% unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse level $V_{IH}=2.4V, V_{IL}=0.6V$ (-70H,-70X)

$V_{IH}=3.0V, V_{IL}=0.0V$ (-55H,-55X)

Input rise and fall time 5ns

Reference level $V_{OH}=V_{OL}=1.5V$

Output loads Fig.1, $C_L=30pF$ (-55H,-70H,-55X,-70X)

$C_L=5pF$ (for t_{en}, t_{dis})

Transition is measured ± 500mV from steady state voltage. (for t_{en}, t_{dis})

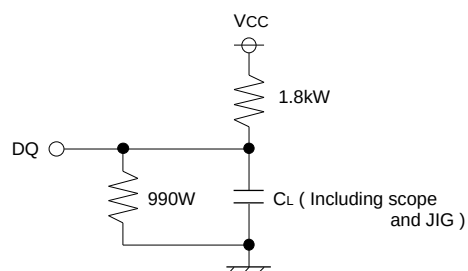


Fig.1 Output load

(2) READ CYCLE

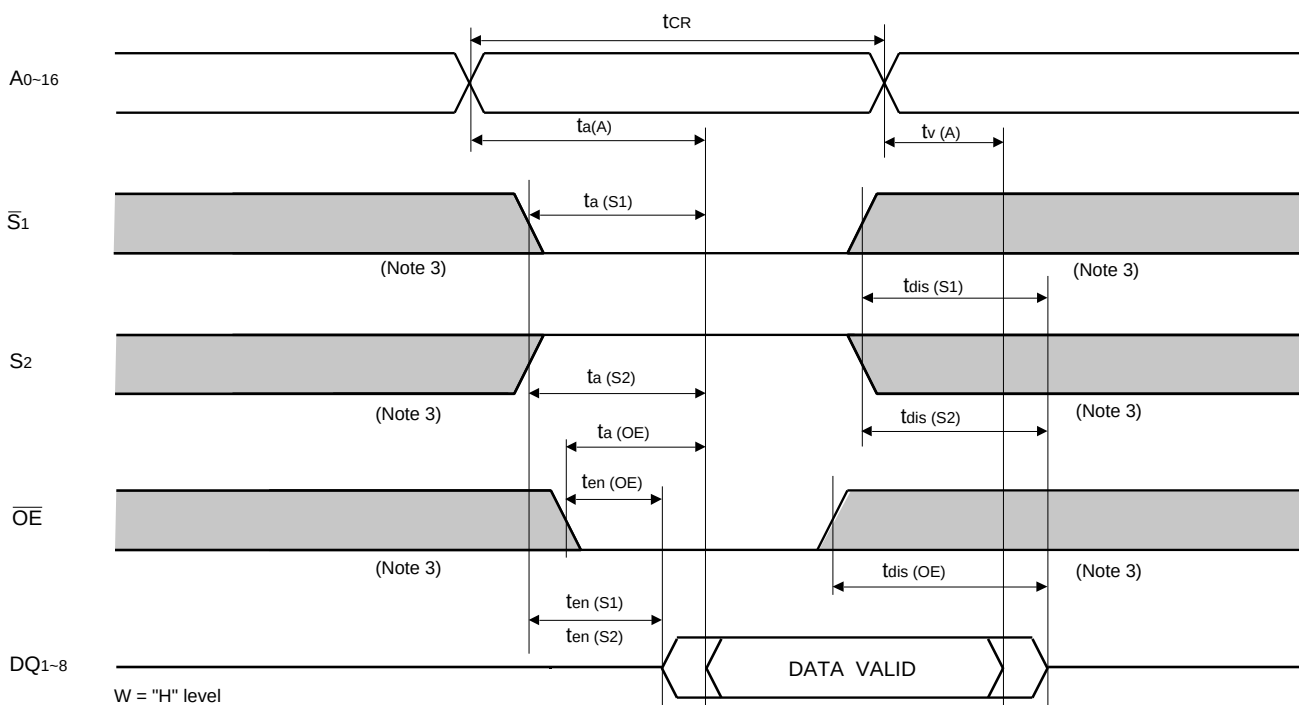
Symbol	Parameter	Limits				Unit
		-55H,-55X		-70H,-70X		
		Min	Max	Min	Max	
tCR	Read cycle time	55		70		ns
ta(A)	Address access time		55		70	ns
ta(S1)	Chip select 1 access time		55		70	ns
ta(S2)	Chip select 2 access time		55		70	ns
ta(OE)	Output enable access time		30		35	ns
tdis(S1)	Output disable time after $\overline{S_1}$ high		20		25	ns
tdis(S2)	Output disable time after S_2 low		20		25	ns
tdis(OE)	Output disable time after $\overline{OE}$ high		20		25	ns
ten(S1)	Output enable time after $\overline{S_1}$ low	5		10		ns
ten(S2)	Output enable time after S_2 high	5		10		ns
ten(OE)	Output enable time after $\overline{OE}$ low	5		5		ns
tv(A)	Data valid time after address	5		10		ns

(3) WRITE CYCLE

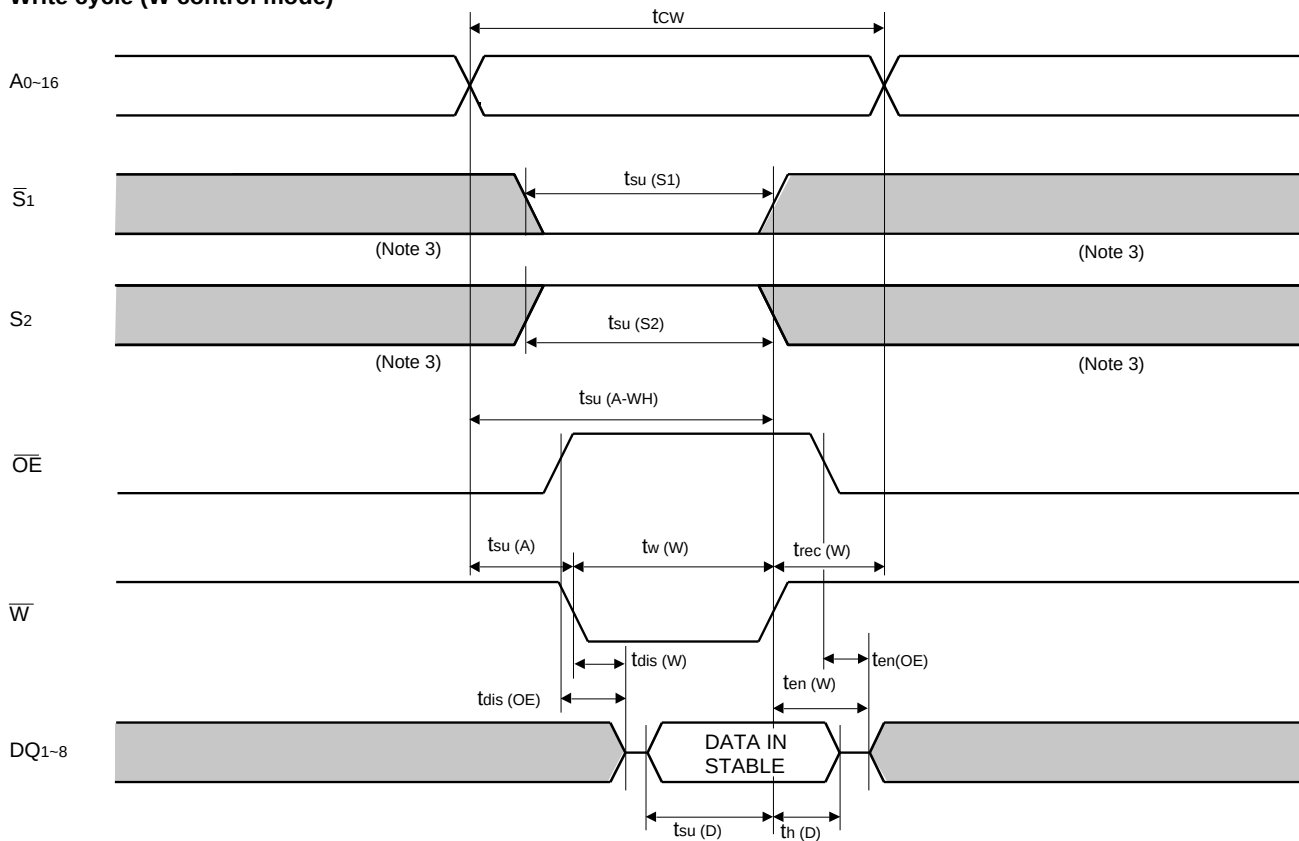
Symbol	Parameter	Limits				Unit
		-55H,-55X		-70H,-70X		
		Min	Max	Min	Max	
tcw	Write cycle time	55		70		ns
tw(W)	Write pulse width	45		55		ns
tsu(A)	Address setup time	0		0		ns
tsu(A-WH)	Address setup time with respect to $\overline{W}$	50		65		ns
tsu(S1)	Chip select 1 setup time	50		65		ns
tsu(S2)	Chip select 2 setup time	50		65		ns
tsu(D)	Data setup time	25		30		ns
th(D)	Data hold time	0		0		ns
trec(W)	Write recovery time	0		0		ns
tdis(W)	Output disable time from $\overline{W}$ low		20		25	ns
tdis(OE)	Output disable time from $\overline{OE}$ high		20		25	ns
ten(W)	Output enable time from $\overline{W}$ high	5		5		ns
ten(OE)	Output enable time from $\overline{OE}$ low	5		5		ns

(4) TIMING DIAGRAMS

Read cycle

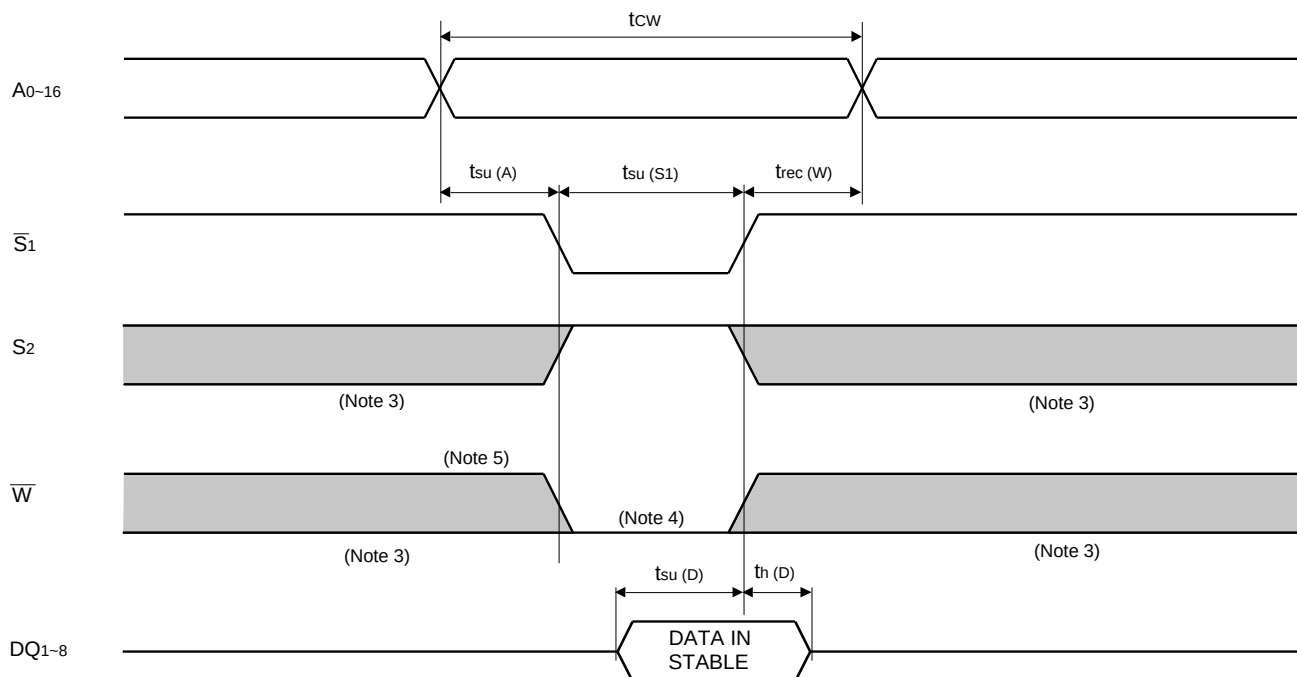


Write cycle ($\overline{W}$ control mode)

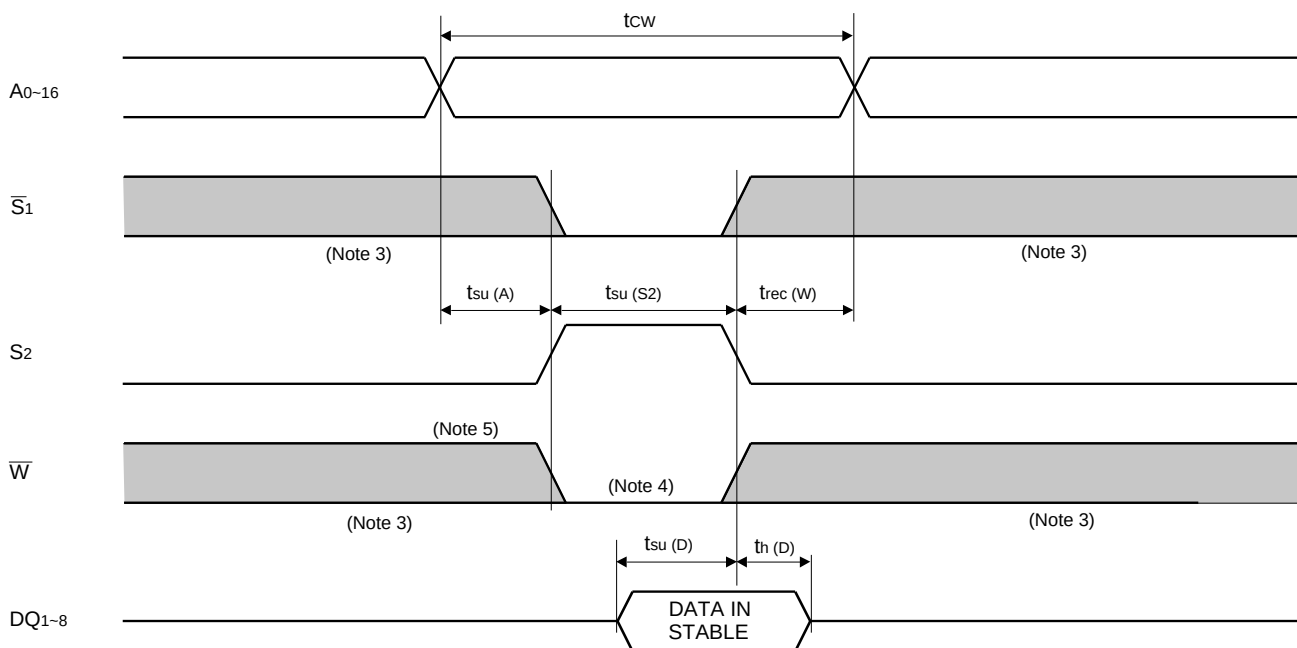


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Write cycle ($\overline{S_1}$ control mode)



Write cycle (S2 control mode)



Note 3: Hatching indicates the state is "don't care".

4: Writing is executed while S2 high overlaps $\overline{S_1}$ and $\overline{W}$ low.

5: When the falling edge of $\overline{W}$ is simultaneously or prior to the falling edge of $\overline{S_1}$ or rising edge of S2, the outputs are maintained in the high impedance state.

6: Don't apply inverted phase signal externally when DQ pin is output mode.

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

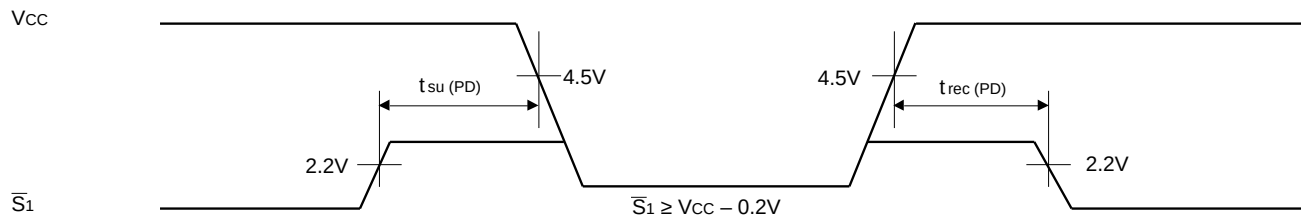
Symbol	Parameter	Test conditions			Limits			Unit
					Min	Typ	Max	
V _{CC} (PD)	Power down supply voltage				2.0			V
V _I (S1)	Chip select input $\overline{S}_1$	2.2V≤V _{CC} (PD)			2.2			V
		2V≤V _{CC} (PD)≤2.2V				V _{CC} (PD)		
V _I (S2)	Chip select input S ₂	4.5V≤V _{CC} (PD)					0.8	V
		V _{CC} (PD)<4.5V					0.2	
I _{CC} (PD)	Power down supply current	V _{CC} = 3V 1) S ₂ ≤ 0.2V, other inputs = 0~3V 2) $\overline{S}_1$ ≥ V _{CC} -0.2V, S ₂ ≥ V _{CC} -0.2V other inputs = 0~3V	-H	~25°C			1	μA
				~40°C			3	
				~70°C			10	
			-X	~25°C			0.5	
				~40°C			1.5	
				~70°C			4	

(2) TIMING REQUIREMENTS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su} (PD)	Power down set up time		0			ns
t _{rec} (PD)	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

$\overline{S}_1$ control mode



S₂ control mode

