To all our customers

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Jan.10,2003 Ver. 2.1

# M5M5J167KT - 70HI

16777216-BIT (1048576-WORD BY 16-BIT / 2097152-WORD BY 8-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5J167KT is a family of low voltage 16Mbit static RAMs organized as 1048576-words by 16-bit / 2097152-words by 8-bit, fabricated by Mitsubishi's high-performance 0.18µm CMOS technology.

The M5M5J167KT is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

The M5M5J167KT is made by stacked-micro-package technology and two chips of 8Mbits SRAMs are assembled in one package. By using this package technology, small package size can be achieved for highdensity SRAM.

The M5M5J167KT is packaged in a 52pin-µTSOP with the outline of 10.79mm x 10.49mm, and pin pitch of 0.40mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

The operating temperature range is -40 ~ +85°C

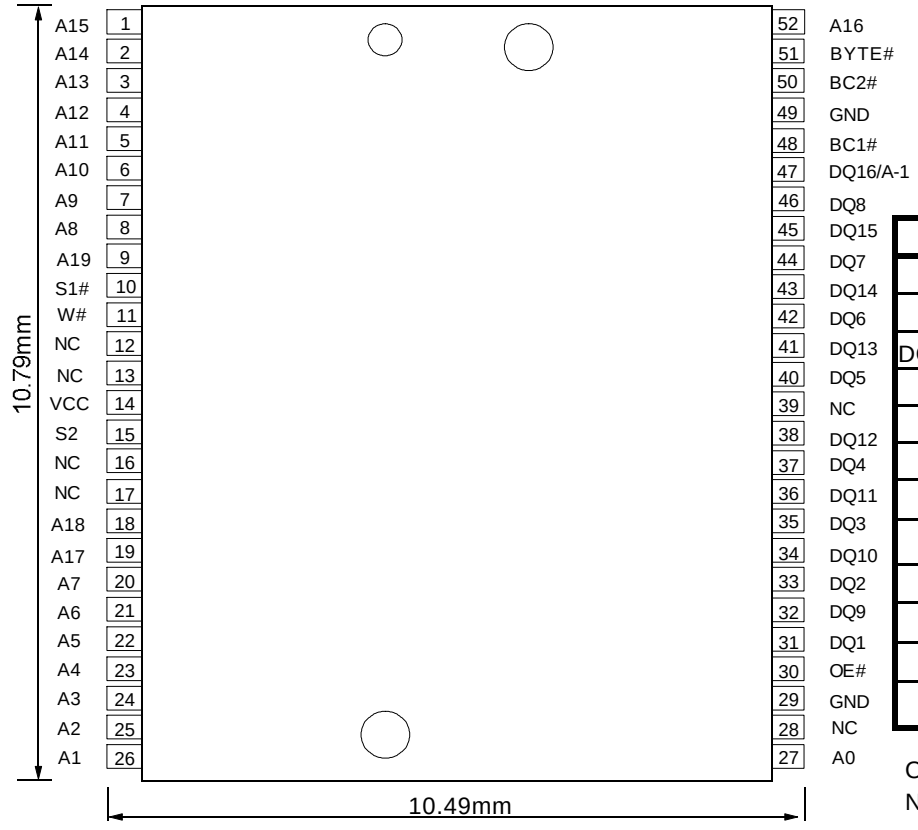
## FEATURES

- Single 2.7~3.6V power supply
- Small stand-by current: 0.2µA (2.0V, typ.)
- No clocks, No refresh
- Data retention supply voltage =2.0~3.6V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S1#, S2, BC1# and BC2#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Byte function (x8 mode) available by Byte# & A-1.
- Process technology: 0.18µm CMOS
- Package: 52pin 10.79mm x 10.49mm µTSOP
  [0.4mm pin pitch]

| Operating temperature | Part name | Power Supply | Access time max. | Stand-by current * Typical 25ºC | Stand-by current * Typical 40ºC | Stand-by current Ratings (max.) 25ºC | Stand-by current Ratings (max.) 40ºC | Stand-by current Ratings (max.) 70ºC | Stand-by current Ratings (max.) 85ºC | Active current Icc1 (3.3V, Typ.) |
|---|---|---|---|---|---|---|---|---|---|---|
| -40 ~ +85°C | M5M5J167KT -70HI | 2.7 ~ 3.6V | 70ns | 2.0 | 2.4 | 10 | 16 | 40 | 80 | 30mA (10MHz) 5mA (1MHz) |

* Typical parameter indicates the value for the center of distribution, and not 100% tested.

## PIN CONFIGURATION




| Pin | Function |
|---|---|
| A0 ~ A18 | Address input |
| A19 | Address input |
| DQ1 ~ DQ16 | Data input / output |
| S1# | Chip select input 1 |
| S2 | Chip select input 2 |
| W# | Write control input |
| OE# | Output enable input |
| BC1# | Lower Byte (DQ1 ~ 8) |
| BC2# | Upper Byte (DQ9 ~ 16) |
| BYTE# | Byte (x8 mode) enable input |
| Vcc | Power supply |
| GND | Ground supply |

Outline: 52PTG-A
N C : No Connection

## FUNCTION

The M5M5J167KT is organized as 1048576-words by 16-bit / 2097152-words by 8-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs BC1# , BC2# , S1#, S2 , W#, OE# and BYTE#. Each mode is summarized in the function table. The address select A19 can select either one 8MSRAM chip or another 8MSRAM chip.

A write operation is executed whenever the low level W# overlaps with the low level BC1# and/or BC2# and the low level S1# and the high level S2. The address (A-1~A19 : Byte mode, A0~A19 : Word mode) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting W# at a high level and OE# at a low level while BC1# and/or BC2# and S1#and S2 are in an active state (S1#=L, S2=H).

When setting BYTE# at a low level, the function will be in the x8 mede, which is, DQ1-8 are available and DQ9-16 are not available. In the x8 mode, A-1 is used as the additional address. During the active function for x8 mode, BC1# BC2# must be low level.

When setting BC1# and BC2# at a high level or S1# at a high level or S2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled.

In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by BC1#, BC2# and S1#, S2.

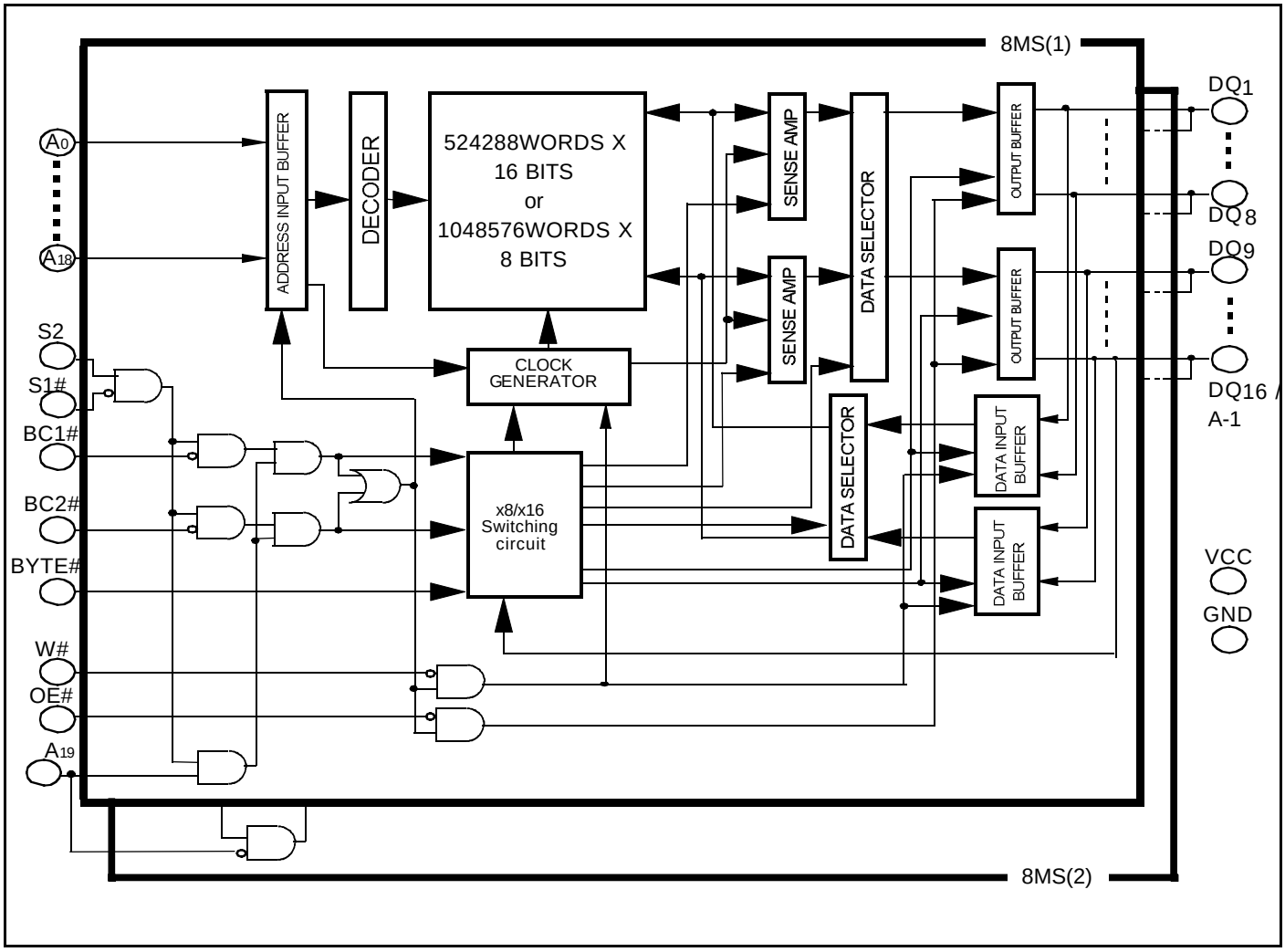
The power supply current is reduced as low as 0.2µA (25°C, typical), and the memory data can be held at +2.0V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

## FUNCTION TABLE

| S1# | S2 | BYTE# | BC1# | BC2# | W# | OE# | Mode | DQ1~8 | DQ9~15 | DQ16 | Icc |
|---|---|---|---|---|---|---|---|---|---|---|---|
| H | H | X | X | X | X | X | Non selection | High-Z | High-Z | High-Z | Standby |
| X | L | X | X | X | X | X | Non selection | High-Z | High-Z | High-Z | Standby |
| X | X | H | H | H | X | X | Non selection | High-Z | High-Z | High-Z | Standby |
| L | H | H | L | H | L | X | Write | Din | High-Z | High-Z | Active |
| L | H | H | L | H | H | L | Read | Dout | High-Z | High-Z | Active |
| L | H | H | L | H | H | H | ------- | High-Z | High-Z | High-Z | Active |
| L | H | H | H | L | L | X | Write | High-Z | Din | Din | Active |
| L | H | H | H | L | H | L | Read | High-Z | Dout | Dout | Active |
| L | H | H | H | L | H | H | ------- | High-Z | High-Z | High-Z | Active |
| L | H | H | L | L | L | X | Write | Din | Din | Din | Active |
| L | H | H | L | L | H | L | Read | Dout | Dout | Dout | Active |
| L | H | H | L | L | H | H | ------- | High-Z | High-Z | High-Z | Active |
| L | H | L | L | L | L | X | Write | Din | High-Z | A-1 | Active |
| L | H | L | L | L | H | L | Read | Dout | High-Z | A-1 | Active |
| L | H | L | L | L | H | H | ------- | High-Z | High-Z | A-1 | Active |

Note1 : "H" and "L" in this table mean $V_{IH}$ and $V_{IL}$, respectively.
Note2 : "X" in this table should be "H" or "L".

BLOCK DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Units |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to GND | - 0.3* ~ +4.6 | V |
| $V_I$ | Input voltage | With respect to GND | - 0.3* ~ Vcc + 0.3 (max. 4.6V) | |
| $V_O$ | Output voltage | With respect to GND | 0 ~ Vcc | |
| $P_d$ | Power dissipation | Ta = 25°C | 700 | mW |
| $T_a$ | Operating temperature | | -40 ~ +85 | °C |
| $T_{stg}$ | Storage temperature | | - 65 ~ +150 | °C |

* -3.0V in case of AC (Pulse width ≦ 30ns)

## DC ELECTRICAL CHARACTERISTICS (Ta=-40~85°C Vcc=2.7V~3.6V,unless otherwise noted)

| Symbol | Parameter | Conditions | | Limits Min | Limits Typ | Limits Max | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | | 2.2 | | Vcc+0.2V | V |
| $V_{IL}$ | Low-level input voltage | | | - 0.2 * | | 0.6 | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$= - 0.5mA | | 2.4 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$= 2.0mA | | | | 0.4 | |
| $I_I$ | Input leakage current | $V_I$ =0 ~ Vcc | | | | ±1 | µA |
| $I_O$ | Output leakage current | BC1# and BC2#=VIH or S1#=VIH or S2=VIL or OE#=VIH, VI/O=0 ~ Vcc | | | | ±1 | |
| Icc1 | Active supply current (AC,MOS level) | BC1# and BC2# ≦ 0.2V, S1# ≦ 0.2V, S2 ≧Vcc-0.2V other inputs ≦ 0.2V or ≧ Vcc-0.2V Output - open (duty 100%) | f= 10MHz | - | 30 | 50 | mA |
| | | | f= 1MHz | - | 5 | 15 | |
| Icc2 | Active supply current (AC,TTL level) | BC1# and BC2#=VIL , S1#=VIL ,S2=VIH other pins =VIH or VIL Output - open (duty 100%) | f= 10MHz | - | 30 | 50 | |
| | | | f= 1MHz | - | 5 | 15 | |
| Icc3 | Stand by supply current (AC,MOS level) | (1) S1# ≧ Vcc - 0.2V and S2 ≧ Vcc - 0.2V, BYTE# ≧ Vcc - 0.2V or ≦ 0.2V, other inputs = 0 ~ Vcc | ~ +25°C | - | 2.0 | 10 | µA |
| | | (2) S2 ≦ 0.2V, BYTE# ≧ Vcc - 0.2V or ≦ 0.2V, other inputs = 0 ~ Vcc | ~ +40°C | - | 2.4 | 16 | |
| | | (3) BC1# and BC2# ≧ Vcc - 0.2V S1# ≦ 0.2V, S2 ≧ Vcc - 0.2V BYTE# ≧ Vcc - 0.2V or ≦ 0.2V, A19 ≧ Vcc - 0.2V or ≦ 0.2V other inputs = 0 ~ Vcc | ~ +70°C | - | - | 40 | |
| | | | ~ +85°C | - | - | 80 | |
| Icc4 | Stand by supply current (AC,TTL level) | BC1# and BC2# =VIH or S1# =VIH or S2=VIL BYTE# ≧ Vcc - 0.2V or ≦ 0.2V, A19 =VIH or VIL Other inputs= 0 ~ Vcc | | - | - | 2.0 | mA |

* -1.0V in case of AC (Pulse width ≦ 30ns)

Note 3: Direction for current flowing into IC is indicated as positive (no mark)

Note 4: Typical parameter indicates the value for the center of distribution at 3.0V, and not 100% tested.

## CAPACITANCE (Ta=-40~+85°C Vcc=2.7V~3.6V,unless otherwise noted)

| Symbol | Parameter | Conditions | Limits Min | Limits Typ | Limits Max | Units |
|---|---|---|---|---|---|---|
| $C_I$ | Input capacitance | $V_I$=GND, $V_I$=25mVrms, f=1MHz | | | 20 | pF |
| $C_O$ | Output capacitance | $V_O$=GND, $V_O$=25mVrms, f=1MHz | | | 20 | |

## AC ELECTRICAL CHARACTERISTICS (Ta=-40~+85ºC, Vcc=2.7V~3.6V, unless otherwise noted)

### (1) TEST CONDITIONS

| | |
|---|---|
| Supply voltage | 2.7~3.6V |
| Input pulse | $V_{IH}$=2.7V, $V_{IL}$=0.2V |
| Input rise time and fall time | 5ns |
| Reference level | $V_{OH}$=$V_{OL}$=1.5V Transition is measured ±200mV from steady state voltage.(for ten,tdis) |
| Output loads | Fig.1,CL=30pF<br>CL=5pF (for ten,tdis) |

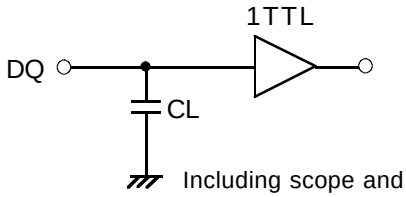



Fig.1 Output load

### (2) READ CYCLE

| Symbol | Parameter | Limits 70HI Min | Limits 70HI Max | Units |
|---|---|---|---|---|
| $t_{CR}$ | Read cycle time | 70 | | ns |
| $t_a$(A) | Address access time | | 70 | ns |
| $t_a$(S1) | Chip select 1 access time | | 70 | ns |
| $t_a$(S2) | Chip select 2 access time | | 70 | ns |
| $t_a$(BC1) | Byte control 1 access time | | 70 | ns |
| $t_a$(BC2) | Byte control 2 access time | | 70 | ns |
| $t_a$(OE) | Output enable access time | | 35 | ns |
| $t_{dis}$(S1) | Output disable time after S1# high | | 25 | ns |
| $t_{dis}$(S2) | Output disable time after S2 low | | 25 | ns |
| $t_{dis}$(BC1) | Output disable time after BC1# high | | 25 | ns |
| $t_{dis}$(BC2) | Output disable time after BC2# high | | 25 | ns |
| $t_{dis}$(OE) | Output disable time after OE# high | | 25 | ns |
| $t_{en}$(S1) | Output enable time after S1# low | 10 | | ns |
| $t_{en}$(S2) | Output enable time after S2 high | 10 | | ns |
| $t_{en}$(BC1) | Output enable time after BC1# low | 5 | | ns |
| $t_{en}$(BC2) | Output enable time after BC2# low | 5 | | ns |
| $t_{en}$(OE) | Output enable time after OE# low | 5 | | ns |
| $t_V$(A) | Data valid time after address | 10 | | ns |

### (3) WRITE CYCLE

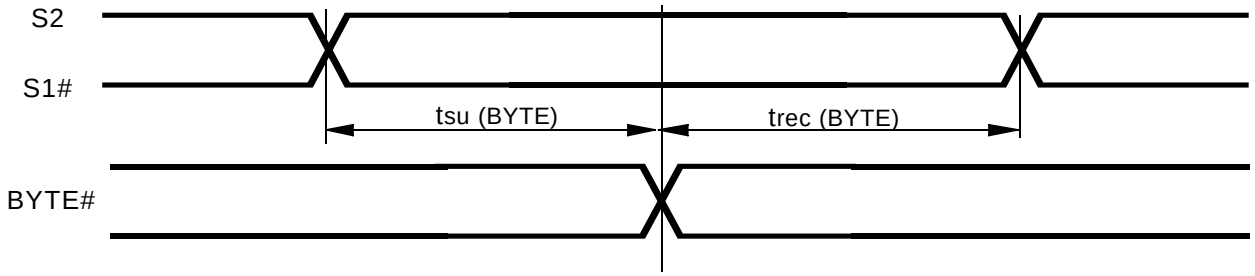
| Symbol | Parameter | Limits 70HI Min | Limits 70HI Max | Units |
|---|---|---|---|---|
| $t_{CW}$ | Write cycle time | 70 | | ns |
| $t_w$(W) | Write pulse width | 55 | | ns |
| $t_{su}$(A) | Address setup time | 0 | | ns |
| $t_{su}$(A-WH) | Address setup time with respect to W# | 65 | | ns |
| $t_{su}$(BC1) | Byte control 1 setup time | 65 | | ns |
| $t_{su}$(BC2) | Byte control 2 setup time | 65 | | ns |
| $t_{su}$(S1) | Chip select 1 setup time | 65 | | ns |
| $t_{su}$(S2) | Chip select 2 setup time | 65 | | ns |
| $t_{su}$(D) | Data setup time | 35 | | ns |
| $t_h$(D) | Data hold time | 0 | | ns |
| $t_{rec}$(W) | Write recovery time | 0 | | ns |
| $t_{dis}$(W) | Output disable time from W# low | | 25 | ns |
| $t_{dis}$(OE) | Output disable time from OE# high | | 25 | ns |
| $t_{en}$(W) | Output enable time from W# high | 5 | | ns |
| $t_{en}$(OE) | Output enable time from OE# low | 5 | | ns |

## (4) Byte# function

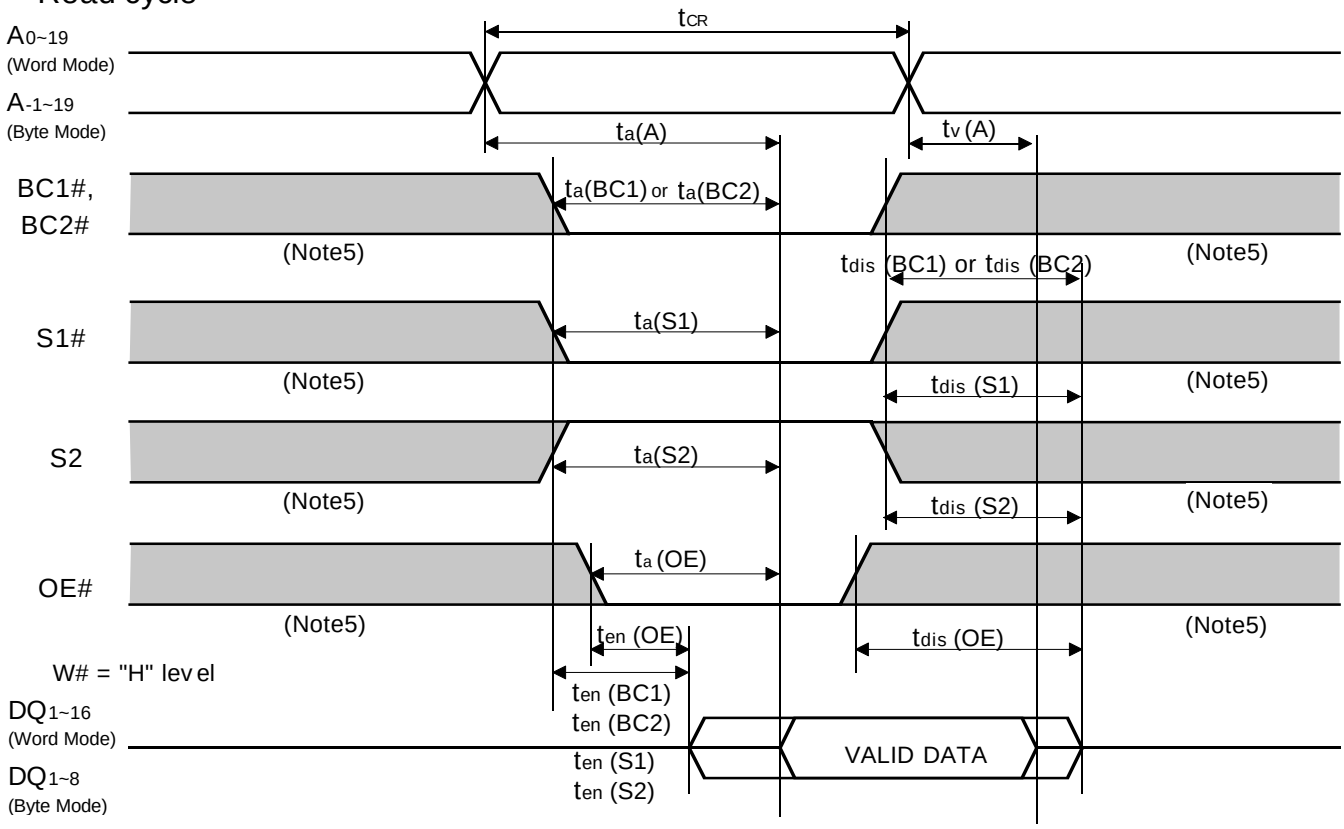
| Symbol | Parameter | Test conditions | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $t_{su\ (BYTE)}$ | / BYTE set up time | | 5 | | | ms |
| $t_{rec\ (BYTE)}$ | / BYTE recovery time | | 5 | | | ms |

## (5) TIMING DIAGRAMS

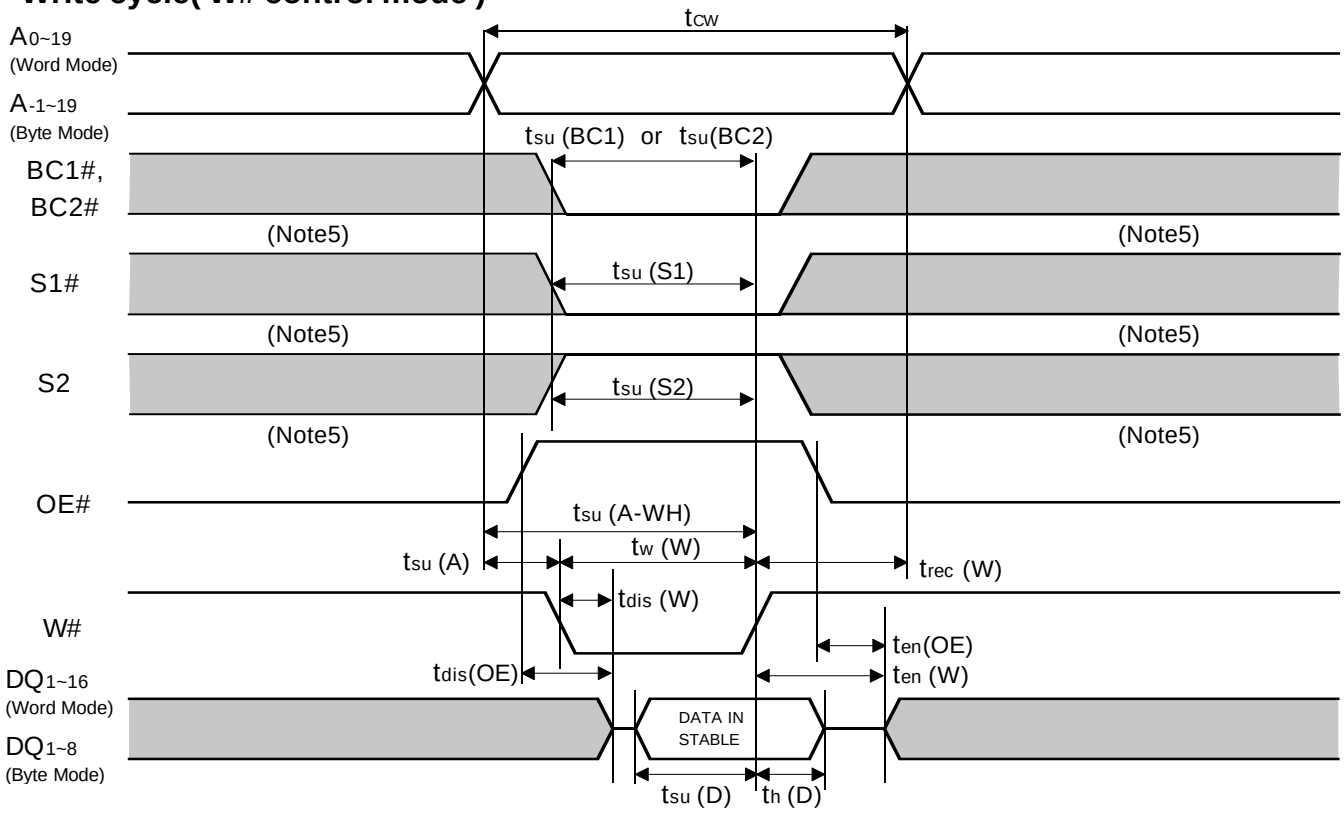
BYTE#



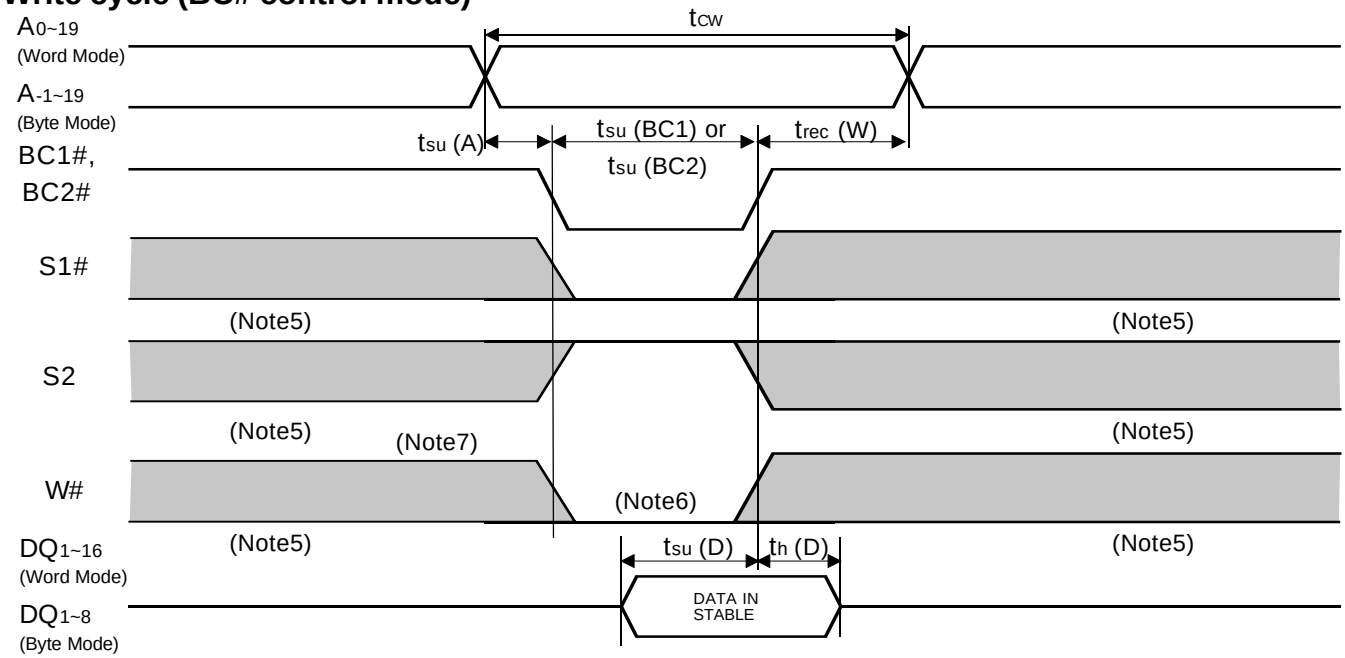

Read cycle



## Write cycle( W# control mode )

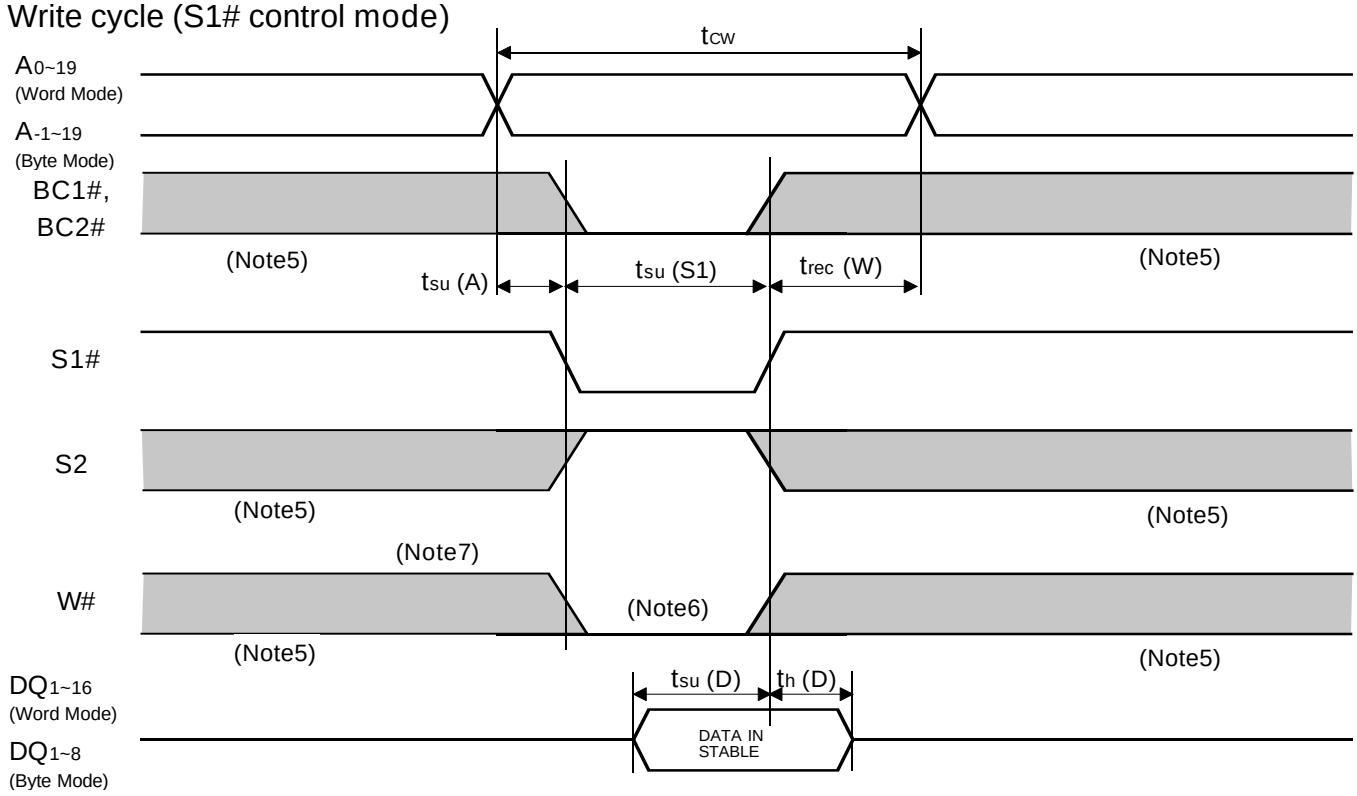



## Write cycle (BC# control mode)

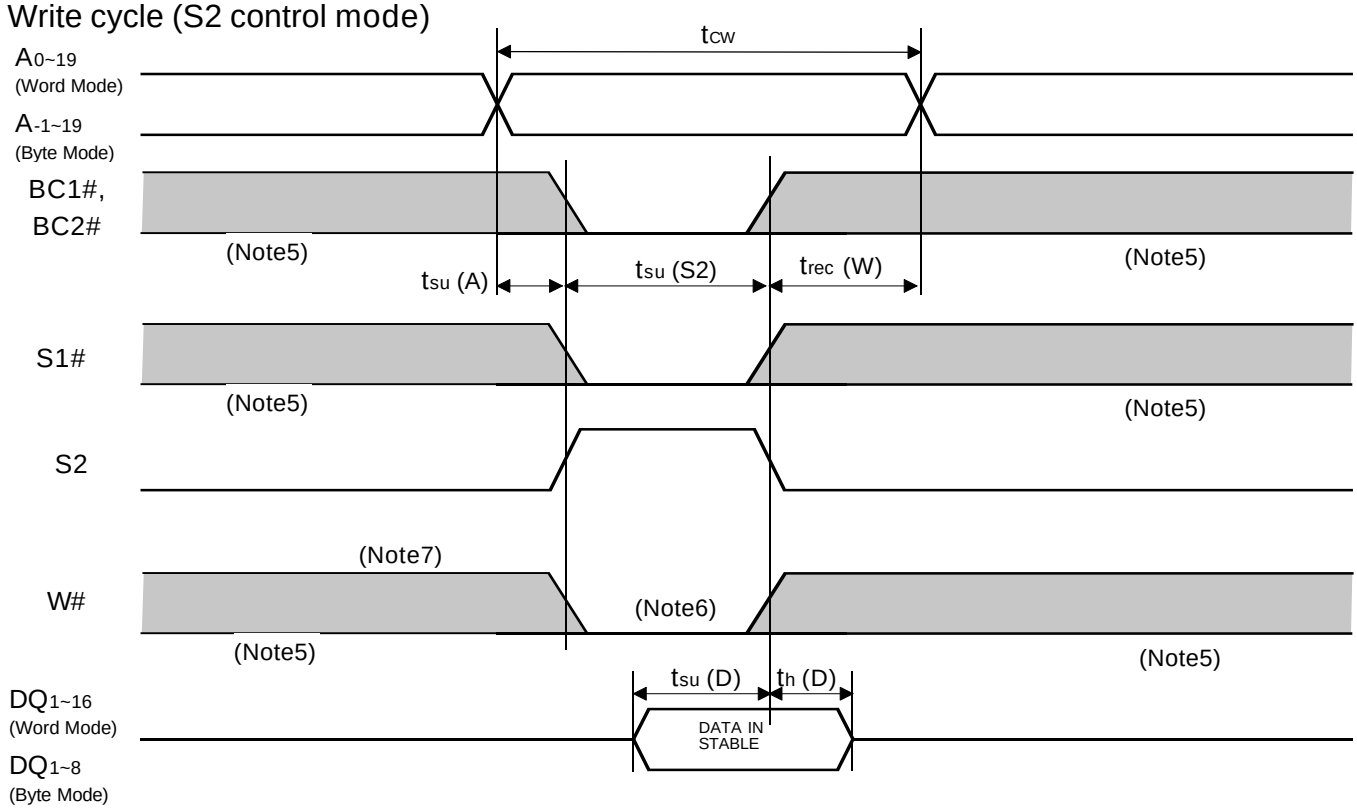



Note 5: Hatching indicates the state is "don't care".
Note 6: A Write occurs during S1# low, S2 high overlaps BC1# and/or BC2# low and W# low.
Note 7: When the falling edge of W# is simultaneously or prior to the falling edge of BC1# and/or BC2# or the falling edge of S1# or rising edge of S2, the outputs are maintained in the high impedance state.
Note 8: Don't apply inverted phase signal externally when DQ pin is in output mode.

Write cycle (S1# control mode)




Write cycle (S2 control mode)



## POWER DOWN CHARACTERISTICS

### (1) ELECTRICAL CHARACTERISTICS (Ta=-40~85ºC, Vcc=2.7V~3.6V,unless otherwise noted)

| Symbol | Parameter | Test conditions | | Limits Min | Limits Typ | Limits Max | Units |
|---|---|---|---|---|---|---|---|
| Vcc (PD) | Power down supply voltage | | | 2.0 | | | V |
| VI (BC) | Byte control input BC1# & BC2# | | | 2.0 | | | V |
| VI (S1#) | Chip select input S1# | | | 2.0 | | | V |
| VI (S2) | Chip select input S2 | | | | | 0.2 | V |
| Icc (PD) | Power down supply current | **Vcc=2.0V** (1) S1# ≥ Vcc - 0.2V, BYTE# ≥ Vcc - 0.2V or ≤ 0.2V other inputs = 0 ~ Vcc (2) S2 ≤ 0.2V , BYTE# ≥ Vcc - 0.2V or ≤ 0.2V other inputs = 0 ~ Vcc (3) BC1# and BC2# ≥ Vcc - 0.2V S1# ≤ 0.2V, S2 ≥ Vcc - 0.2V BYTE# ≥ Vcc - 0.2V or ≤ 0.2V other inputs = 0 ~ Vcc | ~ +25°C | - | 0.2 | 3.0 | µA |
| | | | ~ +40°C | - | 0.4 | 6.0 | |
| | | | ~ +70°C | - | - | 30 | |
| | | | ~ +85°C | - | - | 60 | |

Note 9: Typical parameter of Icc(PD) indicates the value for the center of distribution at 2.0V, and not 100% tested.

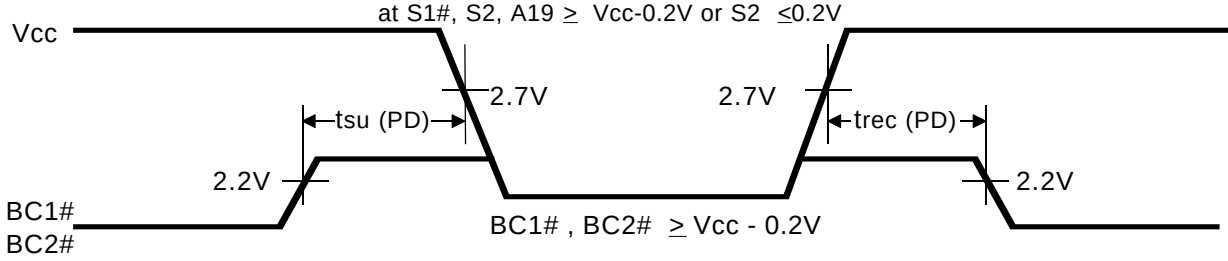
### (2) TIMING REQUIREMENTS

| Symbol | Parameter | Test conditions | Limits Min | Limits Typ | Limits Max | Units |
|---|---|---|---|---|---|---|
| tsu (PD) | Power down set up time | | 0 | | | ns |
| trec (PD) | Power down recovery time | | 5 | | | ms |

### (3) TIMING DIAGRAM

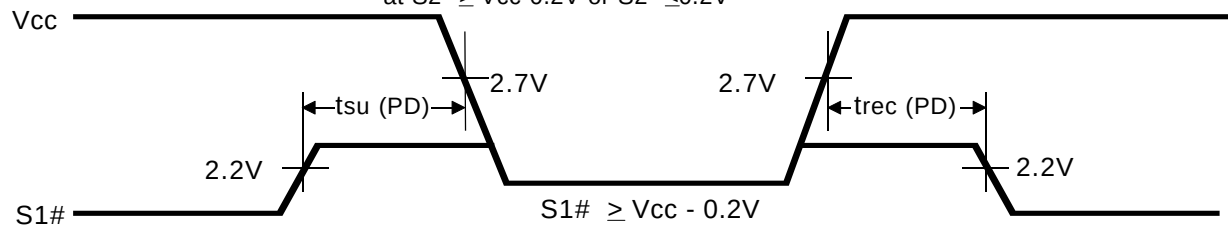
**BC# control mode**

note10:On the BC# control mode, the level of S1# and S2 must be fixed at S1#, S2, A19 ≥ Vcc-0.2V or S2 ≤0.2V

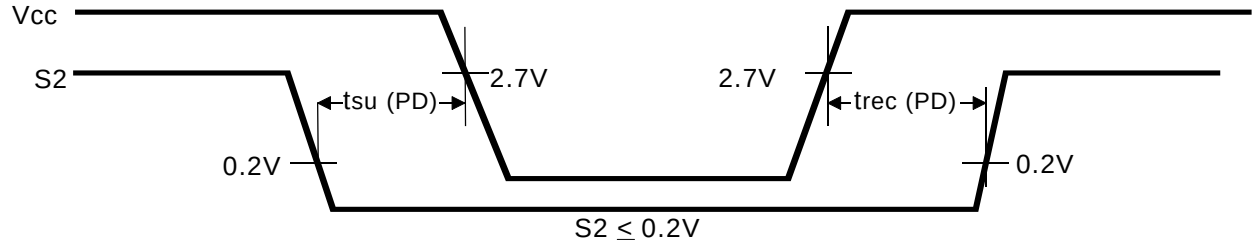



**S1# control mode**

note11:On the S1# control mode, the level of S2 must be fixed at S2 ≥ Vcc-0.2V or S2 ≤0.2V




**S2 control mode**



Jan.10,2003 Ver. 2.1

# M5M5J167KT - 70HI

16777216-BIT (1048576-WORD BY 16-BIT / 2097152-WORD BY 8-BIT) CMOS STATIC RAM

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