M61280M8-xxxFP

NTSC TV Signal Processor with MCU

REJ03F0053-0100Z
Rev.1.0
Sep.23.2003

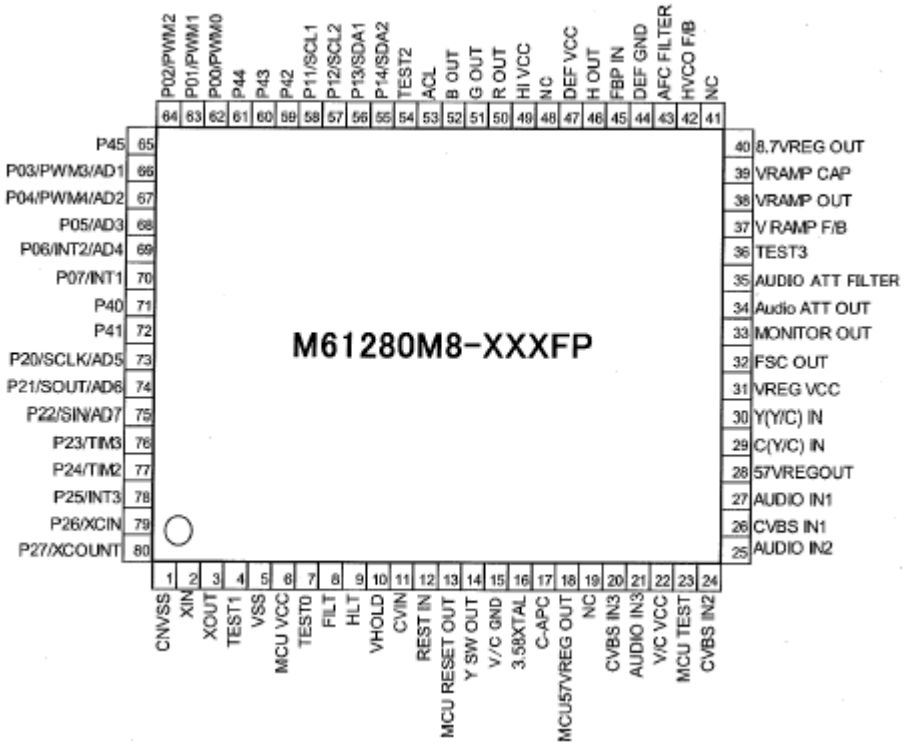
Features

- 3 line composite video signal inputs and 1 line S video signal input are available
- Built-in 3 input audio switch with ATT output
- Correspond to digital OSD
- H output of emitter follower type (L at stopping, same as M61250BFP)
- Selectable of ACL/ABCL
- Built-in H OSC resonator
- Built-in vertical saw tooth generator
- Correspond to fsc clock output
- Built-in 5V & 8V regulator
- Built-in MCU reset circuit
- Built-in 8bit MCU
- ROM: 32kByte, RAM: 1152byte

Applications

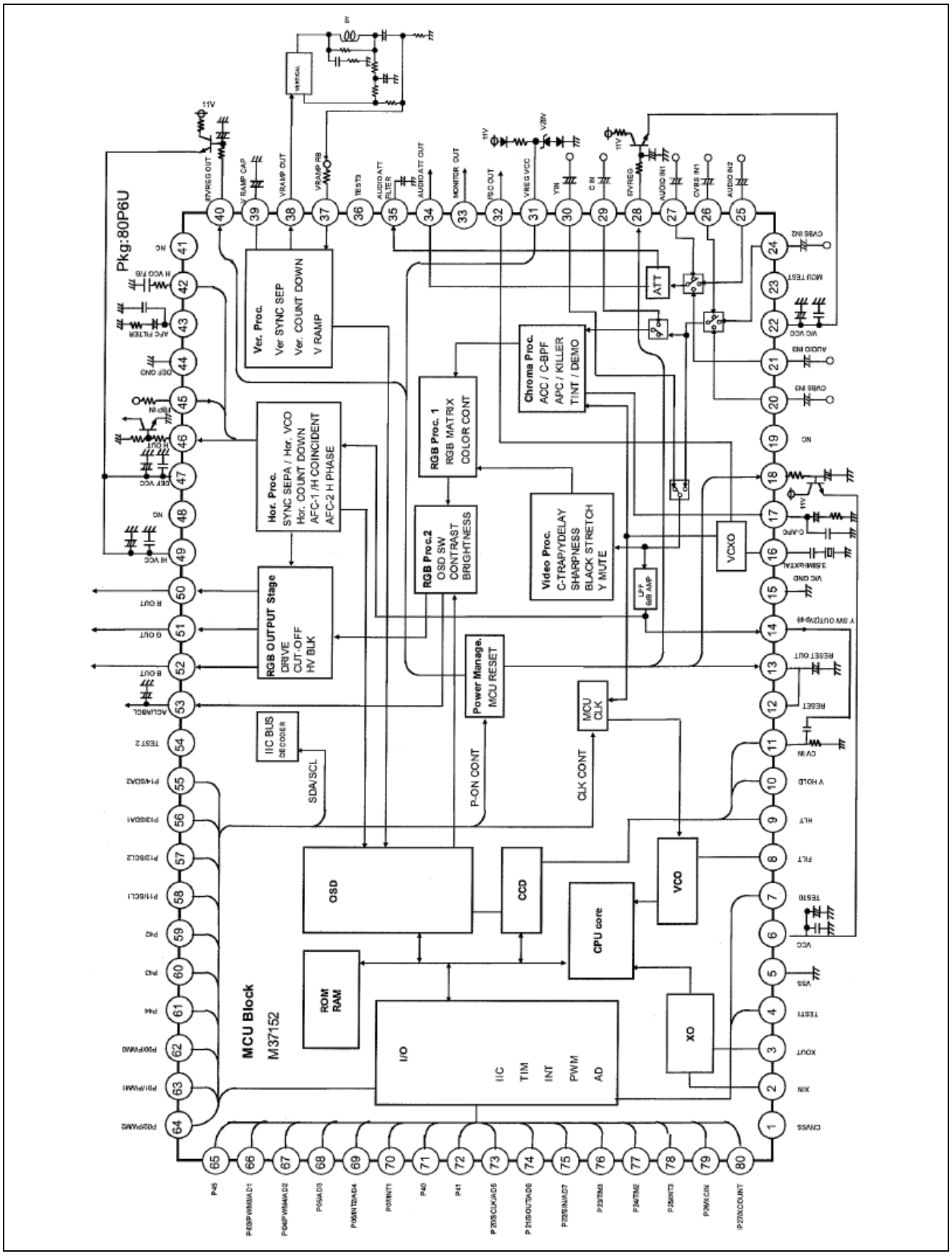
- NTSC color television receivers

Pin Configuration



Package: 80P6U

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Condition	Ratings	Unit
Power supply voltage (ASIC)	Vcc (ASIC)		6.0, 10.0	V
Power supply voltage (MCU)	Vcc (MCU)	Measured with reference to pin Vss. Output transistor in shut-off state.	–0.3 to 6	V
Input voltage (MCU: CNVSS)	VI (MCU)		–0.3 to VCC+0.3	V
Input voltage (MCU: P00 to P07, P11 to P14, P20 to 27, P40 to P45, RESET, CVIN)	V_I (MCU)		–0.3 to VCC+0.3	V
Output voltage (MCU: P00 to P07, P11 to P14, P20 to 27, P40, P41)	V_O (MCU)		–0.3 to VCC+0.3	V
Circuit current (MCU: P11 to P14, P20 to P27, P40, P41)	I_{OH} (MCU)		0 to 1 (Note 1)	mA
Circuit current (MCU: P00 to P07, P20 to P23, P40, P41)	I_{OL1} (MCU)		0 to 2 (Note 2)	mA
Circuit current (MCU: P11 to P14)	I_{OL2} (MCU)		0 to 6 (Note 2)	mA
Circuit current (MCU: P24 to P27)	I_{OL3} (MCU)		0 to 10 (Note 2)	mA
Power dissipation	Pd	Ta = 25°C	2000	mW
Thermal reduction	Kt		20	mW/°C
Operating ambient temperature	Topr		–10 to 65	°C
Storage temperature	Tstg		–40 to 125	°C

Notes: 1. The sum of currents flowing from the IC should not exceed 20 mA.
2. The sum of currents flowing into the IC (IOL1+IOL2) should not exceed 30 mA.
3. Pin names for the different quantities are given as follows.
(1) Dedicated pins: Dedicated pin name
(2) Double/triple-function ports
*When standards are the same: I/O port name
*When standard of functions other than the I/O port are different: function pin name

Recommended Operating Conditions

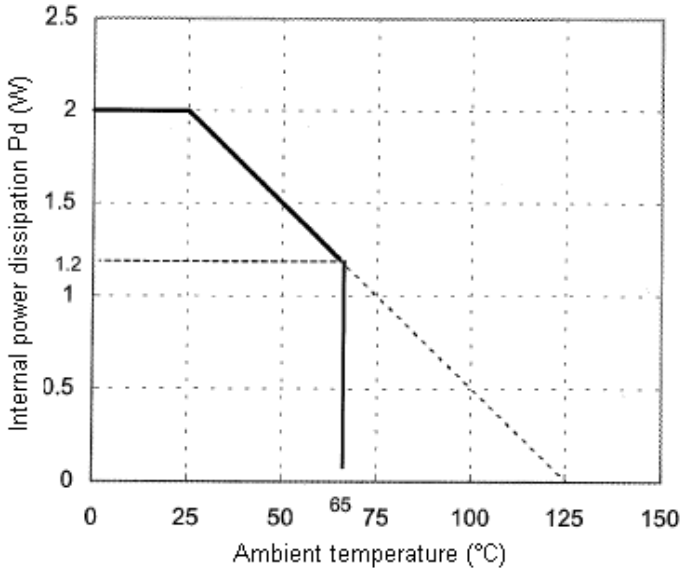
Item	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage (MCU) (Note 1)	VDD(MCU)	4.75	5.0	5.25	V
Power supply voltage1 (ASIC: Pin22)	Vcc1(ASIC)	4.75	5.0	5.25	V
Power supply voltage2 (ASIC: Pin47)	Vcc2(ASIC)	7.6	8.0	8.4	V
Power supply voltage3 (ASIC: Pin49)	Vcc3(ASIC)	7.6	8.0	8.4	V
Power supply voltage4 (ASIC: Pin31)	Vcc4(ASIC)	8.3	8.7	9.1	V
Power supply voltage (MCU)	VSS	0	0	0	V
""H" input voltage (MCU: P00 to P07, P11 to P14, P20 to P27, P40 to P45, RESET)	V_{IH1}	$0.8V_{DD}$	—	V_{DD}	V
"H" input voltage (MCU: SCL1, SCL2, SDA1, SDA2)(using I^2C-BUS)	V_{IH2}	$0.7V_{DD}$	—	V_{DD}	V
"L" input voltage (MCU: P00 to P07, P11 to P14, P20 to P27, P40 to P45)	V_{IL1}	0	—	$0.4V_{DD}$	
"L" input voltage (MCU: SCL1, SCL2, SDA1, SDA2)(using I^2C-BUS)	V_{IL2}	0	—	$0.3V_{DD}$	V
"L" input voltage (Note 2) (MCU: RESET, TIM3, INT1, INT2, INT3, S_{IN}, S_{CLK})	V_{IL3}	0	—	$0.2V_{DD}$	V
"H" output average current (Note 3) (MCU:P10 to P16, P20 to 27)	I_{OH}	—	—	1	mA

Recommended Operating Conditions (cont.)

Item	Symbol	Min.	Typ.	Max.	Unit
"L" output average current (Note 4) (MCU:P00 to P14, P20 to P23)	I_{OL1}	—	—	2	mA
"L" output average current (Note 4) (MCU:P11 to P14)	I_{OL2}	—	—	6	mA
"L" output average current (Note 5) (MCU:P24 to P27)	I_{OL3}	—	—	10	mA
Oscillation frequency (CPU operation) (Note 6) (MCU: X_{IN})	$f(X_{IN})$	7.9	8.0	8.1	MHz
Oscillation frequency (subclock operation) (MCU: X_{CIN})	$f(X_{CIN})$	29	32	35	kHz
Input frequency (MCU:TIM3, INT1, INT2,.INT3)	fhs 1	—	—	100	kHz
Input frequency (MCU: SCLK)	fhs 2	—	—	1	MHz
Input frequency (MCU: SCL1,SCL2)	hs 3	—	—	400	kHz
Input amplitude (MCU: TV video signal CVIN)	VI	1.5	2.0	2.5	V

Notes:
1. In order to eliminate power supply noise, a 0.1 μF or greater capacitor should be connected externally across power supply pins VDD and VSS. In addition, a 0.1 μF or greater capacitor should also be connected across VDD and CNVSS. (The recommended crystal oscillator is Murata model no. CSA8.00MTZ (8.00 MHz), shown in the measurement circuit diagram.)
2. Pin names for the different quantities are given as follows.
   (1) Dedicated pins: Dedicated pin name
   (2) Double/triple-function ports
   *When standards are the same: I/O port name
   *When standard of functions other than the I/O port are different: function pin name
3. The sum of currents flowing from the IC should not exceed 20 mA.
4. The sum of currents flowing into the IC (IOL1+IOL2) should not exceed 30 mA.
5. The sum of the average currents of ports P24 to P27 flowing into the IC should not exceed 20 mA.
6. When using a CPU oscillation circuit (XIN, XOUT), a crystal oscillator or a ceramic resonator should be used.

Thermal Derating (Maximum Rating)



I²C Bus Table

1. Slave Address = BAH (WRITE), BBH (READ)

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	1	1	1	0	1	1/0

2. Write Table (input bytes)

SUB ADDRESS		DATA								INITIAL	
HEX	BIN	D7	D6	D5	D4	D3	D2	D1	D0	HEX	DEC
00H	00000000	OSD Clip OFF		Contrast Control							
		V0	V1	V0	V0	V0	V0	V0	V0	40H	64
01H	00000001	Brightness Control									
		V1	V0	V0	V0	V0	V0	V0	V0	80H	128
02H	00000010	FORCE MONO	Drive(R)								
		0	1	0	0	0	0	0	0	40H	64
03H	00000011	White Back	Drive(B)								
		0	1	0	0	0	0	0	0	40H	64
04H	00000100	Cut Off(R)									
		1	0	0	0	0	0	0	0	80H	128
05H	00000101	Cut Off(G)									
		1	0	0	0	0	0	0	0	80H	128
06H	00000110	Cut Off(B)									
		1	0	0	0	0	0	0	0	80H	128
07H	00000111	ACL OFF	Fsc-Free	ABCL	ABCL Gain	TRAP OFF	HTONE	Killer Level	TAKE OFF		
		0	0	0	0	0	0	0	0	00H	0
08H	00001000	BGP FBP OFF	Tint Control								
		0	V1	V0	V0	V0	V0	V0	V0	40H	64
09H	00001001	Blue Back	Color Control								
		V0	V1	V0	V0	V0	V0	V0	V0	40H	64
0AH	00001010	Video Mute	HV BLK OFF	Video Tone							
		0	0	V1	V0	V0	V0	V0	V0	20H	32
0BH	00001011	Black Stre. Off	Black Stretch CONT			FASTBLK H	VIDEO SW				
		0	0	0	0	0	V0	V0	V0	00H	0
0CH	00001100	V.1Widows	Not Assigned		C.Angle 95	YSW LPF	Y DL Fine Adj	Y DL Time Adj			
		0	1	0	0	0	0	0	0	00H	64
0DH	00001101	SERVICE	Slice Det Down	S.Slice Down		TEST	V Shift				
		0	1	0	0	0	0	0	0	40H	64
0EH	00001110	V Out Stop	V-Free	V-Size							
		1	0	1	0	0	0	0	0	A0H	160
0FH	00001111	H Start	H-Free	Not Assigned	AFC2 Gain Down	AFC2 H Phase					
		0	0	0	0	1	0	0	0	08H	8
10H	00010000	Audio Mute	Audio ATT								
		0	0	0	0	0	0	0	0	00H	0
11H	00010001	Monitoring				Not Assigned	TEST	AUDIO SW			
		0	0	0	0	0	0	0	0	08H	0
12H	00010010	TEST	TEST	TEST		Vsync Det Time	AFC1 GAIN				
		0	0	0	0	0	1	0	0	04H	4
1CH	00011100	TEST		TEST	MCU VCOUT	HPMSB	HVCO ADJ				
		0	0	0	1	0	1	0	0	14H	20
1DH	00011101	TEST 1	TEST 0	TEST ON	Not Assigned	Black Discharge2	FORCE COLOR	C-TRAP ADJ			
		0	0	0	0	0	0	0	0	03H	0
1EH	00011110	Not Assigned					C-SYNC ADJ.				
		0	0	0	0	0	0	0	0	00H	0
1FH	00011111	HBLK STOP	VBLK STOP	Not Assigned	Not Assigned	OSD BRIGHT	IM MSB	HVCO REF OFF	HVCO OFF		
		0	0	0	0	0	0	0	0	00H	0

NOTE: V0/V1->V-LATCH BIT

If it needs to write any data on TEST bit, the initial data : 0 is requested.

3. Read Table (output byts)

D7	D6	D5	D4	D3	D2	D1	D0
KILLERB	2WIN WIDEB	VFREEB	VCONIB	0	0	HCOINB	1

4. Bus Functions

- Write

	Function	Bit	Sub Add	DATA	Discription	Initial	Note
Audio	Audio ATT	7	10H	D0-D6	Pin 34 audio output level adjustment	00H	
	Audio SW	2	11H	D0-D1	Audio input switching; 0: Audio 1, 1: Audio 2, 2: Audio 3	X0H	
	Audio Mute	1	10H	D7	Pin 34 audio output on/off (mute) switching; 0: audio on (non-muted), 1: mute	0	
Video	Video Tone	6	0AH	D0-D5	Sharpness level control	20H	V Latch
	Contrast Control	7	00H	D0-D6	Contrast level control	40H	V Latch
	OSD Contras Clip	1	00H	D7	OSD (EXT RGB) contrast lower-limit clipping on/off; 0: clipping on, 1: clipping off	0	V Latch
	Y DL Time Adj	2	0CH	D0-D1	Y signal delay adjustment	X0H	
	Y DL Fine Adj	1	0CH	D2	Y signal delay fine adjustment	0	
	Vidio SW	3	0BH	D3	Video input pins 26/24/20/30 switching; 0: pin 26, 1: pin 24, 2: pin 20, 3: pin 30	X0H	V Latch
	Y SW LPF	1	0CH	D3	Pin 14 (Y SW OUT) output f-characteristic switching; 0: flat, 1: LPF (fc = 700 kHz)	0	
	Vidio Mute	1	0AH	D7	Y signal output on/off (mute) switching; 0: mute off, 1: mute	0	
	TRAP Off	1	07H	D3	Y signal chroma trap on/off switching; 0: trap on, 1: trap off	0	
	C-TRAP Adj	2	1DH	D0-D1	Chroma trap frequency fine adjust	X0H	
	Black Stretch Off	1	0BH	D7	Black stretch circuit on/off switching; 0: black stretch on, 1: black stretch off	0	
	Black Stretch Cont	3	0BH	D4-D6	Black stretch charge, discharge time constant adjustment; D4, D5: charge time constant adjustment; D6: discharge time constant adjustment	0XH	
	Black Dicharge2	1	1DH	D3	Black stretch discharge time constant adjustment; discharge time constant adjustment	0XH	
CHROMA	Tint Control	7	08H	D0-D6	Hue control	40H	V Latch
	Color Control	7	09H	D0-D6	Color level control	40H	V Latch
	Take Off	1	07H	D0	Chroma BPF take-off function on/off switching; 0: BPF; 1: take off	0	
	C Angle95	1	0CH	D4	Color demodulation angle switching; 0: 103 deg, 1: 95 deg	0	
	Killer Level	1	07H	D1	Colorkiller sensitivity switching (active shallow direction); 0: 40 dB, 1: 35 dB	0	
	Force Mono	1	02H	D7	Forced b/w mode; 0: normal; 1: b/w	0	
	Force Color	1	1DH	D2	Forced color mode; 0: normal; 1: color	0	
	Fsc Free	1	07H	D6	X'tal oscillation circuit forced free-running mode; 0: off, 1: free-running	0	
RGB	Brightness Control	8	01H	D0-D7	Bright level control	80H	V Latch
	Drive (R)	7	02H	D0-D6	R output level control	40H	
	Drive (B)	7	03H	D0-D6	B output level control	40H	
	Cut Off (R)	8	04H	D0-D7	R output DC level control	80H	
	Cut Off (G)	8	05H	D0-D7	G output DC level control	80H	
	Cut Off (B)	8	06H	D0-D7	B output DC level control	80H	
	Blue Back	1	09H	D7	Blue back screen on/off switching; 0: off, 1: blue back	0	
	WhiteBack	1	03H	D7	White raster on/off switching; 0: off, 1: white back	0	
	ABCL	1	07H	D5	ABCL on/off switching; 0: off, 1: ABCL on	0	
	ABCL Gain	1	07H	D4	ABCL sensitivity low/high switching; 0: low, 1: hi	0	
	OSD Bright	1	1FH	D3	OSD level switching; 0: normal, 1: –8%	0	
	ACL OFF	1	07H	D7	ACL on/off switching; 0: normal, 1: ACL max	0	
	HTONE	1	07H	D2	Halftone on/off switching; 0: normal, 1: halftone	0	
	FASTBLK Hi	1	0BH	D3	FASTBLK switching; 0: normal, 1: hi (full-screen OSD mode)	0	

- Write (cont.)

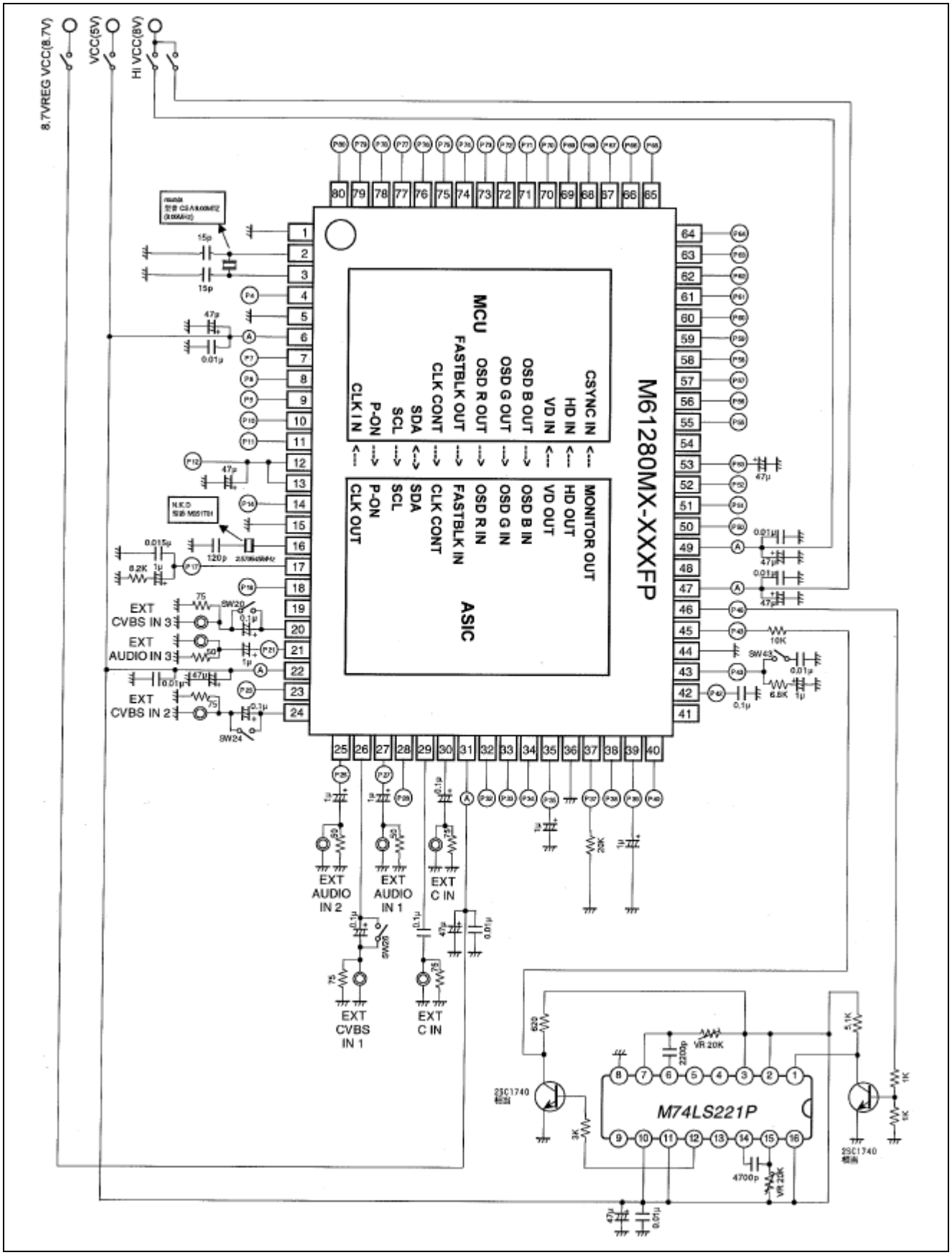
	Function	Bit	Sub Add	DATA	Discription	Initial	Note
DEF	AFC2 H Phase	4	0FH	D0-D3	Screen horizontal position adjustment	X8H	
	V Out Stop	1	0EH	D7	Pin 38 VOUT (ramp) forced stop mode (when stopped, pin 38 at DC GND level); 0: VOUT, 1: STOP	0	
	Service SW	1	0DH	D7	Vertical output on/off switching; 0: vertical output on, 1: vertical output off	0	
	H Start	1	0FH	D7	Horizontal output out/stop switching; 0: stop, 1: H out	0	
	AFC1 Gain	3	12H	D0-D2	Horizontal AFC gain adjustment; 000: low to 111: hi	X4H	
	AFC2 Gain Down	1	0FH	D4	Horizontal AFC2 gain high/low switching; 0: high, 1: low	0	
	H VCO Adj	3	1CH	D0-D2	H VCO free-running frequency adjustment	X4H	
	V Shift	3	0DH	D0-D2	Vertical ramp start timing adjustment	X0H	
	V-Size	6	0EH	D0-D5	Vertical ramp amplitude adjustment	20H	
	H-free	1	0FH	D6	Horizontal output forced free-running mode on/off switching; 0: off, 1: horizontal free-running	0	
	V-free	1	0EH	D6	Vertical output forced free-running mode on/off switching; 0: off, 1: vertical free-running	0	
	S Slice Down	2	0DH	D4-D5	Sync detection slice level switching (0: 50%, 1: 30%, 2: 40%, 3: 25%)	0XH	
	Slice Det Down	1	0DH	D6	0: normal, 1: lower sync detection sensitivity (end of video signal only)	0	
	HV BLK OFF	1	0AH	D6	Horizontal/vertical blanking on/off switching; 0: blanking on, 1: blanking off	0	
	V SYNC DET TIME	1	12H	D3	Vertical minimum sync detection width switching; 0: sync detect width =18 μs, 1: sync detect width =14 μs	0	
	V1 Window	1	0CH	D7	Vertical sync detection switching (1 window/2 windows); 0: 2 windows, 1: 1 window	0	
	BGPFBP OFF	1	08H	D7	Internal BGP on/off switching when no FBP input; 0: BGP on, 1: BGP off	0	
	C-SYNC Adj	3	1EH	D0-D2	C-sync output LPF cutoff frequency adjustment	X0H	
	Monitoring	4	11H	D4-D7	Pin 18 intelligent monitor mode switching	0XH	

- Read

HCONB	1	00H	D1	Horizontal sync detection; "1" when asynchronous
—	1	00H	D2	0
—	1	00H	D3	0
VCOINB	1	00H	D4	Vertical sync detection; "1" when asynchronous
VFREEB	1	00H	D5	V free-running mode; 0: V free-running, 1: V lock
2WIN WIDEB	1	00H	D6	Vertical 2-window detection; 0: wide window, 1: narrow window
KILLERB	1	00H	D7	Colorkiller information output; "1" when killer off

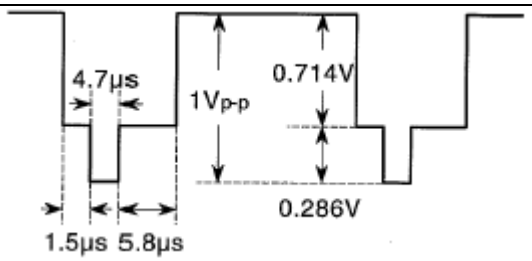
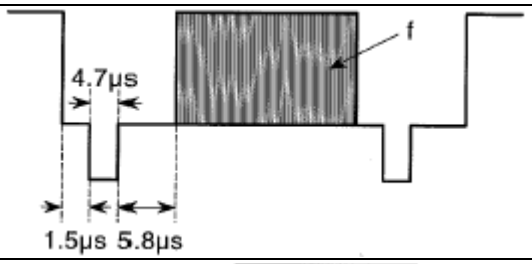
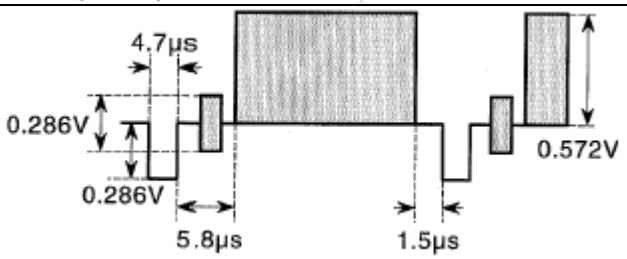
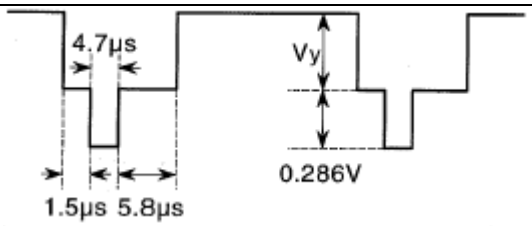
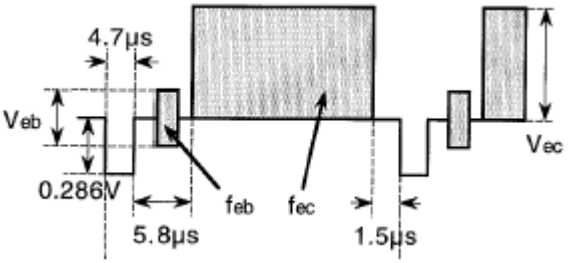
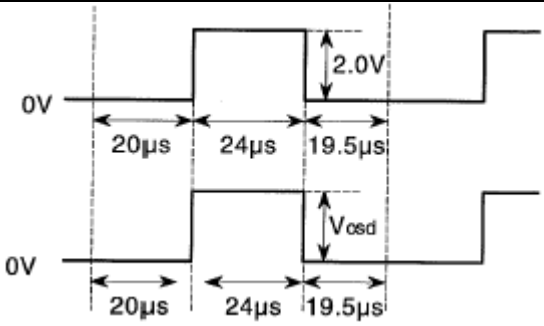
Note: Functions not listed in this bus function table are used only in testing, and operation is not guaranteed.

Test Circuit

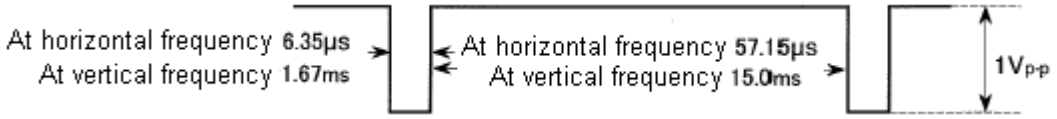
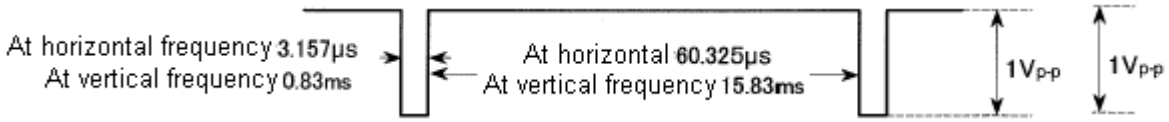
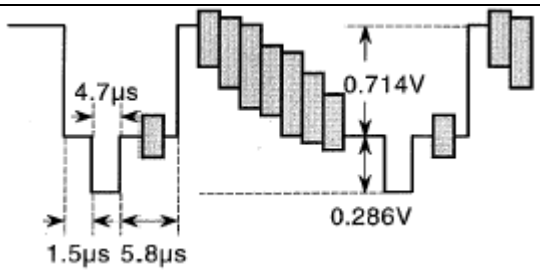


Input Signals

1. Video/Chroma/RGB/DEF Block

SG No.	Signal Description (75 Ω termination)	
SG. A	NTSC format APL 100% standard video signal. Vertical signal is interlaced at 60 Hz.	
SG. B	In the SG.A signal, the Lumi. signal frequency and amplitude can be changed. However, standard amplitude is 0.714 Vp-p. In the figure on the right, the Lumi. signal is represented by f.	
SG. C	NTSC standard monochrome video signal. Vertical signal is interlaced at 60 Hz.	
SG. D	NTSC format video signal; APL variable. Vertical signal is interlaced at 60 Hz.	
SG. E	NTSC format monochrome video signal. In the SG.C signal, the burst and chroma part frequency and amplitude can be changed. Vertical signal is interlaced at 60 Hz. (Standard state: Veb = 0.286 V, Vec = 0.572 V, feb = fec = 3.579545 MHz)	
SG. F	Fast blanking signal; synchronized with video input signal. External RGB (OSD) signal; synchronized with video input signal and blanking signal.	

1. Video/Chroma/RGB/DEF Block (cont.)

SG No.	Signal Description (75 Ω termination)
SG.G	NTSC format rainbow color bar video signal. Vertical signal is interlaced at 60 Hz.
SG. H	Duty 90%, variable frequency, variable level. (Standard horizontal frequency = 15.734 kHz, vertical frequency = 60 Hz, 1 Vp-p) 
SG. I	Duty variable (standard 95%), frequency variable, level variable (Standard: horizontal frequency = 15.734 kHz, vertical frequency = 60 Hz, 1 Vp-p) 
SG. J	NTSC format standard color bar video signal; vertical signal is interlaced at 60 Hz. 
SG. K	NTSC format, standard 8-step wave signal; vertical signal is interlaced at 60 Hz.
SG. L	NTSC format red raster signal; vertical signal is interlaced at 60 Hz.

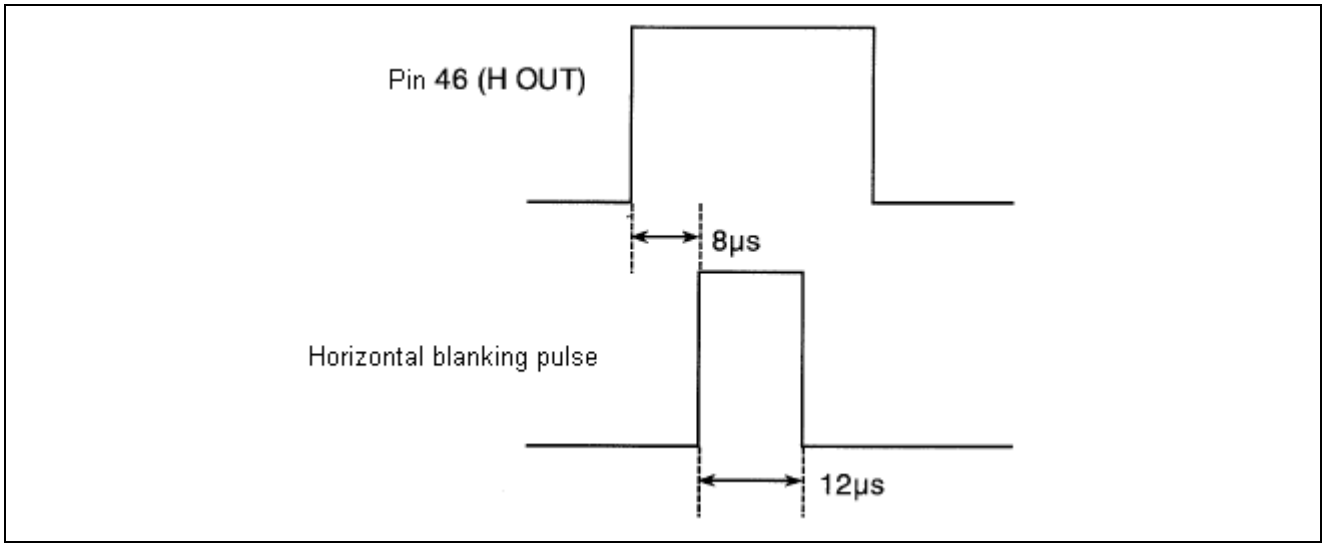
2. Audio Block

SG No.	Signal Description (50 Ω termination)
SG.AU	fo = 400 Hz, 500 mVrms, CW

Setup Instructions for Evaluation PCB

1. Horizontal Blanking Pulse Adjustment

The horizontal blanking pulse timing and pulse width are adjusted using the variable resistances of a one-shot multivibrator, as shown below.



The timing is adjusted to 8 µs using the pin 15 variable resistance of the M74LS221P TTL IC. Also, the pulse width is adjusted to 12 µs using the pin 7 variable resistance.

2. H VCO Adjustment

Prior to measurement of the M61280Mx-xxxFP, the following method is used for H VCO adjustment.

1. The H VCO control I^2C bus data (1 CH D0-D2) is adjusted, and the pin 46 (H OUT) frequency is set to approx. 15.734 kHz.

Electrical Characteristics, ASIC

(Ta = 25°C)

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
ICC	Standard conditions								Pins 4, 7=0 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
ICC5V	5 V circuit current (pin 22)	—	—	22	40	55	70	mA	MCU/VIDEO/Chroma Vcc
ICC8V	8 V circuit current	—	—	47,48, 49	27	42	57	mA	Deflection/RGB Drive 8 V Vcc
ICC12	Pin 47 circuit current	—	—	47	—	23	—	mA	Reference data; Deflection/Vcc
ICC49	Pin 49 circuit current	—	—	49	—	19	—	mA	Reference data; RGB Drive/AUDIO 8 V Vcc
ICC31	Pin 31 circuit current	—	—	31	3	6	9	mA	8.7 VREG Vcc
Power	Power supply circuit standard conditions								Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
Vth9	Power on control threshold voltage	—	—	9	2.6	3	3.4	V	
V40H	8.7 VREG output voltage 1	—	—	40	8.3	8.7	9.1	V	Pin 9 = 5 V
V40L	8.7 VREG output voltage 2	—	—	40	—	0	0.3	V	Pin 9 = 0 V
V28	5.7 VREG output voltage 1	—	—	28	5.55	5.8	6.05	V	Pin 9 = 5 V
V18H1	MCU 5.7 VREG output voltage 1	—	—	18	5.45	5.7.	5.95	V	Pin 9 = 5 V
V18H2	MCU 5.7 VREG output voltage 2	—	—	18	5.45	5.7	5.95	V	Pin 9 = 0 V
Reset	Reset standard conditions								Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
V13H	Maximum reset output voltage	—	—	13	4.5	5	5.5	V	
V13L	Minimum reset output voltage	—	—	13	—	0	0.5	V	
TH9	Reset threshold voltage	—	—	9	4	4.2	4.4	V	
I^2C	I^2C standard conditions	—	—	—	—	—	—	—	
IACK	ACK current	—	—		—	1	—	mA	Reference data
VIL	SCL/SDA VTH (L)	—	—	56,58	0.0	0.75	1.5	V	
VIH	SCL/SDA VTH (H)	—	—	56,58	3.5	4.25	5.0	V	
F_{SCL}	Clock frequency	—	—	56	—	—	100	kHz	

Symbol	Subaddress																									
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
ICC	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
ICC5V																											
ICC8V																											
ICC12																											
ICC49																											
ICC31																											

Power	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
Vth9																											
V40H																											
V40L																											
V28																											
V18H1																											
V18H2																											
Reset	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
V13H																											
V13L																											
TH9																											

I^2C	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
I_{ACK}																											
VIL																											
VIH																											
F_{SCL}																											

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
AUDIO	AUDIO standard conditions								Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
GEAu1	Audio gain1	27	SG.AU	34	–3	0	3	dB	Expressed as 20 log (measured value/input amplitude)
GEAu2	Audio gain2	25	SG.AU	34	–3	0	3	dB	Expressed as 20 log (measured value/input amplitude)
GEAu3	Audio gain3	21	SG.AU	34	–3	0	3	dB	Expressed as 20 log (measured value/input amplitude)
VOL-max	Maximum audio output amplitude	27	SG.AU	34	350	500	720	mVms	
VOL-min	Maximum audio output attenuation	27	SG.AU	34	—	–65	–60	dB	Expressed as 20 log (measured value / input amplitude)

Symbol	Subaddress																									
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
AUDIO	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
GEAu1																	7F										
GEAu2																	7F	01									
GEAu3																	7F	02									
VOL-max																	7F										
VOL-min																											

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
VIDEO	Video standard conditions	—	—	—	—	—	—	—	Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
2AGV1	Video SW1 output level (CVBS1 input)	26	SG.A	14	1.6	2.0	2.6	Vpp	
2AGV2	Video SW2 output level (CVBS2 input)	24	SG.A	14	1.6	2.0	2.6	Vpp	
2AGV3	Video SW3 output level (CVBS3 input)	20	SG.A	14	1.6	2.0	2.6	Vpp	
2AGVY	Video SWY output level (Y/C input)	30	SG.A	14	1.6	2.0	2.6	Vpp	
Ymax	Maximum video output	26	SG.A	50,51, 52	2.9	4.2	5.6	V	
GY	Video gain	26	SG.A	50,51, 52	12	15	18	dB	
FBY	Video frequency characteristic	26	SG.B	50,51, 52	–4	–1	—	dB	f = 5 MHz, C-trap: OFF
CRF1	Chroma trap attenuation 1	26	SG.C	50,51, 52	—	—	–18	dB	
CRF2	Chroma trap attenuation 2	26	SG.L	50,51, 52	—	—	–6.5	dB	
YDL1	YDL time 1	26	SG.A	50,51, 52	190	260	330	ns	
YDL2	YDL time 2	26	SG.A	50,51, 52	100	150	250	Ns	YDL2 = measured value – YDL1 measured value
YDL3	YDL time 3	26	SG.A	50,51, 52	100	150	250	ns	YDL3 = measured value – YDL2 measured value
YDL4	YDL time 4	26	SG.A	50,51, 52	100	150	250	ns	YDL4 = measured value – YDL3 measured value
Gtnor	Video tone control characteristic 1	26	SG.B	50,51, 52	1.0	1.4	1.8	V	f = 2.5 MHz
GTmax	Video tone control characteristic 2	26	SG.B	50,51, 52	7	10	14	dB	f = 2.5 MHz
GTmin	Video tone control characteristic 3	26	SG.B	50,51, 52	–6	–2	2	dB	f = 2.5 MHz
GT2M	Video tone control characteristic 4	26	SG.B	50,51, 52	–1	2	5	DB	f = 2 MHz
GT5M	Video tone control characteristic 5	26	SG.B	50,51, 52	–9	–5	–1	dB	f = 5 MHz
BLS	Black stretch characteristic	26	SG.K	50,51, 52	0.01	0.03	0.05	V	
VMF	Video mute function	26	SG.A	50,51, 52	—	–45	–35	dB	

Symbol	Subaddress																											
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
VIDEO	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
2AGV1													04														
2AGV2												81	04														
2AGV3												82	04														
2AGVY												83	04														
Ymax	7F									00			04														
GY	7F									00			04														
FBY	7F		08							00			04														
CRF1										00			04												02		
CRF2	54				50	50	50			40			04												02		
YDL1										00			04														
YDL2										00			05														
YDL3										00			06														
YDL4										00			07														
GTnor										00			04														
GTmax										00	3F		04														
GTmin										00	00		04														
GT2M										00			04														
GT5M										00			04														
BLS	adj	adj								00		C0/40	04														
VMF	7F									00	80		04														

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
CHROMA	Chroma standard conditions	—	—	—	—	—	—	—	Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
CnorR	Chroma standard output (R-Y)	26	SG.C	33	390	560	790	mVpp	
CnorB	Chroma standard output (B-Y)	26	SG.C	33	640	920	1290	mVpp	
ACC1	ACC characteristic 1	26	SG.E	33	–3	0	3	dB	Veb, Vec: standard input level +6 dB
ACC2	ACC characteristic 2	26	SG.E	33	–6.5	0	1.5	dB	Veb, Vec: standard input level –18 dB
OV	Chroma overload characteristic	26	SG.E	33	–3	2	5	dB	Vec = 800 mV
VikN	Killer operation input level	26	SG.E	33	—	–40	–35	dB	Veb, Vec: variable
KillP	Color remaining on colorkilling	26	SG.E	33	—	–45	–30	dB	Veb = 0 mV
APCU	APC pull-in range (upper)	26	SG.E	33	300	600	—	Hz	feb = fec: variable
APCL	APC pull-in range (lower)	26	SG.E	33	—	–600	–300	Hz	feb = fec: variable
R/BN	Demodulation ratio	26	SG.E	33	0.40	0.57	0.80	—	feb = feb + 50 kHz
R-YN1	Demodulation angle 1	26	SG.E	33	86	103	120	deg	feb = feb + 50 kHz
R-YN2	Demodulation angle 2	26	SG.E	33	78	95	112	deg	feb = feb + 50 kHz
TC1	TINT control characteristic 1	26	SG.E	33	30	45	60	deg	feb = feb + 50 kHz
TC2	TINT control characteristic 2	26	SG.E	33	30	45	60	deg	feb = feb + 50 kHz
Ffsc	fsc output frequency	26	SG.C	32	3.5793	3.5796	3.5799	MHz	
Vfsc	fsc output amplitude	26	SG.C	32	250	500	800	mVpp	
Ffscfree	fsc output frequency in fsc free mode	26	SG.C	32	3.5790	3.5795	3.5810	MHz	
Vfscfree	fsc output amplitude in fsc free mode	26	SG.C	32	250	500	800	mVpp	

Symbol	Subaddress																										
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
CHROMA	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
CnorR																									E0		04
CnorB																									A0		04
ACC1																									A0		04
ACC2																									A0		04
OV																									A0		04
VlkN																									A0		04
KillP																									A0		04
APCU																									A0		04
APCL																									A0		04
R/BN																									E0/A0		04
R-YN1																									E0/A0		04
R-YN2													10												E0/A0		04
TC1									7F																A0		04
TC2									00																A0		04
Ffsc																											
Vfsc																											
Ffscfree								40																			
Vfscfree								40																			

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
RGB	RGB standard conditions	—	—	—	—	—	—	—	Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
VBLK	Output blanking voltage	26	SG.A	50,51, 52	0	0.1	0.3	V	
Gytyp	Contrast control characteristic 1	26	SG.B	50,51, 52	2.2	2.8	3.3	Vpp	f = 100 kHz
GYmin	Contrast control characteristic 2	26	SG.B	50,51, 52	—	200	300	mVpp	f = 100 kHz
GYEnor	Contrast control characteristic 3	26	SG.A	50,51, 52	2.2	2.8	3.3	Vpp	Pin 53 = 2.9 V
GYEmin	Contrast control characteristic 4	26	SG.A	50,51, 52	—	100	200	mVpp	Pin 53 = 0.0 V
GYEclip	Contrast control characteristic 5	59,60, 61	SG.F	50,51, 52	0.50	0.65	0.80	Vpp	Pin 65 = 2.0 V
Lum nor	Brightness control characteristic 1	26	SG.D	50,51, 52	1.7	2.1	2.5	V	Vy = 0.0 V
Lum max	Brightness control characteristic 2	26	SG.D	50,51, 52	2.3	3	—	V	Vy = 0.0 V
Lum min	Brightness control characteristic 3	26	SG.D	50,51, 52	—	1.3	2	V	Vy = 0.0 V
D(R)1	R driving control characteristic 1	26	SG.A	50	2.0	4.0	6.0	dB	
D(B)1	B driving control characteristic 1	26	SG.A	52	2.0	4.0	6.0	dB	
D(R)2	R driving control characteristic 2	26	SG.A	50	–5.0	–3.0	–1.0	dB	
D(B)2	B driving control characteristic 2	26	SG.A	52	–5.0	–3.0	–1.0	dB	
EXD1(R)	Digital OSD (R) I/O characteristic 1	61,65, 26	SG.F, SG.A	50	1.0	1.5	2.0	Vpp	Vosd = 1.0 V, SW61 = ON
EXD1(G)	Digital OSD (G) I/O characteristic 1	61,65, 26	SG.F, SG.A	51	1.0	1.5	2.0	Vpp	Vosd = 1.0 V, SW60 = ON
EXD1(B)	Digital OSD (B) I/O characteristic 1	61,65, 26	SG.F, SG.A	52	1.0	1.5	2.0	Vpp	Vosd = 1.0 V, SW59 = ON
EXD1(R-G)	Digital OSD (R-G) amplitude difference	—	—	—	–350	0	350	mV	
EXD1(G-B)	Digital OSD (G-B) amplitude difference	—	—	—	–350	0	350	mV	
EXD1(B-R)	Digital OSD (B-R) amplitude difference	—	—	—	–350	0	350	mV	
EXD2(R-G)	Digital OSD black level DC voltage difference (R-G)	—	SG.F	50,51	–250	0	250	mV	
EXD2(G-B)	Digital OSD black level DC voltage difference (G-B)	—	SG.F	51,52	–250	0	250	mV	
OFRG	Offset voltage (R-G)	26	SG.D	50,51	–100	0	100	mV	Vy = 0.0 V
OFBG	Offset voltage (B-G)	26	SG.D	51,52	–100	0	100	mV	Vy = 0.0 V
C(R)1	R cutoff control characteristic 1	26	SG.D	50	2.6	2.9	3.2	V	Vy = 0.0 V
C(G)1	G cutoff control characteristic 1	26	SG.D	51	2.6	2.9	3.2	V	Vy = 0.0 V
C(B)1	B cutoff control characteristic 1	26	SG.D	52	2.6	2.9	3.2	V	Vy = 0.0 V
C(R)2	R cutoff control characteristic 2	26	SG.D	50	1.1	1.4	1.7	V	Vy = 0.0 V
C(G)2	G cutoff control characteristic 2	26	SG.D	51	1.1	1.4	1.7	V	Vy = 0.0 V

Symbol	Subaddress																										
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
RGB	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
VBLK										00																	
GYtyp										00																	
GYmin	00									00																	
GYEnor										00																	
GYEmin										00																	
GYEclip	00									00																	
Lum nor										00																	
Lum max		FF								00																	
Lum min		00								00																	
D(R)1		00	7F							00																	
D(B)1		00		7F						00																	
D(R)2		00	00							00																	
D(B)2		00		00						00																	
EXD1(R)										00																	
EXD1(G)										00																	
EXD1(B)										00																	
EXD1(R-G)																											
EXD1(G-B)																											
EXD1(B-R)																											
EXD2(R-G)																											
EXD2(B-G)																											
OFRG										00																	
OFBG										00																	
C(R)1					FF					00																	
C(G)1						FF				00																	
C(B)1							FF			00																	
C(R)2					00					00																	
C(G)2						00				00																	

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
C(B)2		26	SG.D	52	1.1	1.4	1.7	V	Vy = 0.0 V
Ccon1		26	SG.C	51	2	5	8	dB	
Ccon2		26	SG.C	51	—	–15	–10	dB	
Ccon3		26	SG.C	51	—	–40	–35	dB	
MTXRB		26	SG.G	50,52	0.81	0.98	1.08	—	
MTXGB		26	SG.G	51,52	0.29	0.37	0.45	—	
DOSD1		61,65, 26	SG.F, SG.A	50	—	0.05	0.13	μs	Vosd = 1.0 V, SW59 = ON
DOSD2		61,65, 26	SG.F, SG.A	50	—	0.05	0.13	μs	Vosd = 1.0 V, SW59 = ON
BB(R)		26	SG.A	50	1.7	2.1	2.5	V	
BB(G)		26	SG.A	51	1.7	2.1	2.5	V	
BB(B)		26	SG.A	52	2.7	3.7	4.7	V	
WB		26	SG.A	50,51, 52	2.7	3.7	4.7	V	
WBL-RB		26	SG.A Y=30%	50,52	–80.0	–20.0	10.0	mV	White level difference with, without burst, with reference to pin 52 (Bout)
WBL-GB		26	SG.A Y=30%	51,52	–	10.0	80.0	mV	White level difference with, without burst, with reference to pin 52 (Bout)

Symbol	Subaddress																										
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
C(B)2							00			00																	
Ccon 1										7F	80																
Ccon 2										01	80																
Ccon 3										00	80																
MTXRB																											
MTXGB																											
DOSD1	7F																										
DOSD2	7F																										
BB(R)										80																	
BB(G)										80																	
BB(B)										80																	
WB				C0																							
WBL-RB		40																									
WBL-GB		40																									

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
DEF	Deflection system standard conditions	—	—	—	—	—	—	—	Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
fH1	Horizontal free-running frequency 1	—	—	46	15.3	15.7	16.1	kHz	
fH2	Horizontal free-running frequency 2	—	—	46	14.7	15.1	15.5	kHz	
fH3	Horizontal free-running frequency 3	—	—	46	15.8	16.2	16.6	kHz	
Hfree	Forced horizontal free-running operation	26	SG.A	46	15.3	15.7	16.1	kHz	In Hfree operation (0FH: D6 = 1)
FPHU	Horizontal pull-in range (upper)	26	SG.H	46	250	500	—	Hz	Variable input frequency
FPHL	Horizontal pull-in range (lower)	26	SG.H	46	—	–500	–250	Hz	Variable input frequency
HPT1	Horizontal pulse timing 1	26	SG.A	46	4.5	6.0	7.5	µs	
HPT2	Horizontal pulse timing 2	26	SG.A	46	3.5	5.0	6.5	µs	
HPTW	Horizontal pulse width	—	—	46	21	25	29	µs	
VH	Horizontal pulse amplitude	—	—	46	4.7	5.4	—	V	
HSTOP	Horizontal pulse stop operation	—	—	46	—	0.0	0.5	V	When OFH: D7 = 0, confirm that horizontal pulse is stopped
AFCG	AFC gain operation	26	SG.A	43	2.0	3.0	10.0	dB	When 12H is 03, 07, measure and compute amplitude
fV	Vertical free-running frequency	—	—	38	55	60	65	Hz	
Vfree	Forced vertical free-running operation	26	SG.A	38	55	60	65	Hz	In Vfree operation (0EH: D6 = 1)
SVC	Service mode operation	—	—	38	1.0	1.5	2	V	
FPVU	Vertical pull-in frequency (upper)	26	SG.H	38	63	67	—	Hz	Variable input frequency
FPVL	Vertical pull-in frequency (lower)	26	SG.H	38	—	55	57	Hz	Variable input frequency
VRsi1	Vertical ramp size	26	SG.A	38	1.6	2.0	2.4	Vpp	
VRsc1	Vertical ramp size control range 1	26	SG.A	38	2.0	2.4	2.8	Vpp	
VRsc2	Vertical ramp size control range 2	26	SG.A	38	0.8	1.2	1.6	Vpp	
VRpo1	Vertical ramp position control range 1	26	SG.A	38	18	38	58	µs	
VRpo2	Vertical ramp position control range 2	26	SG.A	38	805	825	845	µs	Measured value – VRpo 1
VBLKW	Vertical blanking width	26	SG.A	50,51, 52	1.32	1.47	1.62	ms	
WVSS	Minimum width in minimum sync operation	26	SG.I	38	14	—	—	µs	Variable input signal duty

Symbol	Subaddress																									
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
DEF	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
fH1																											
fH2																								00			
fH3																								06			
Hfree																C8											
FPHU																											
FPHL																											
HPT1																80			0F								
HPT2																8F			0F								
HPTW																											
VH																											
HSTOP																08											
AFCG																			Variable								
fV																											
Vfree															64												
SVC														C0													
FPVU																											
FPVL																											
VRsi 1																											
VRsc 1															30												
VRsc 2															00												
VRpo 1																											
VRpo 2														47													
VBLKW										00																	
WVSS																											

Symbol	Item	Imput signal		Test point	Limits			Unit	Notes
		Pin	SG		Min	Typ	Max		
Monitoring	Intelligent monitor system standard conditions	—	—	—	—	—	—	—	Pins 4, 7 = 5 V; pins 9, 10 = 5 V; pins 23, 65 = 0 V; pins 47, 49 = 8 V
MONI1	Intelligent monitor 1 (composite sync)	26	SG.A	33	—	4.9	—	V	Reference data
MONI6	Intelligent monitor 6 (video SW output)	26	SG.A	33	—	0.95	—	Vpp	Reference data
MONI7	Intelligent monitor 7 (G out)	26	SG.A	33	—	2.0	—	Vpp	Reference data. Amplitude measured from blanking level
MONI8	Intelligent monitor 8 (R out)	26	SG.A	33	—	2.0	—	Vpp	Reference data. Amplitude measured from blanking level
MONI9	Intelligent monitor 9 (B out)	26	SG.A	33	—	2.0	—	Vpp	Reference data. Amplitude measured from blanking level
MONI10	Intelligent monitor 10 (ACL)	—	—	33	—	4.3	—	V	Reference data
MONI11	Intelligent monitor 11 (V sync)	26	SG.A	33	—	4.0	—	Vpp	Reference data
MONI12	Intelligent monitor 12 (H out)	26	SG.A	33	—	3.0	—	Vpp	Reference data
MONI14	Intelligent monitor 14 (DEF Vcc)	—	—	33	—	2.90	—	V	Reference data
MONI15	Intelligent monitor 15 (video/chroma Vcc)	—	—	33	—	2.70	—	V	Reference data
MONI16	Intelligent monitor 16 (Hi Vcc)	—	—	33	—	2.90	—	V	Reference data

- Intelligent Monitor Map
  1. Sub Address: 11HD4 – D7
  2. Output Pin: Pin33
  3. Specification

No.	11H	11H				Output
	HEX	D7	D6	D5	D4	Signal
1	0	0	0	0	0	Composite Sync
2	1	0	0	0	1	—
3	2	0	0	1	0	—
4	3	0	0	1	1	—
5	4	0	1	0	0	—
6	5	0	1	0	1	Y SW OUT
7	6	0	1	1	0	G OUT
8	7	0	1	1	1	R OUT
9	8	1	0	0	0	B OUT
10	9	1	0	0	1	ACL/ABCL
11	A	1	0	1	0	V SYNC
12	B	1	0	1	1	H OUT
13	C	1	1	0	0	DEF VCC
14	D	1	1	0	1	DEF VCC
15	E	1	1	1	0	V/C VCC
16	F	1	1	1	1	HI VCC

Symbol	Subaddress																									
	00H	01H	02H	03H	04H	05H	06H	07H	08H	09H	0AH	0BH	0CH	0DH	0EH	0FH	10H	11H	12H	13H	14H	15H	1BH	1CH	1DH	1EH	1FH
MONITORING	40	80	40	40	80	80	80	00	40	40	20	80	00	40	20	88	00	00	04	00	00	00	00	14	02	00	00
MONI1																		00									
MONI6																		50									
MONI7										00								60									
MONI8										00								70									
MONI9										00								80									
MONI10																		90									
MONI11																		A0									
MONI12																		B0									
MONI14																		D0									
MONI15																		E0									
MONI16																		F0									

Method of Measurement of Electrical Characteristics

Video Clock

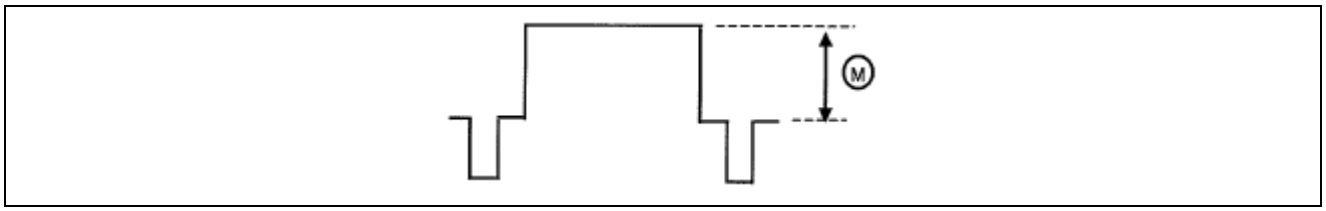
2AGTV1-3 video SW output level (CVBS1-3 input)
2AGEVY video SW output level (Y input)

1. Input SG.A to pin 26 (CVBS1), or pin 24 (CVBS2), or pin 20 (CVBS3), or pin 30 (Yin).
2. The amplitude (p-p) at pin 14 is measured.

* In order to select TV or external input, use the subaddress 0BH.

Y max maximum video output

1. Input SG.A to pin 26.
2. Measure the amplitude (p-p) other than the blanking part of the output of pins 50, 51, 52.



FBY video frequency characteristic

1. Input SG.B (5 MHz, 0.4 Vp-p) to pin 26.
2. Measure the amplitude (p-p) other than the blanking part of the output of pins 50, 51, 52, take the result to be YB.
3. FYB is defined as follows.

$$FYB = 20 \log \frac{YB\ (Vp\text{-}p)}{GY\ (Vp\text{-}p)} (dB)$$

CRF1 chroma trap attenuation 1 (normal R/G/B output)
TRF maximum chroma trap attenuation

1. Input SG.C to pin 26, measure the 3.58 MHz frequency level with TRAP ON/OFF (07H D3) DATA 1, take his to be N_0.
2. Also measure the level with TRAP ON/OFF (07H D3) DATA 0.
3. CRF1 is defined as follows.

$$CRF1 = 20 \log \frac{\text{measured value}\ (mVp\text{-}p)}{N_0\ (mVp\text{-}p)} (dB)$$

4. Take the minimum value of CRF1 when the I^2C BUS data of the TRAP fine ADJ (12H D0 / D1) is adjusted to be TRF.

CRF2 chroma trap attenuation 2 (normal R / G / B output)

1. Input SG.L to pin 26. The input 3.58 MHz frequency level is N_1.
2. Measure the 3.58 MHz frequency level when TRAP ON/OFF (07H D3) DATA 0.
3. CRF2 is defined as follows.

$$CRF2 = 20 \log \frac{\text{measured value}\ (mVp\text{-}p)}{N_1\ (mVp\text{-}p)} (dB)$$

YDL1: YDL time 1

1. Input SG.A to pin 26.
2. Measure the delay time relative to the input signal of pins 50, 51, 52.

The delay time at 50% rise level is measured.

YDL2, 3, 4: YDL time 2, 3, 4

1. Input SG.A to pin 26.
2. Measure the delay time of the input signal and the pin 50, 51, 52 output signals.
3. YDL2, YDL3, YDL4 are defined as follows.
   YDL2 = measured value (ns) – YDL1 (measured value)
   YDL3 = measured value (ns) – YDL2 (measured value)
   YDL4 = measured value (ns) – YDL3 (measured value)

GTmax video tone control characteristic 2

1. Input SG.B (f = 2.5 MHz) to pin 26.
2. The output amplitude of pins 50, 51, 52 when the video tone data is at the center (20 H) is taken to be GTnor.
3. The output amplitude of pins 50, 51, 52 when the video tone data is maximum is measured.
4. GTmax is defined as follows.

$$GTmax = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} (dB)$$

GTmin video tone control characteristic 3

1. Input SG.B (f = 2.5 MHz) to pin 26.
2. The output amplitude of pins 50, 51, 52 when the video tone data is at the center (20 H) is taken to be GTnor.
3. The output amplitude of pins 50, 51, 52 when the video tone data is minimum is measured.
4. GTmin is defined as follows.

$$GTmin = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} (dB)$$

GT2M video tone control characteristic 4

1. Take pin 50, 51, 52 output amplitude when input signal frequency is 2.5 MHz to be GTnor.
2. Input SG.B (f = 2 MHz) to pin 26.
3. Measure pin 50, 51, 52 output amplitude.
4. GT2M is defined as follows

$$GT2M = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} (dB)$$

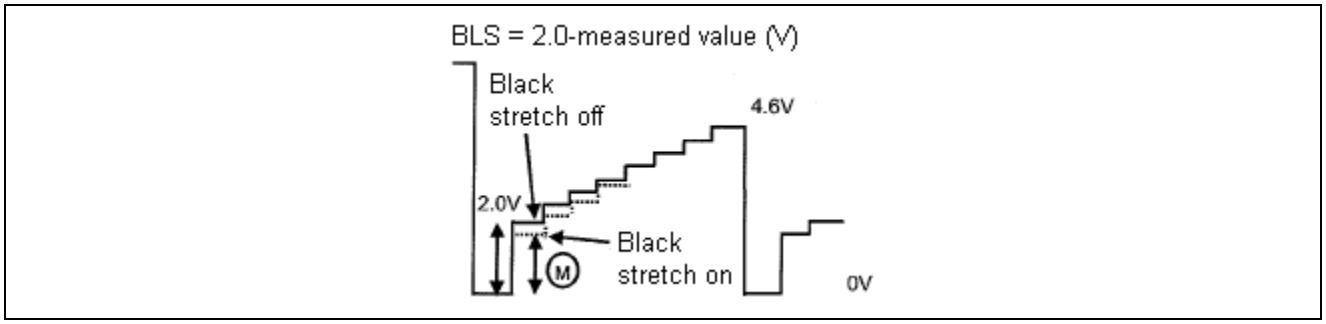
GT5M video tone control characteristic 5

1. Take pin 50, 51, 52 output amplitude when input signal frequency is 2.5 MHz to be GTnor.
2. Input SG.B (f = 2 MHz) to pin 26.
3. Measure pin 50, 51, 52 output amplitude.
4. GT5M is defined as follows.

$$GT5M = 20 \log \frac{\text{measured value (Vp-p)}}{GTnor(Vp\text{-}p)} \text{ (dB)}$$

BLS black stretch characteristic

1. Input SG.K to pin 26.
2. With black stretch off (0BH D7 = 1), adjust the contrast (00H) and brightness (01H), and set the pin 50, 51, 52 output level of the first stage (lowest stage) to 2.0 V, and the output level of the eighth stage (highest stage) to 4.6 V.
3. Change black stretch to on (0BH D7 = 0), and measure the pin 50, 51, 52 first stage output level.
4. BLS is defined as follows.



VMF video mute function

1. Input SG.A to pin 26.
2. With the mute switch (0AH D7) on "VMFon", off "VMFoff", measure the output amplitude.
3. VMF is defined as follows.

$$VMF = 20 \log \frac{VMFon(Vp\text{-}p)}{VMFoff(Vp\text{-}p)} \text{ (dB)}$$

Chroma Block

CnorR chroma standard output (R-Y)
CnorB Chroma standard output (B-Y)

1. Input SG.C to pin 26.
2. When "test mode" I^2C data is 1FH D2=1, 1DH D5=1, take the pin 33 output amplitude when 1DH D6 = 1, D7 = 1 and D6=0, D7=1 to be the chroma standard output (R-Y) and chroma standard output (B - Y), respectively.

ACC1 ACC characteristic 1

1. Input SG.E (eb = 570 mV: level + 6 dB) to pin 26.
2. Measure the pin 33 output amplitude.
3. ACC1 is defined as follows.

$$ACC1 = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma standard output 1 (mVp-p)}} \text{(dB)}$$

ACC2 ACC characteristic 2

1. Input SG.E (input level: -18 dB) to pin 26.
2. Measure the pin 33 output amplitude.
3. ACC2 is defined as follows.

$$ACC2 = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma standard output 1 (mVp-p)}} \text{(dB)}$$

OV chroma overload characteristic

1. Input SG.E (eb = 800 mVp-p: chroma + 3 dB) to pin 26.
2. Measure the pin 33 output amplitude.
3. OV is defined as follows.

$$OV = 20 \log \frac{\text{measured value (mVp-p)}}{\text{chroma standard output 1 (mVp-p)}} \text{(dB)}$$

VikN killer operation input level

1. Input SG.E (variable level) at input level 0 dB to pin 26.
2. While monitoring the pin 33 output amplitude, lower the input level, and measure the input level when the output amplitude vanishes.

KillP hue remaining with killer

1. Input SG.E (level: -40 dB) to pin 26.
2. Measure the pin 33 output amplitude.

APCU APC pull-in range (upper)
APCL APC pull-in range (lower)

1. Input SG.E (feb-fec-3.579545 MHz) to pin 26.
2. After raising the frequency until the output from pin 33 vanishes, lower the frequency, and take the point at which an output appears to be fu.
3. After lowering the frequency until the output from pin 33 vanishes, raise the frequency, and take the point at which an output appears to be fl.
4. APCU and APCL are defined as follows.
   APCU = fu – 3579545 Hz
   APCL = fl – 3579545 Hz

R/BN demodulation ratio R-Y/B-Y

1. Input SG.E (eb = single chroma = ec + 50 kHz) to pin 26.
2. Take the pin 33 output amplitude when "test mode" I^2C data is 1DH D6 = 1, D7 = 1 to be VRY.
3. Take the pin 33 output amplitude when "test mode" I^2C data is 1DH D6 = 0, D7 = 1 to be VBY.
4. R/BN is defined as follows.

$$R/BN = \frac{VRY\ (mVp\text{-}p)}{VBY\ (mVp\text{-}p)}$$

R-YN demodulation angle

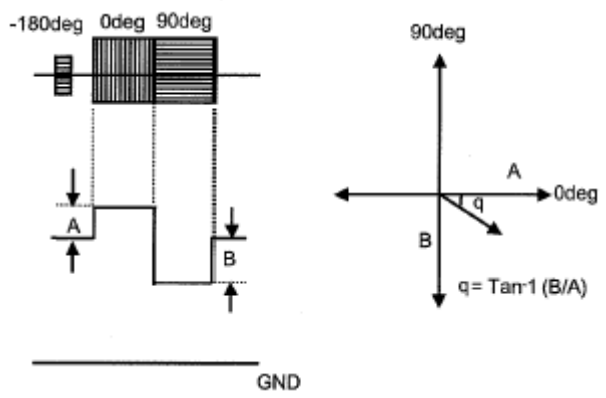
1. Input SG.E (eb = single chroma = ec + 5 kHz) to pin 26.
2. Take the pin 33 output amplitude when "test mode" I^2C data is 1DH D6 = 1, D7 = 1 to be VRY.
3. Take the pin 33 output amplitude when "test mode" I^2C data is 1DH D6 = 0, D7 = 1 to be VBY.
4. R/YN is defined as follows.

$$R\text{-}YN = \mathrm{Tan}^{-1}\ \frac{VRY \times 3.8}{(VBY \times 1.9) + 45}(deg)$$

* The vector is determined taking the demodulator gain into account.

TC1 TINT control characteristic 1
TC2 TINT control characteristic 2

1. Input SG.C (see figure below) to pin 26. Measure the absolute angle with reference to the pin 33 output voltage, referring to the figure below.



2. Take the TINT data center part (08H data 3CH) to be reference angle "TC", determine the TINT DATA maximum and minimum values. TC1 and TC2 are defined as follows.
   TC1 = Tcmax – TC(deg)
   TC2 = TC – Tcmin(deg)

Ffsc fsc output frequency
Vfsc fsc output amplitude

1. Input SG.C to pin 26.
2. Measure the pin 32 output frequency and amplitude.

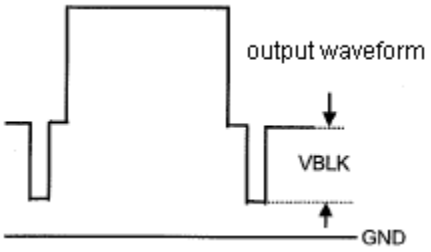
Ffscfree fsc output frequency in fsc free mode
Vfscfree fsc output amplitude in fsc free mode

1. Input SG.C to pin 26.
2. Measure the pin 32 output frequency and amplitude with fsc free (07H D6) DATA 1.

RGB Interface Block

VBLK output blanking voltage

1. Input SG.A to pin 26.
2. Measure the voltage of the pin 50, 51, 52 pedestal and blanking parts.



GYmax contrast control characteristic 1
GYmin contrast control characteristic 2

1. Input SG.B (f = 100 kHz) to pin 26.
2. Measure the pin 50, 51, 52 output amplitude.

GYEnor contrast control characteristic 3
GYEmin contrast control characteristic 4

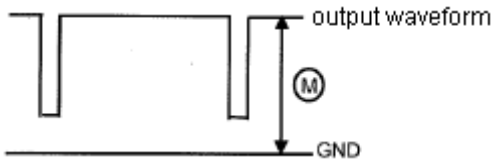
1. Input SG.A to pin 26.
2. Measure the pin 50, 51, 52 output amplitude when applying 2.9 V and 0 V to pin 33.

GYEclip contrast control characteristic 5

1. Input SG.F to pins 59, 60, 61, 65.
2. Minimize the contrast control data, and measure the output amplitude at and above the pedestal part of pins 50, 51, 52. The amplitude of the blanking part is not measured.

Lum nor brightness control characteristic 1
Lum max brightness control characteristic 2
Lum min brightness control characteristic 3

1. Input SG.D (Vy = 0 V) to pin 26.
2. Measure the DC voltage other than the blanking part of the output of pins 50, 51, 52.



D(R)1 R drive control characteristic 1

1. Input SG.A to pin 26.
2. Measure the pin 50 output amplitude when the drive control data is at center and is maximum, take the results to beDRnor and DRmax respectively.
3. D (R) 1 is defined as follows.

$$D(R)1 = 20 \log \frac{DRmax\ (Vp\text{-}p)}{DRnor\ (Vp\text{-}p)} (dB)$$

D(B)1 B drive control characteristic 1

1. Input SG.A to pin 26.
2. Measure the pin 52 output amplitude when the drive control data is at center and is maximum, take the results to be DBnor and DBmax respectively.
3. D(B)1 is defined as follows.

$$D(B)1 = 20 \log \frac{DBmax\ (Vp\text{-}p)}{DBnor\ (Vp\text{-}p)} (dB)$$

D(R)2 R drive control characteristic 2

1. Input SG.A to pin 26.
2. Measure the pin 50 output amplitude when the drive control data is at center and is minimum, take the results to be DRnor and DRmin respectively.
3. D(R)2 is defined as follows.

$$D(R)2 = 20 \log \frac{DRmin\ (Vp\text{-}p)}{DRnor\ (Vp\text{-}p)} (dB)$$

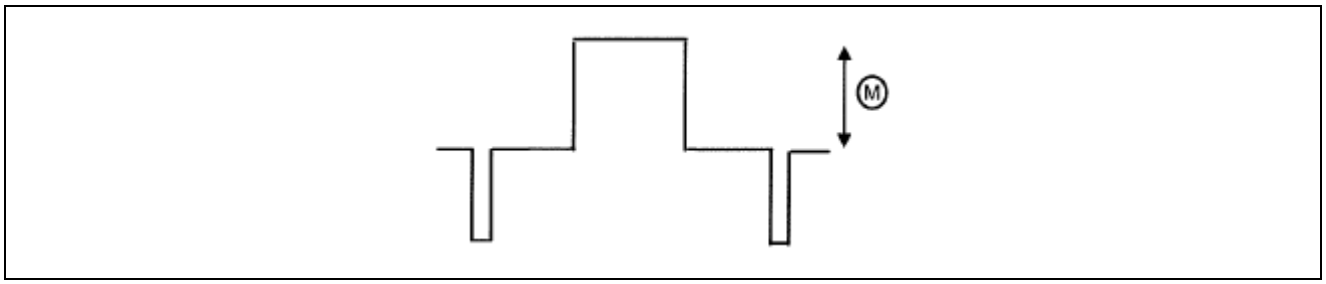
D(B)2 R drive control characteristic 2

1. Input SG.A to pin 26.
2. Measure the pin 52 output amplitude when the drive control data is at center and is minimum, take the results to be DBnor and DBmin respectively.
3. D(B)2 is defined as follows.

$$D(B)2 = 20 \log \frac{DBmin\ (Vp\text{-}p)}{DBnor\ (Vp\text{-}p)} (dB)$$

EXD(R) digital OSD(R) input/output characteristic
EXD(G) digital OSD(G) input/output characteristic
EXD(B) digital OSD(B) input/output characteristic

1. Input SG.F (Vosd = 1.0 V) to pins 59, 60, 61, 65.
2. Measure the output amplitude at and above the pedestal part in pins 50, 51, 52. The amplitude of the blanking part is not measured.



EXD(R-G) digital OSD (R-G) amplitude difference
EXD(G-B) digital OSD (G-B) amplitude difference
EXD(B-R) digital OSD (B-R) amplitude difference

1. EXD (R-G), EXD (G-B) and EXD (B-R) are defined as follows.

$$EXD(R\text{-}G) = EXD(R) - EXD(G)$$
$$EXD(G\text{-}B) = EXD(G) - EXD(B)$$
$$EXD(B\text{-}R) = EXD(B) - EXD(R)$$

C (R) 1 R cutoff characteristic 1
C (G) 1 G cutoff characteristic 1
C (B) 1 B cutoff characteristic 1
C (R) 2 R cutoff characteristic 2
C (G) 2 G cutoff characteristic 2
C (B) 2 B cutoff characteristic 2

1. Input SG.D (Vy = 0 V) to pin 26.
2. Measure the DC voltage of other than the blanking part in the outputs of pins 50, 51, 52.

Ccon1 color control characteristic 1
Ccon2 color control characteristic 2
Ccon3 color control characteristic 3

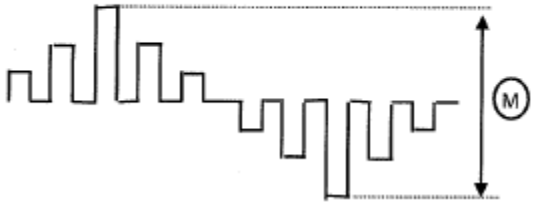
1. Input SG.C to pin 26.
2. Measure the output amplitudes of pins 50, 51, 52 when IIC DATA 09H = 40h, take this to be Ccon0.
3. Measure the output amplitudes of pins 50, 51, 52 under each set of conditions.
4. Ccon1, Ccon2, Ccon3 are defined as follows.

$$\text{Ccon1,Ccon2,Ccon3} = 20 \log \frac{\text{measured value (Vp-p)}}{\text{Ccon0 (Vp-p)}} \text{ (dB)}$$

MTXRB matrix ratio R/B
MTXGB matrix ratio G/B

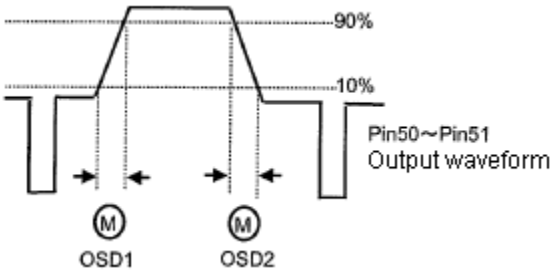
1. Input SG.G (rainbow color bar) to pin 26.
2. Measure the output amplitude when pins 50, 51, 52 are respectively VR, VG, VB.
3. MTXRB, MTXGB are defined as follows.

$$\text{MTXRB} = \frac{\text{VR (Vp-p)}}{\text{VB (Vp-p)}} \quad \text{MTXGB} = \frac{\text{VG (Vp-p)}}{\text{VB (Vp-p)}}$$



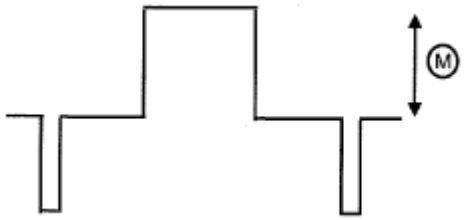
DOSD1 digital OSD switching characteristic 1
DOSD2 digital OSD switching characteristic 2

1. Input SG.F (Vosd = 1.0 V) to pins 65, 59, 60, 61.
2. Measure the rise time and fall time of the output signals of pins 50, 51, 52 at and above pedestal level. The blanking part is not measured.



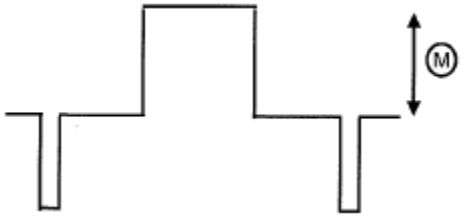
BB(R) blue back function (R)
BB(G) blue back function (G)
BB(B) blue back function (B)

1. Input SG.A to pin 26.
2. Measure the output amplitude (p-p) of pins 50, 51, 52 other than the blanking part.



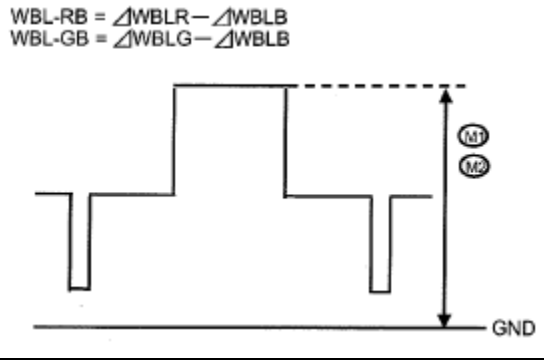
WB white raster function

1. Input SG.A to pin 26.
2. Measure the output amplitude (p-p) of pins 50, 51, 52 other than the blanking part.



WBL-RB white balance difference-RB
WBL-GB white balance difference-GB

1. Input SG.A (Y = 30%L with burst) to pin 26.
2. Measure the pin 50, 51, 52 output white level potential from GND. Measured values are taken to be M1R, M1G, M1B respectively.
3. Input SG.A (Y = 30%: without burst) to pin 26.
4. Measure the pin 50, 51, 52 output white level potential from GND. Measured values are taken to be M2R, M2G, M2B respectively.
5. Calculate the differences in measured values.
6. Calculate the differences between calculated values of Rch and Bch with the Bch measured value as reference, defined as follows.



Deflection Block

fH1 horizontal free-running frequency 1
fH2 horizontal free-running frequency 2
fH3 horizontal free-running frequency 3

1. Measure the frequency of pin 46 with no input.

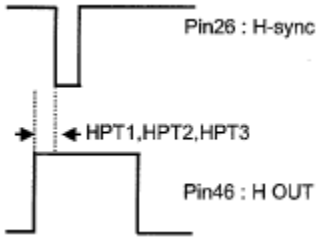
Hfree forced horizontal free-running operation

1. Input SG.A to pin 26.
2. Set H-FREE CONTROL DATA to on, measure the frequency at pin 46.

FPHU horizontal pull-in range (upper)
FPHL horizontal pull-in range (lower)

1. Input SG.H to pin 26.
2. Change the frequency of SG.H, measure the frequency range for which the pin 46 output signal and pin 26 input signal are pulled in, with respect to the video signal horizontal frequency.

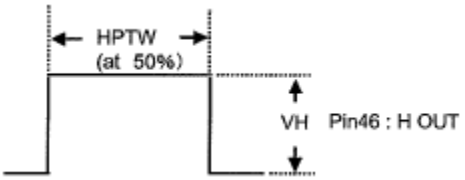
HPT1 horizontal pulse timing 1



HPT2 horizontal pulse timing 2

1. Measure the horizontal pulse timing using the method for HPT1.
2. Standard
   HPT2 = (measured value) – HPT1

HPTW horizontal pulse width
VH horizontal pulse amplitude



HSTOP horizontal pulse stop operation

1. Confirm that when H.START SW OFF (0FH:D7 = 0), the horizontal output goes low.

AFCG AFC gain operation

1. Measure the pin 43 output amplitude during AFC switching, taking the result when 12HD0 = 1, D1 = 1, D2 = 0 to be AFCtyp, and 12H D0 = 1, D1 = 1, D2 = 1 to be AFCmax.
2. AFCG is defined as follows.

$$AFCG = 20 \log \frac{AFCmax\ (Vp\text{-}p)}{AFCtyp\ (Vp\text{-}p)}\ (dB)$$

fV vertical free-running frequency

1. Measure the pin 38 output frequency with no input.

Vfree forced vertical free-running operation

1. Input SG.A to pin 26.
2. Set V-FREE CONTROL DATA to on, measure the pin 38 output amplitude.

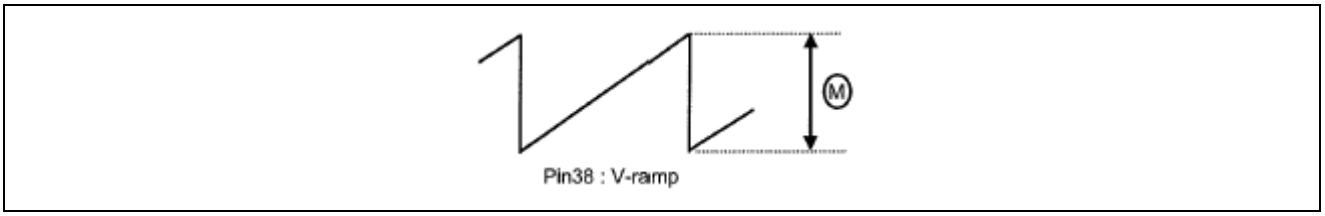
SCV service mode operation

1. Measure the pin 38 output DC voltage with the service switch on.

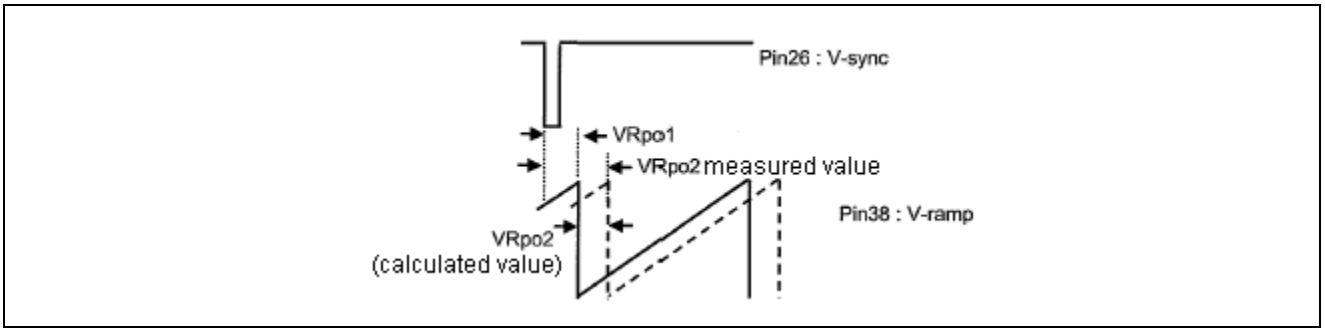
FPVU vertical pull-in frequency (upper)
FVPL vertical pull-in frequency (lower)

1. Change the SG.H vertical frequency, and measure the frequency when the pin 38 output waveform is pulled in.

VRsi vertical ramp size
VRsc1 vertical ramp size control range 1
VRsc2 vertical ramp size control range 2



VRpo1 vertical ramp position control range 1

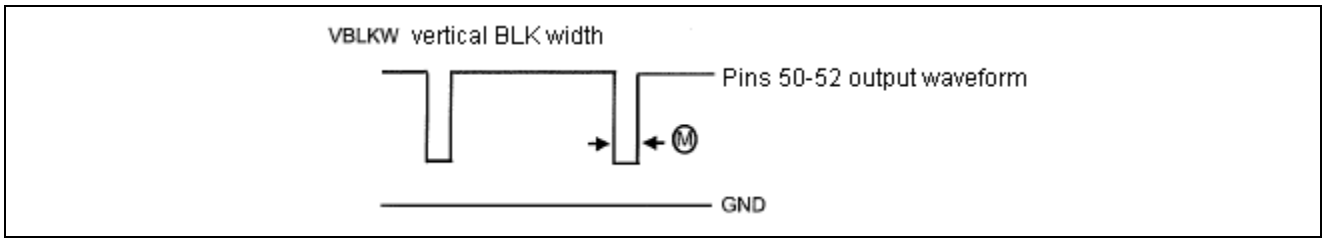


Rpo1 vertical ramp position control range 2

1. Measure the vertical ramp timing using the same method as for VRpo1.
2. VRpo2 is defined as follows.

VRpo2 = (measured value) - VRpo1

VBLKW vertical BLK width



WVSS minimum width at minimum sync operation

1. Reduce the width of the SG.I signal, and measure the input signal width when the pin 38 output waveform pull-in is lost.

Electrical Characteristics (MCU unit)

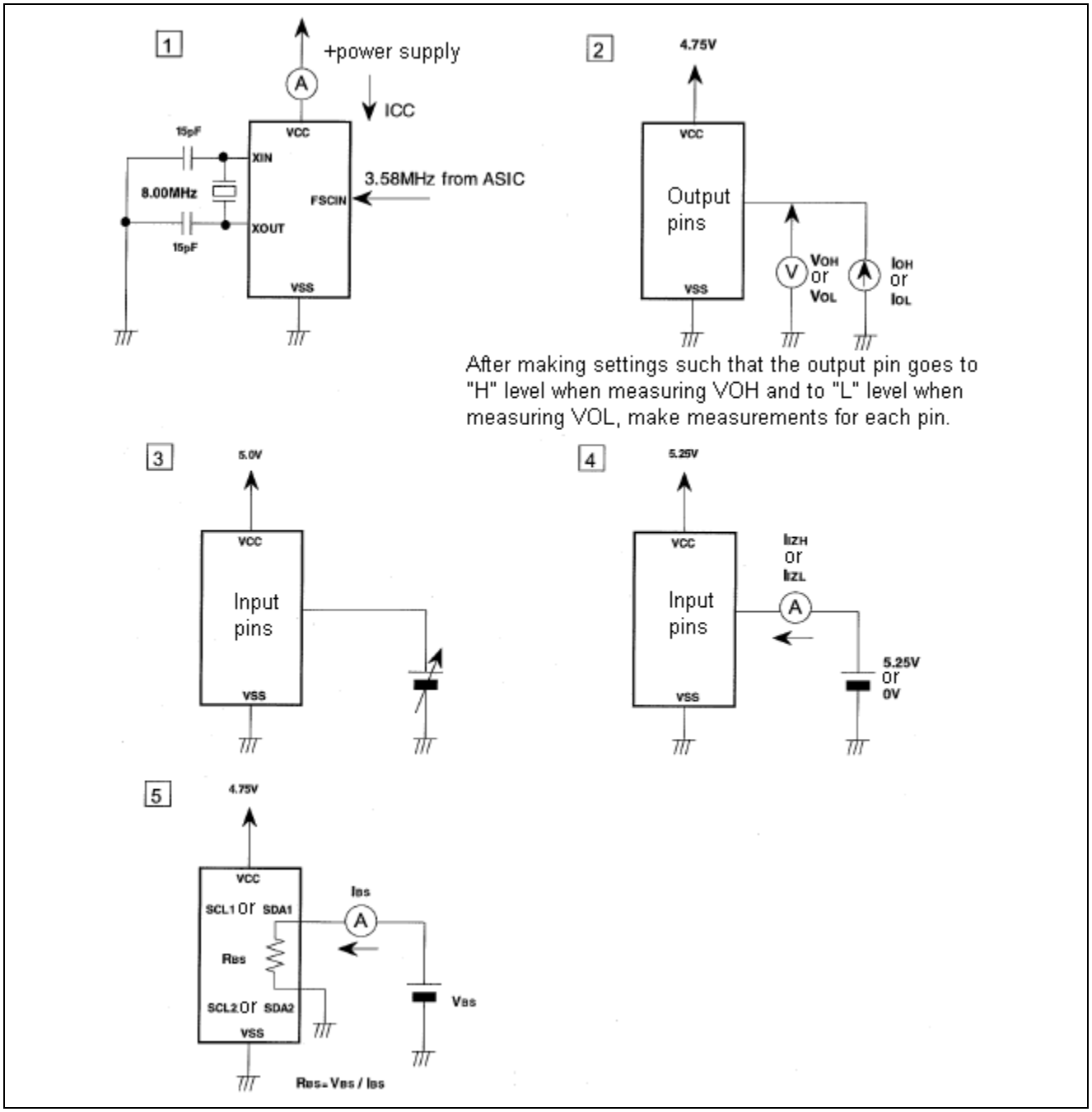
1. Electrical characteristics

(unless otherwise noted, VDD = 5 V ±5%, Vss = 0 V, f(XIN) = 8.95 MHz, Ta = –10 to 65°C)

Symbol	Item		Measurement Conditions		Limits Min.	Limits Typ.	Limits Max.	Unit	Measurement Circuit
I_{CC}	Power supply current	During system operation	Vcc=5.25V, $f(X_{IN})$=8.95MHz	OSD OFF Data slicer off	—	15	30	mA	1
				OSD ON Data slicer on	—	30	45	mA	
			Vcc=5.25V, $f(X_{IN})$=0, $f(X_{CIN})$=32kHz, OSD OFF, Data slicer off, Low power dissipation mode (CM5="0", CM6="1")		—	60	200	µA	
		During wait	Vcc=5.25V, $f(X_{IN})$=8MHz		—	2	4	mA	
			Vcc=5.25V, $f(X_{IN})$=0, $f(X_{CIN})$=32kHz, Low power dissipation mode (CM5="0", CM6="1")		—	60	200	µA	
		When stopped	Vcc=5.25V, $f(X_{IN})$=0, $f(X_{CIN})$=0		—	1	10		
V_{OH}	"H" output voltage	P11~P14, P20~P27, P40, P41	Vcc=4.75V, I_{OH}=–0.5mA		2.4	—	—	V	2
V_{OL}	"L" output voltage	P00~P07, P20~P23, P40, P41	Vcc=4.75V, I_{OL}=0.5mA		—	—	0.4	V	
		P24~P27	Vcc=4.75V, I_{OL}=10.0mA		—	—	3.0		
		P11~P14	Vcc=4.75V	I_{OL}=3mA	—	—	0.4		
				I_{OL}=6mA			0.6		
$V_{T+} - V_{T-}$	Hysteresis (*1) RESET, INT1, INT2, INT3, TIM3,S_{IN}, S_{CLK}, SCL1, SCL2, SDA1, SDA2		Vcc=5.0V		—	0.5	1.3	V	3
I_{IZH}	"H" input leakage current P00~P07, P11~P14, P20~P27, P40~P45, RESET		Vcc=5.25V, V_I=5.25V		—	—	5	µA	4
I_{IZL}	"L" input leakage current P00~P07, P11~P14, P20~P27, P40~P45, RESET		Vcc=5.25V, V_I=0V		—	—	5	µA	4
R_{BS}	I^2C-BUS bus switch connection resistance (between SCL1 and SCL2, SDA1 and SDA2)		Vcc=4.75V		—	—	130	Ω	5

Note: 1. when using P06, P07, P16, P23, P24, P25 as interrupt inputs or external clock inputs for timers, when using P20 to P22 as serial I / O, and when using P11 to P14 as multi-master I^2C-BUS interface pins, there is hystersis.

2. Test Circuit

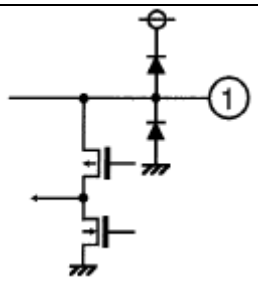
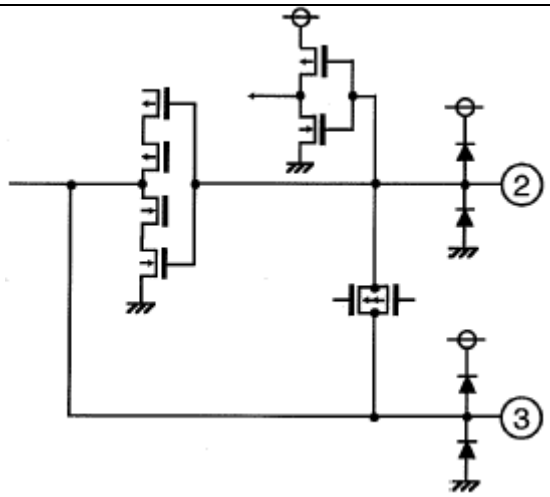
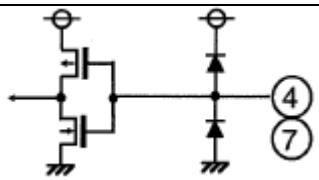
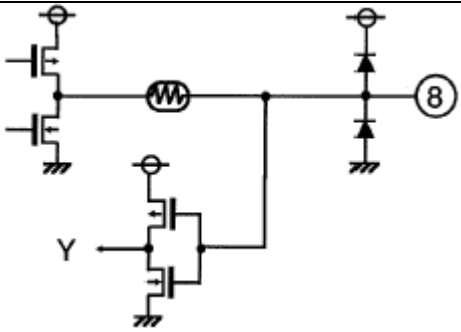
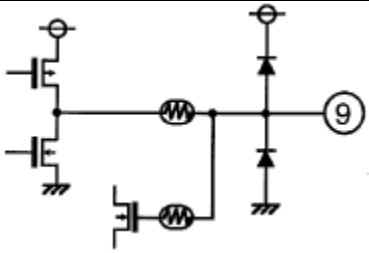


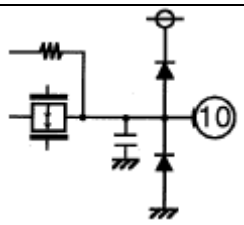
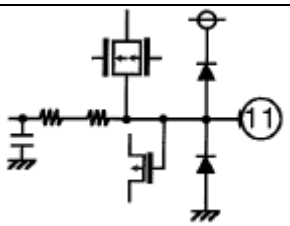
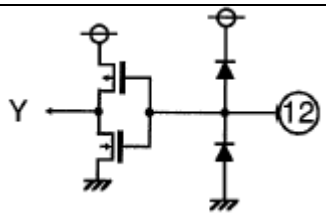
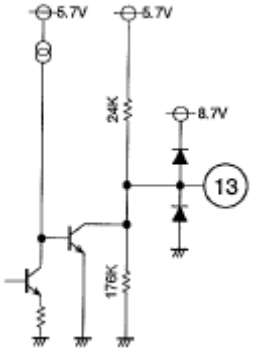
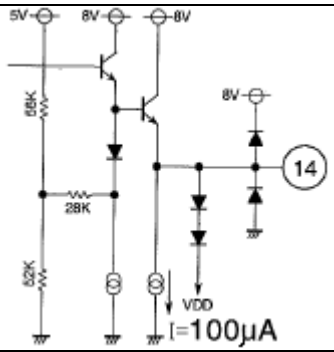
A/D Converter Characteristics

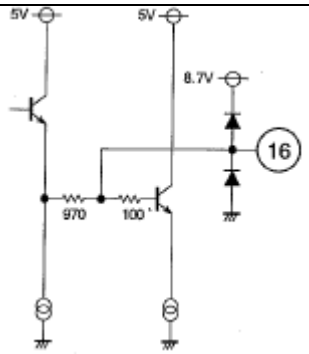
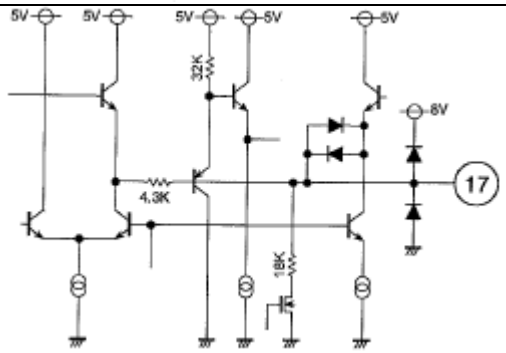
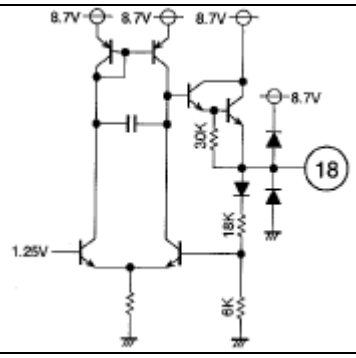
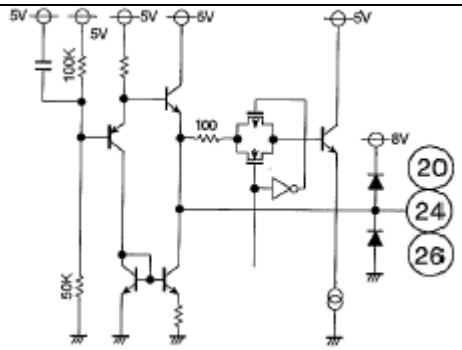
(unless otherwise noted, VDD = 5 V ±5%, Vss = 0 V, f(XIN) = 8.95 MHz, Ta = –10 to 65°C)

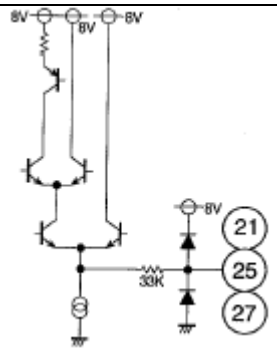
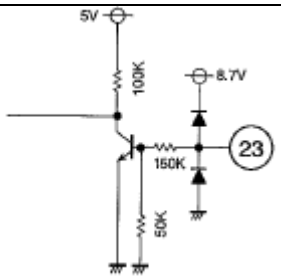
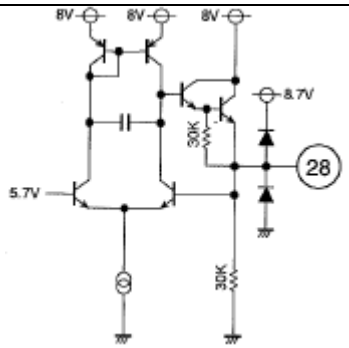
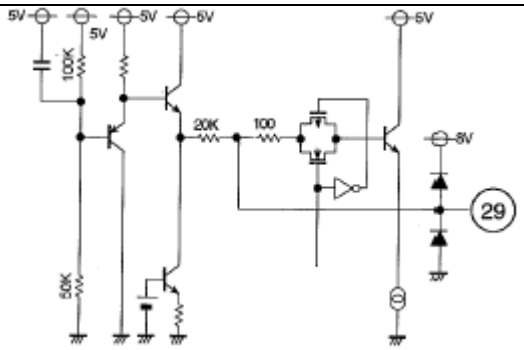
Symbol	Item	Measurement Conditions	Limits			Unit
			Min	Typ	Max	
–	Resolution				7	bits
–	Nonlinear				±1.5	LSB
–	Diffierential Nonlinear error				±0.9	LSB
V_{OT}	Zero-transition error	IOL (SUM) = –0 mA			2	LSB
V_{EST}	Full-scale transition error				–2	LSB

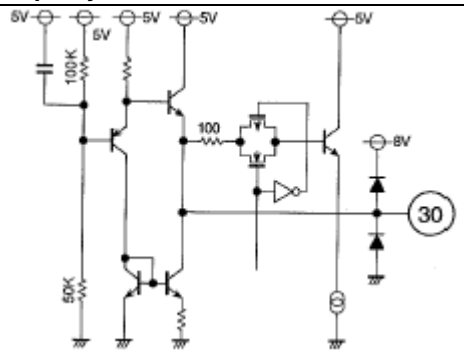
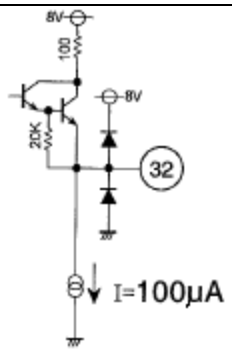
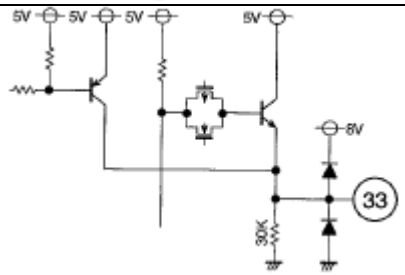
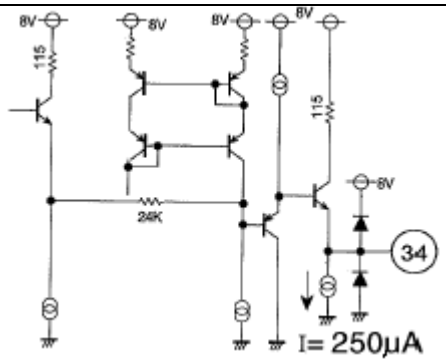
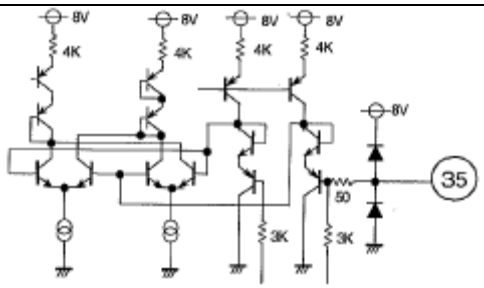
Pin Description

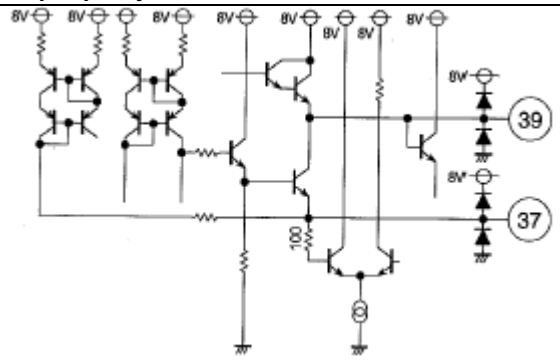
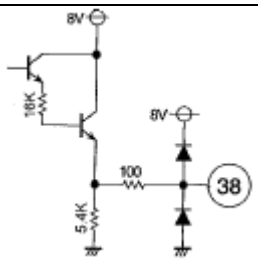
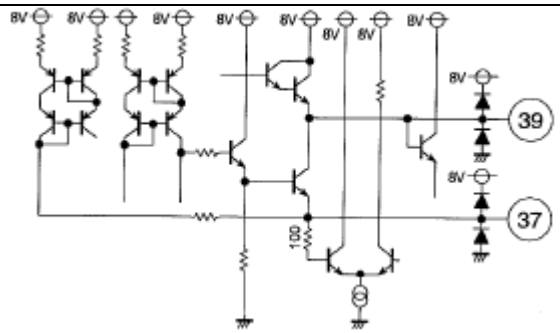
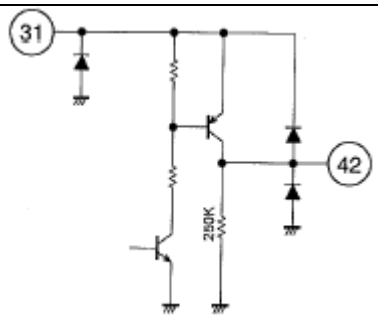
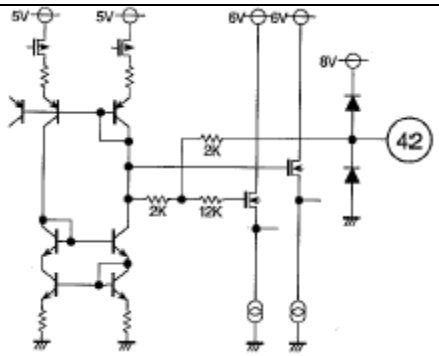
Pin no.	Name	Pin periphery	Notes
1	CNVSS		0 V
2 3	X IN XOUT		—
4 7	TEST1 TEST0		—
5	Vss (MCU)	—	Power source for MCU 0 V
6	Vdd (MCU)	—	Power source for MCU 5.0 V ±5%
8	FILT		—
9	HLF		—

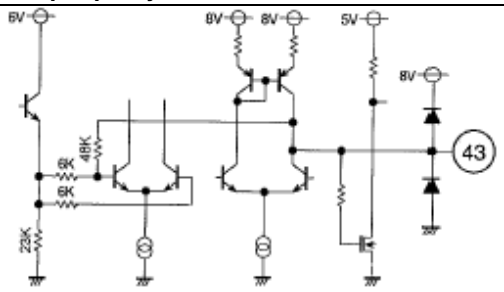
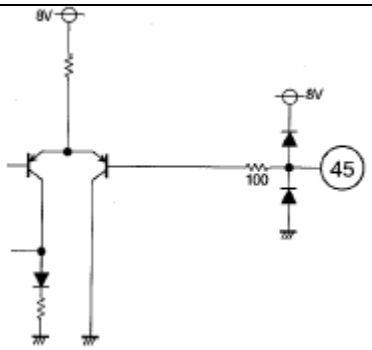
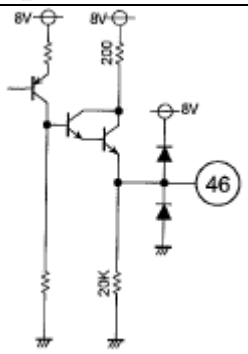
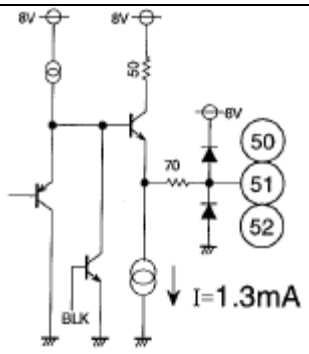
Pin no.	Name	Pin periphery	Notes
10	VHOLD		—
11	CVIN		—
12	RESET		—
13	MCU RESET OUT		H: 5.0 V L: 0.0 V
14	Y SW OUT		1.7 V
15	Video/Chroma GND	—	0.0 V

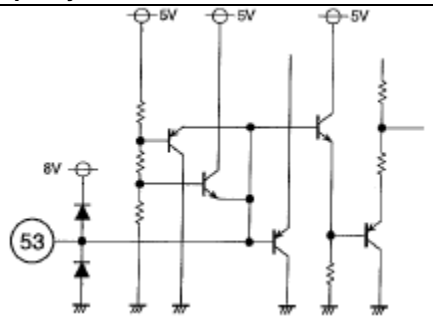
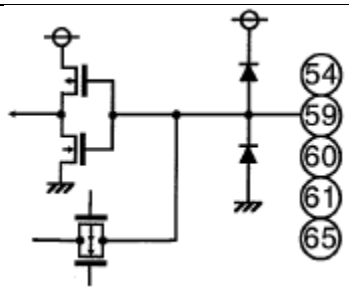
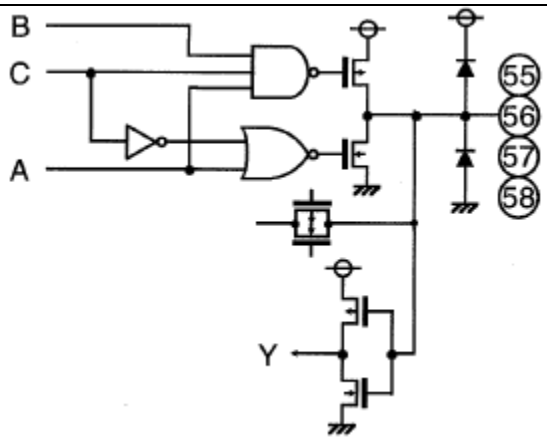
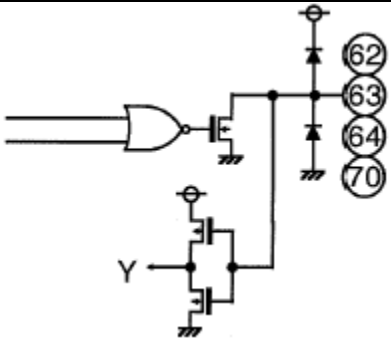
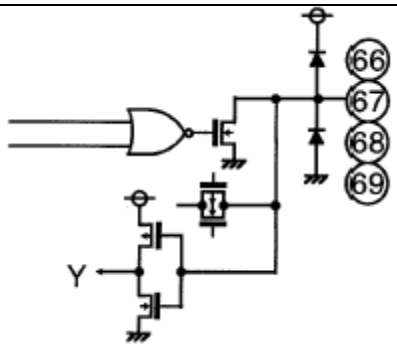
Pin no.	Name	Pin periphery	Notes
16	X-TAL 3.58		3.3 V
17	CHROMA APC FILTER		3.2 V
18	MCU 5.7VREG OUT		5.7 V Maximum outflow current = 2.5 mA
19	NC	—	—
20 24 26	CVBS IN 3/2/1		1.7 V

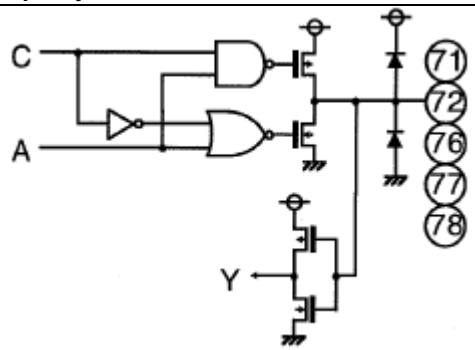
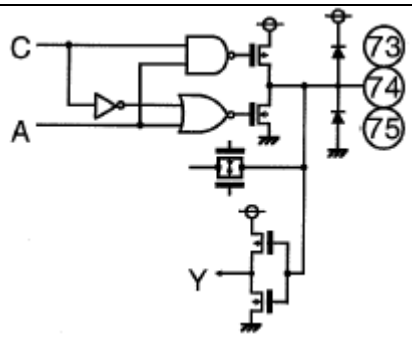
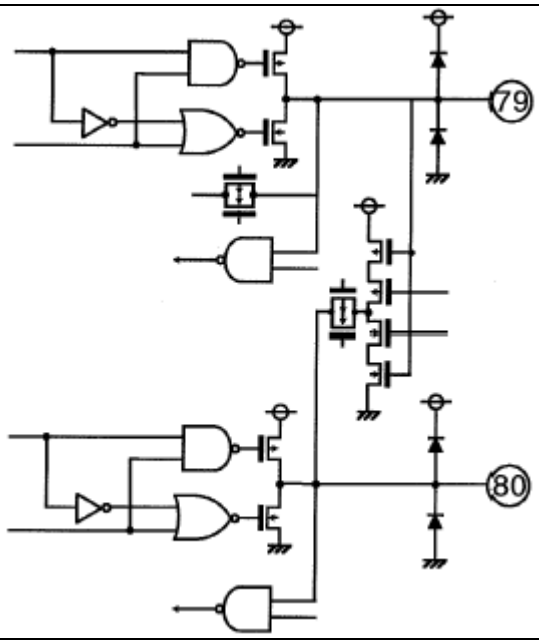
Pin no.	Name	Pin periphery	Notes
21 25 27	AUDIO IN 3/2/1		2.3 V
22	Video/Chroma Vcc	—	5.0 V
23	MCU TEST		0 V
28	5.7 VREG OUT		5.7 V Maxim outflow current = 5 mA
29	C IN		2.1 V

Pin no.	Name	Pin periphery	Notes
30	Y IN		1.7 V
31	VREG Vcc	—	8.7 V
32	fsc OUT		3.0 V
33	INTELLIGENT MONITOR		Maxim outflow current = 100 µA
34	AUDIO ATT OUT		3.5 V
35	AUDIO ATT FILTER		2.75 V to 3.25 V
36	TEST2	—	GND

Pin no.	Name	Pin periphery	Notes
37	V RAMP FEED BACK		—
38	RAMP OUT		4.6 V Maxim outflow current = 1 mA
39	V RAMP CAP		—
40	8.7 VREG OUT		8.7 V Maximum outflow current = 1 mA
41	NC	—	—
42	H VCO FEEDBACK		3.0 V

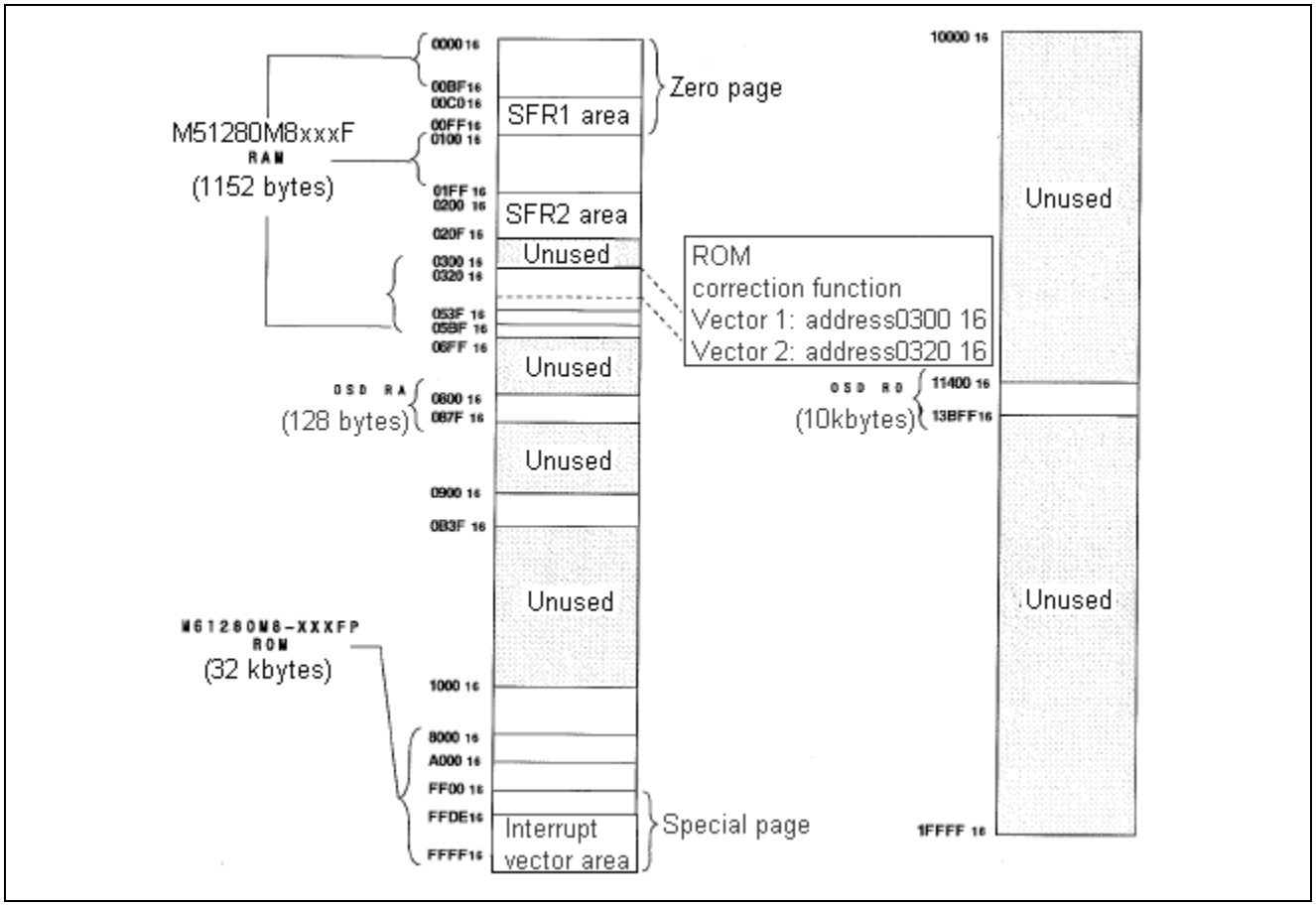
Pin no.	Name	Pin periphery	Notes
43	AFC FILTER		3.5 V
44	DEF GND	—	—
45	FBP IN		V_{TH}: 1.0 V
46	H OUT		V_{OL}: 0.0 V V_{OH}: 5.4 V Maximum outflow current = 4 mA
47	DEF Vcc	—	8V
48	NC	—	—
49	Hi Vcc	—	8V
50 51 52	R OUT G OUT B OUT		—

Pin no.	Name	Pin periphery	Notes
53	ACL/ABCL		—
54	TEST2		Use with only pin 54 open
59 60 61 65	P42 P43 P44 P45		—
55 56 57 58	P14/SDA2 P13/SDA1 P12/SCL1 P11/SCL2		—
62 63 64 70	P00/PWM0 P01/PWM1 P02/PWM2 P07/INT1		—
66 67 68 69	P03/PWM3/AD1 P04/PWM4/AD2 P05/AD3 P06/INT2/AD4		—

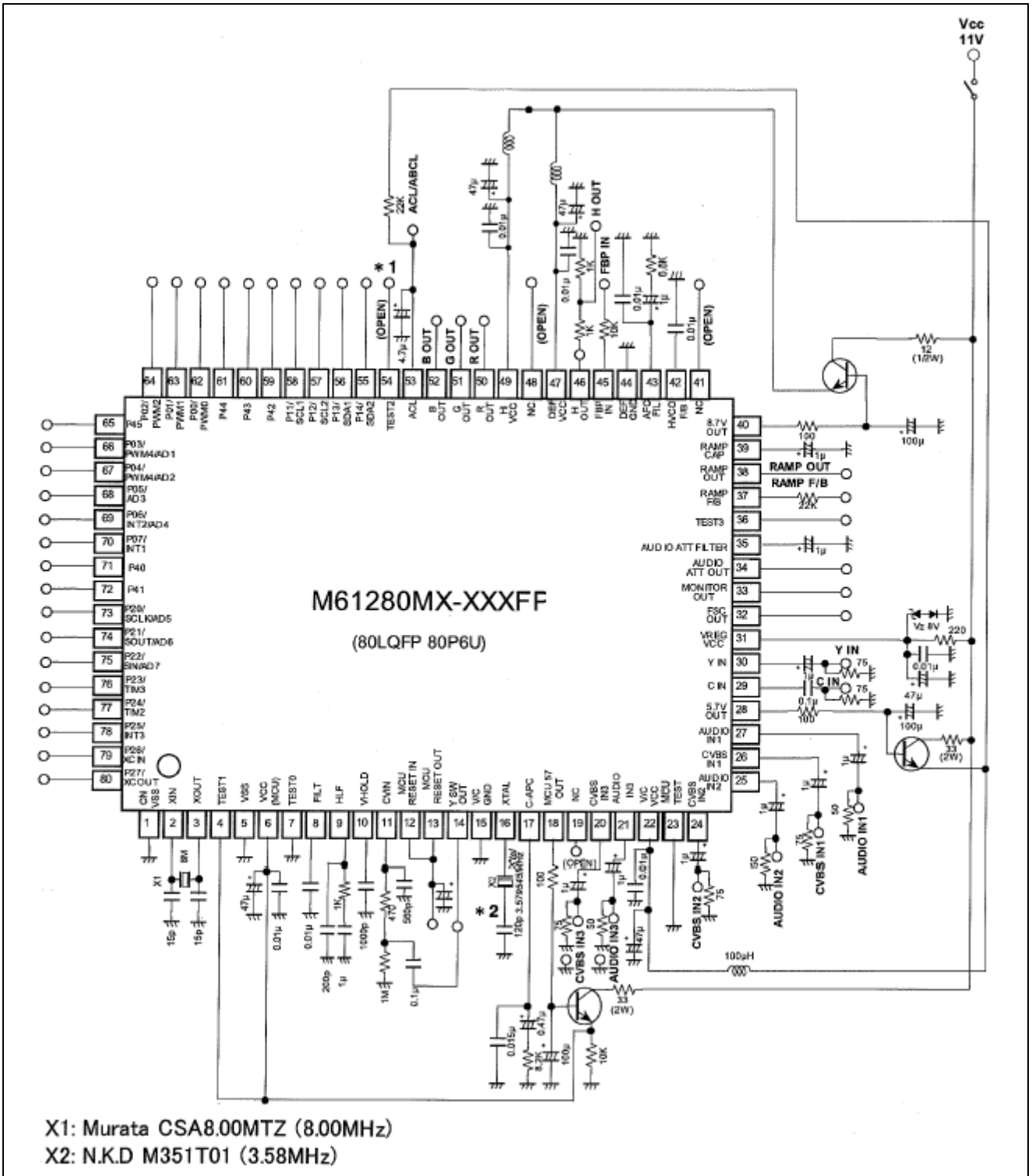
Pin no.	Name	Pin periphery	Notes
71 72 76 77 78	P40 P41 P23/TIM3 P24/TIM2 P25/INT3		—
73 74 75	P20/SLK/AD5 P21/SOUT/AD6 P22/SIN/AD7		—
79 80	P26/XCIN P27/XCOUT		—

Note: Voltage, current and other values appearing in the Notes column are reference values, and are not guaranteed rated values.

Memory Layout Diagram



Application Circuit



Notes: 1. Pin 54 should be kept open.

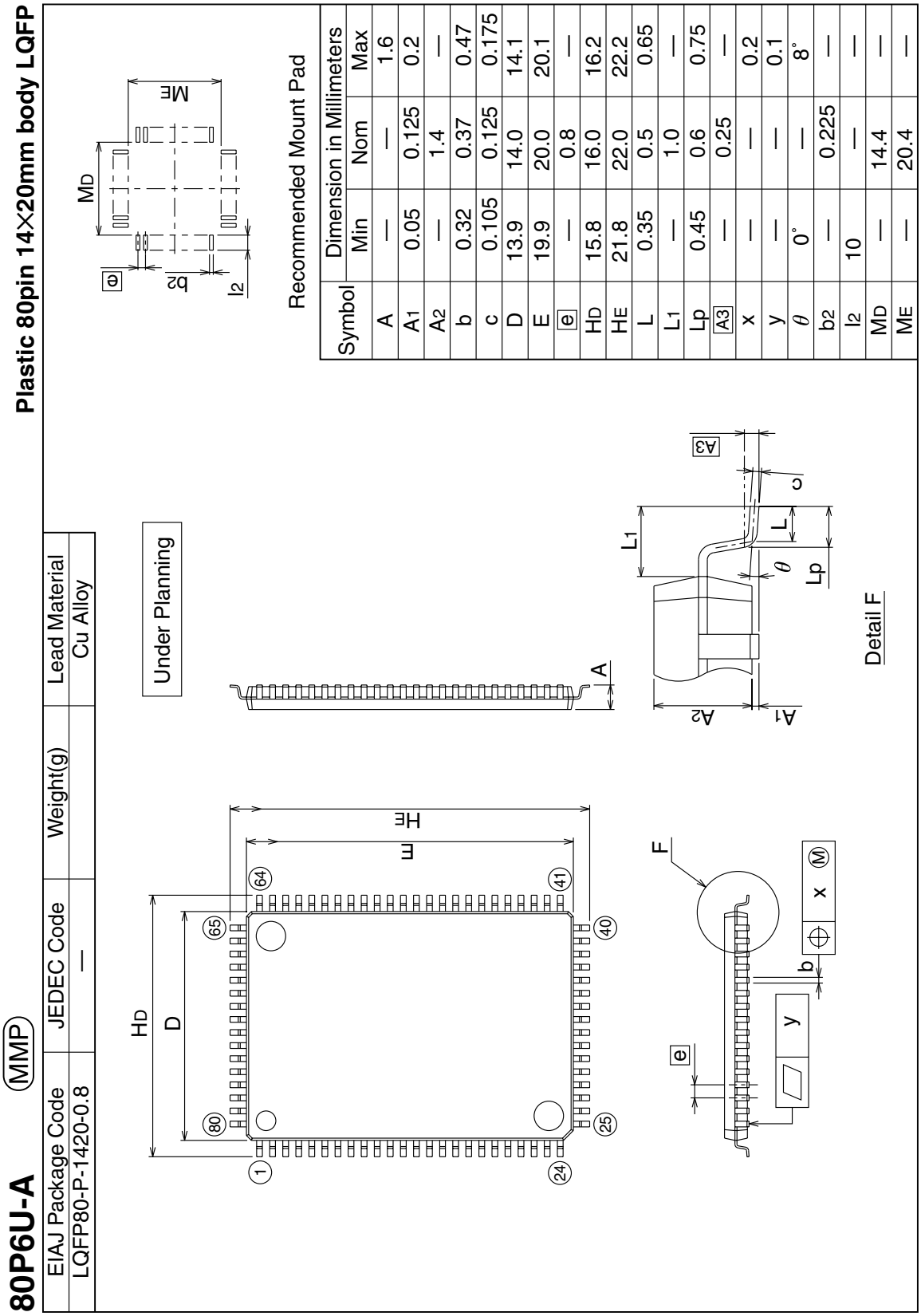
2. If a crystal oscillator other than that recommended is used, the capacitance connected to X2 (3.58 MHz Xtal) must be studied.

Note: Connections to pins 55 to 80 may differ depending on conditions of use.

Important Information

- Each application should be thoroughly studied and evaluated before making a decision.
- 47 μF and higher electrolytic capacitors and 0.01 μF and higher ceramic capacitors should be connected in parallel between each of the power supply pins (6, 22, 31, 47, 49) and ground. In addition, it is recommended that the connections be made as close to the IC power supply pins as possible.
- When purchasing I^2C bus components, a license to use these components within a I^2C bus system is provided under the I^2C patent rights of Philips Corp.
- However, the bus system must conform to the I^2C specifications stipulated by Philips.

Package Dimensions



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