

# M61506FP

Peak hold IC for 5 band spectrum analyzer displays

## DESCRIPTION

The M61506FP is a 5 band peak hold ICs that use microprocessor time division to produce serial output for spectrum analyzer displays.

## FEATURES

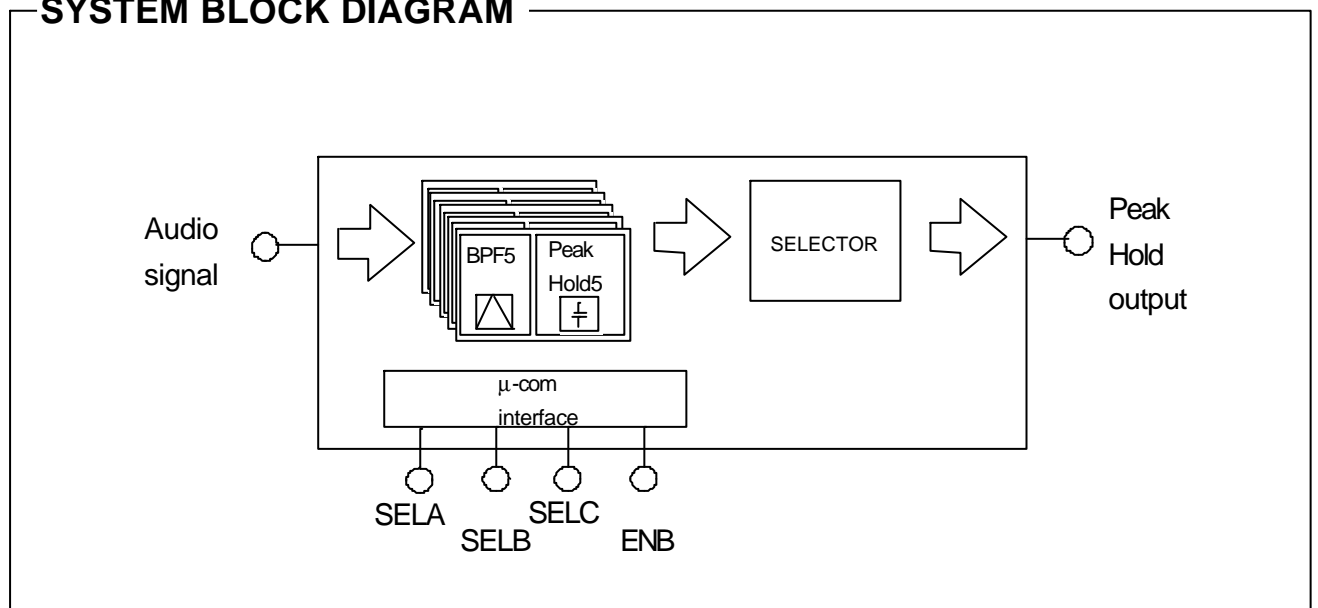
- 5 band peak hold elements for spectrum analyzer displays.
- Discharge time constant circuit for each band is on the chip.
- Single 5V power supply.

## RECOMMENDED OPERATING CONDITIONS

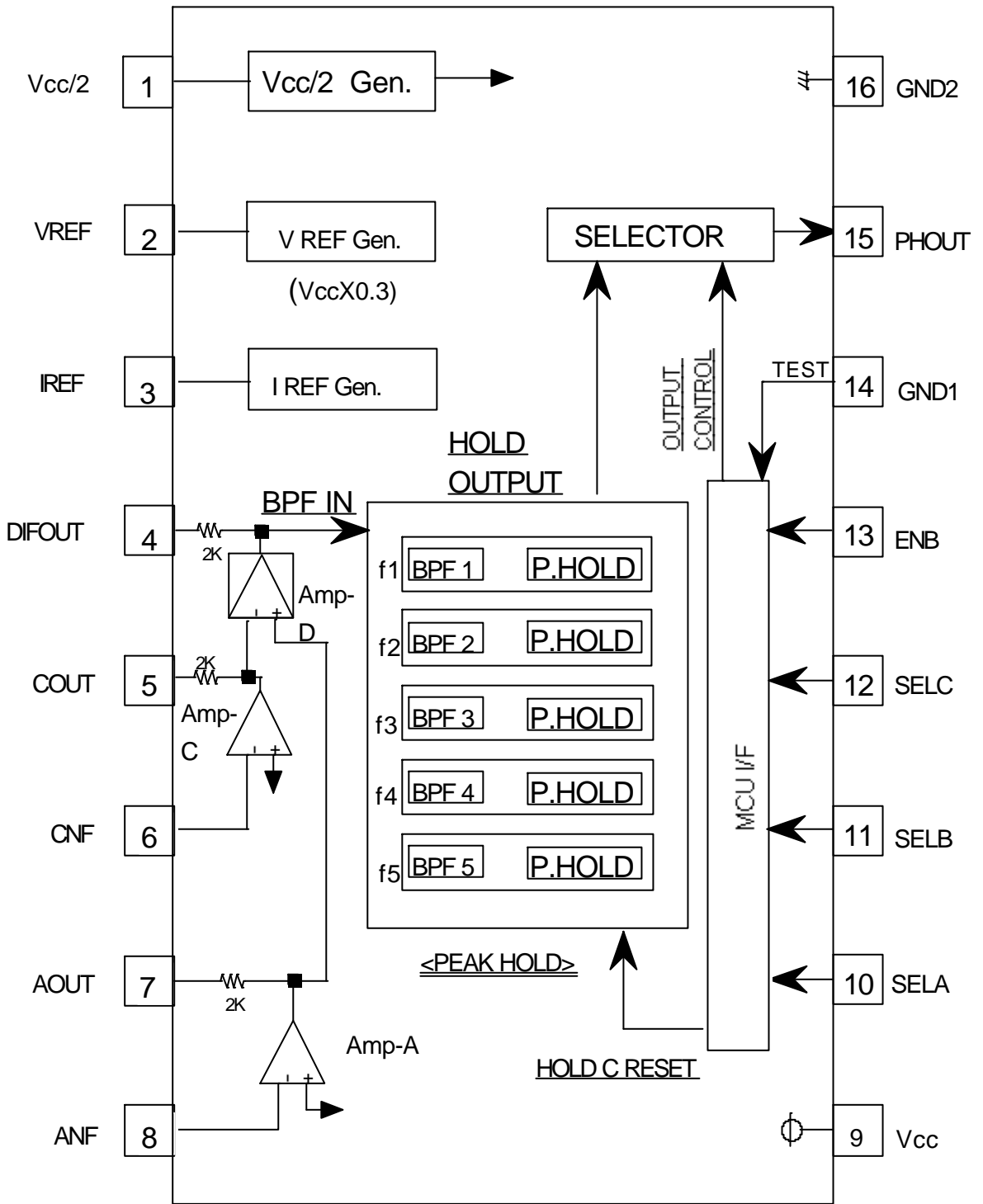
Supply voltage range ——— 4.5 to 6.5V

Rated supply voltage ——— 5.0V

## SYSTEM BLOCK DIAGRAM



# BLOCK DIAGRAM



(Notes)  $f_1=105\text{Hz}$ ,  $f_2=340\text{Hz}$ ,  $f_3=1\text{KHz}$ ,  $f_4=3.4\text{KHz}$ ,  $f_5=10.5\text{KHz}$

(The value is the design value)

Units Resistance :  $\Omega$   
Capacitance: F

## FUNCTIONAL DESCRIPTION

(1)The audio signal amplified by Amp-A and Amp-D into BPF/peak hold circuit for spectrum analyzer display.

Because the last output signal inputs into A/D of microprocessor.

The Vcc,GND had better be common with Vcc,GND of A/D of maicroprocessor.

It utilizes effect of common-mode rejection of Amp-D.Amp-C is the input amplifier to reject common-mode signal(noise).To get to good ground isolation.

(2)BPF/peak hold circuit is fit for 5 band spectrum analyzer display.

<center frequency>

f1=105Hz

f2=340Hz

f3=1KHz

f4=3.4KHz

f5=10.5KHz

(The value is the design value)

Center frequency and Q of BPF is

$\omega_0 = gm/C$

gm:matual conductance of inside amplifier circuit

(It depends on outside resistor value of Pin.No.3)

C:inside capacitor

$Q = (R1+R2)/R1$ :it is fixed by inside resistor ratio.

(The design value of Q is 3.5)

(3)The hold capacitor of peak hold circuit is included.

The reset(discharge) signal is made automatically after ending the output of hold value(Discharge pulse effect:-3dB(typ).fall refer to output value)

(4)The internal output voltage of peak hold circuit is refered to Vcc/2.

(Pin.No.1)

When it is selected by the output select circuit,it appear at PHout

(Pin.No.15) refered to GND.

## PIN DESCRIPTION

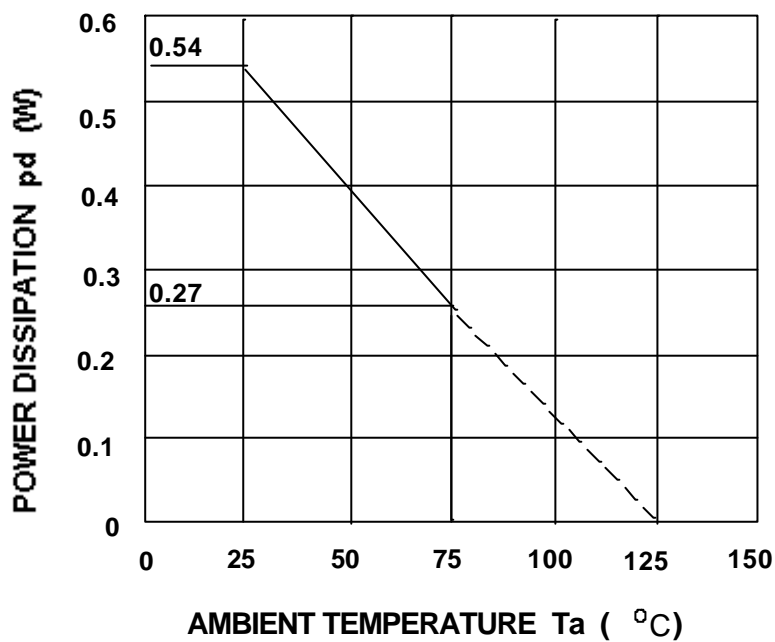
PIN No.	Name	I/O	Function
1	Vcc/2	I	1/2Vcc bias
2	VREF	I	0.3Vcc bias
3	IREF	I	BPF center frequency setting current terminal
4	DIFOUT	O	Output of amplifier-D(BPF input signal)
5	COUT	O	Output of amplifier-C
6	CNF	I	Inverted input of amplifier-C
7	AOUT	O	Output of amplifier-A
8	ANF	I	Inverted input of amplifier-A
9	Vcc	I	System supply
10	SELA	I	Output setting control terminal A(logic input)
11	SELB	I	Output setting control terminal B(logic input)
12	SELC	I	Output setting control terminal C(logic input)
13	ENB	I	Output setting control enable terminal(logic input)
14	GND1	I	Ground 1
15	PHOUT	O	Peak hold output terminal
16	GND2	I	Ground 2

PIN No.	Name	I/O	Peripheral circuit of pins
1	V <sub>cc</sub> /2	I	
2	VREF	I	
3	IREF	I	
4	DIFOUT	O	
5	COUT	O	
6	CNF	I	
7	AOUT	O	
8	ANF	I	
9	V <sub>cc</sub>	I	Supply
10	SELA	I	
11	SELB	I	
12	SELC	I	
13	ENB	I	
14	GND1	I	Ground1
15	PHOUT	O	
16	GND2	I	Ground2

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>cc(max)</sub>	Supply Voltage		7	V
P <sub>d</sub>	Power dissipation	T <sub>a</sub> ≤ 25 °C	540	mW
K $\theta$	Thermal derating	T <sub>a</sub> > 25 °C	5.4	mW/ °C
T <sub>opr</sub>	Operating temperature		-20 to +75	°C
T <sub>stg</sub>	Storage temperature		-40 to +125	°C
V <sub>i(max)</sub>	Input voltage range		GND-0.3 to V <sub>cc</sub> +0.3	V
V <sub>o(max)</sub>	Output voltage range		GND to V <sub>cc</sub>	V

Thermal derating(maximum rating)



## Recommended operating conditions

(Ta=25 °C unless otherwise noted)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Supply voltage	V <sub>CC</sub>		4.5	5.0	6.5	V
Logic input H level voltage	V <sub>IH</sub>	V <sub>CC</sub> =5V	2.5	—	V <sub>CC</sub>	V
Logic input L level voltage	V <sub>IL</sub>	V <sub>CC</sub> =5V	GND	—	0.5	V

(Note 1)

The center frequency characteristics of BPF are determined by the resistor connected between 3pin terminal and GND. If it is necessary, adjust the resistor value (note: all bands will be shifted together).

The Q of BPF is fixed in 3.5 by inside circuit.

(Note 2)

The internal output resistor of peak hold output (PIN 15) is 10kΩ typ.

The input resistance of the microprocessor must be much larger than 10kΩ.

(Note 3)

The control voltage from the microprocessor must be from GND -0.3V to V<sub>CC</sub>+0.3V.

If the control voltage is out of the above range.

It's necessary to modify the control voltage in the above range by using resistors or diodes.

# OUTPUT CONTROL SPECIFICATION

## <Output select logic table>

PHout (PinNo.15)	ENB	SELA	SELB	SELC	Note
GND(output stop)	0	X	X	X	X:Don't Care
GND	1	0	0	0	
f1:105Hz	1	0	0	1	
f2:340Hz	1	0	1	0	
GND	1	0	1	1	
f3:1kHz	1	1	0	0	
GND	1	1	0	1	
f4:3.4kHz	1	1	1	0	
f5:10.5kHz	1	1	1	1	

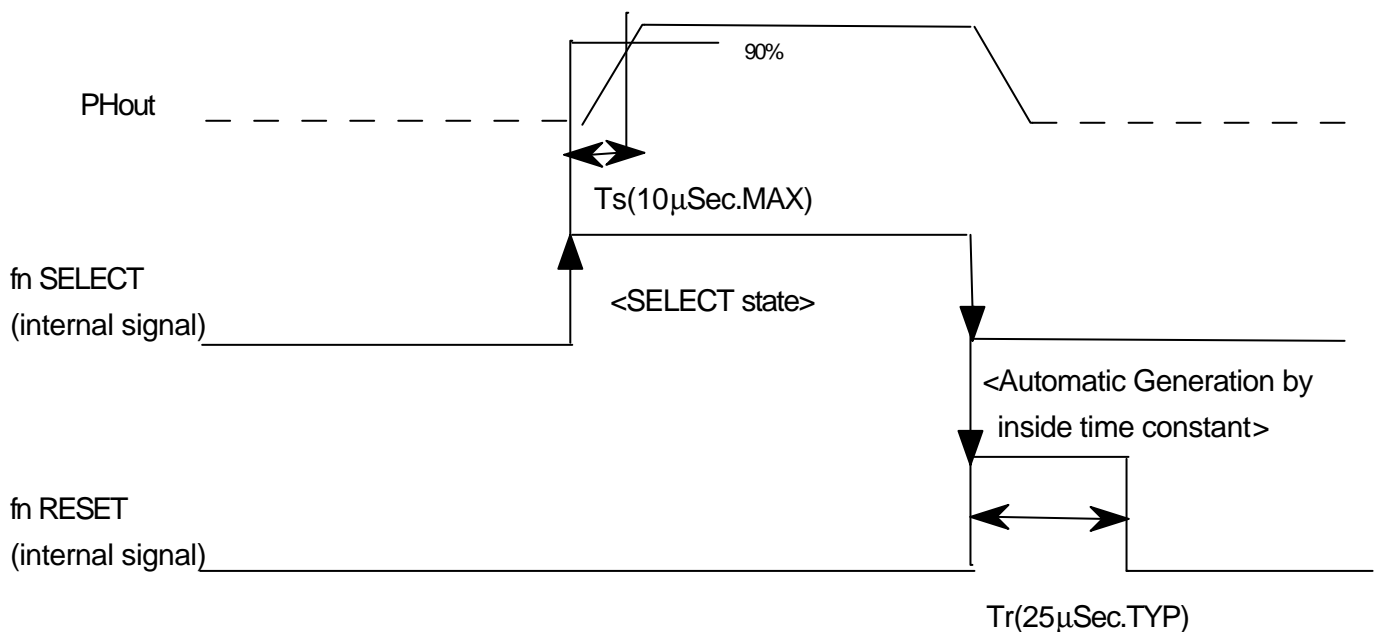
### <Note 1>

'H'=low level,'1'=high level,'X'='0'or'1'

### <Note 2>

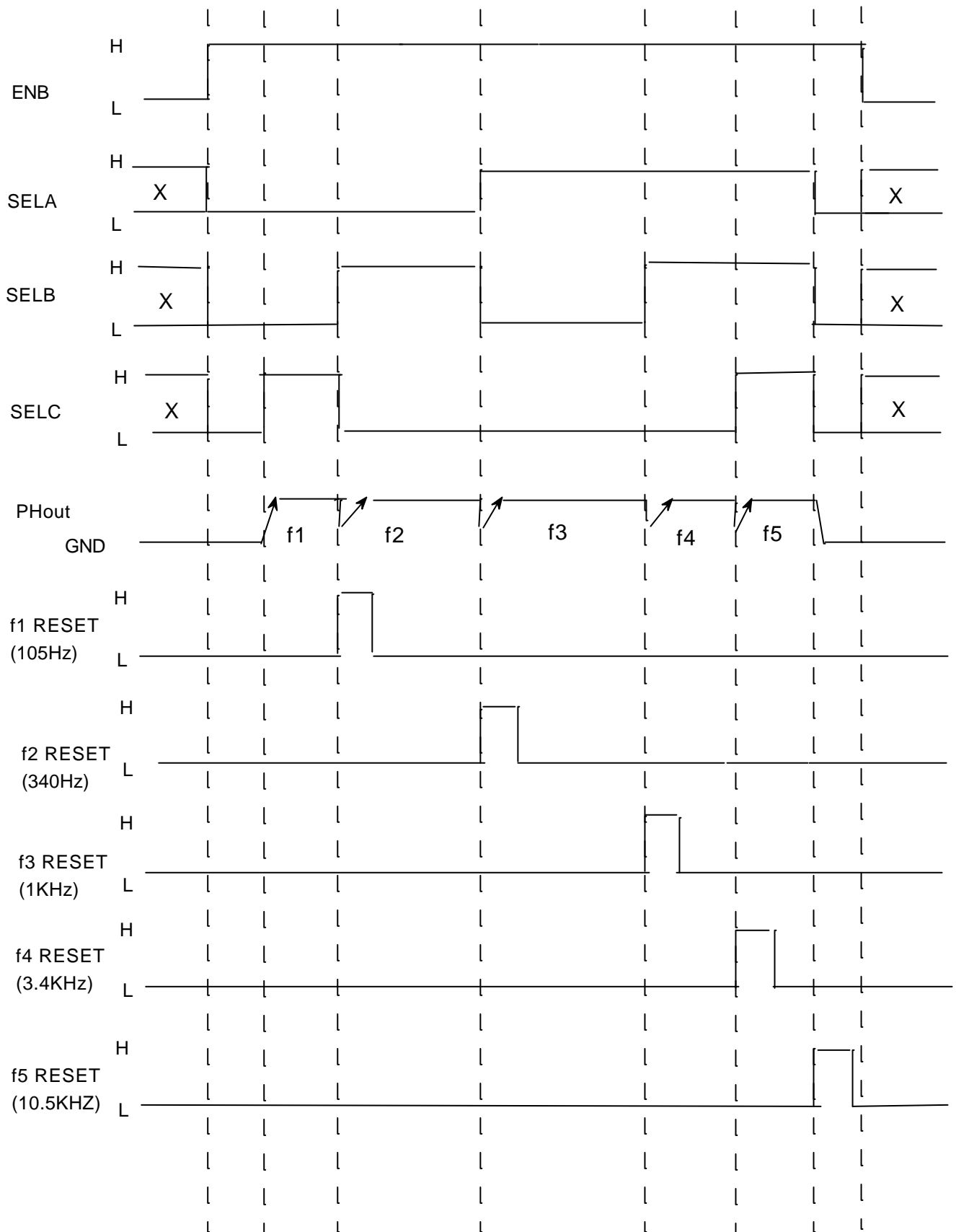
The output setting time is more than 10 $\mu$ sec.

(When the output setting time is short,the output value and reset signal become unstable)





# TIMING CHART

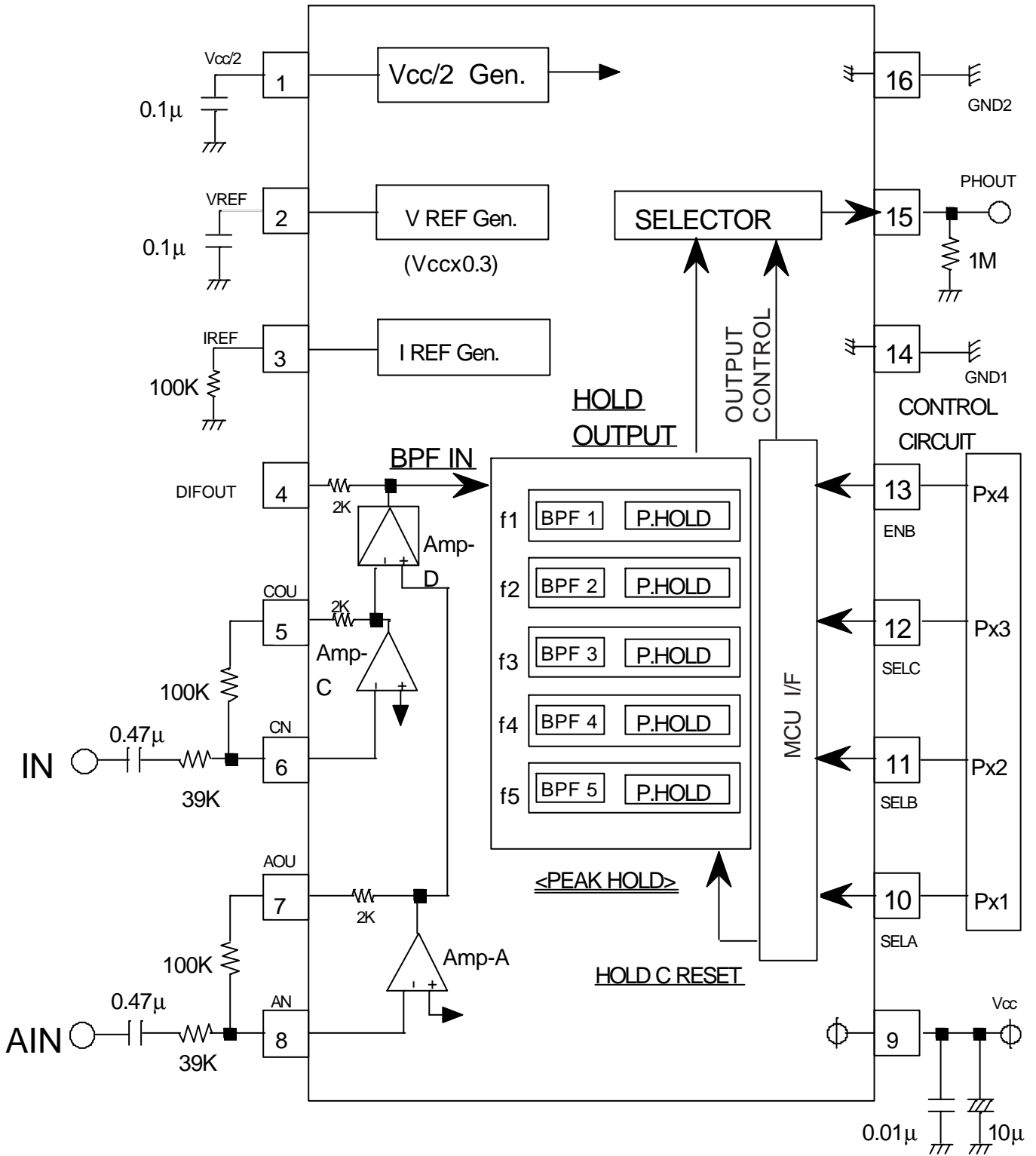


## ELECTRICAL CHARACTERISTICS

( $T_a=25\text{ }^\circ\text{C}$ ,  $V_{cc}=5.0\text{V}$ ,  $P_{Hout}(\text{Pin.No.15})R_L=1\text{M}\Omega$  unless otherwise noted.  $V_{AIN}=-30\text{dBV}$ ,  $f=1\text{KHz}$ ,  $\text{ENB}(\text{Pin.No.13})=1$ )

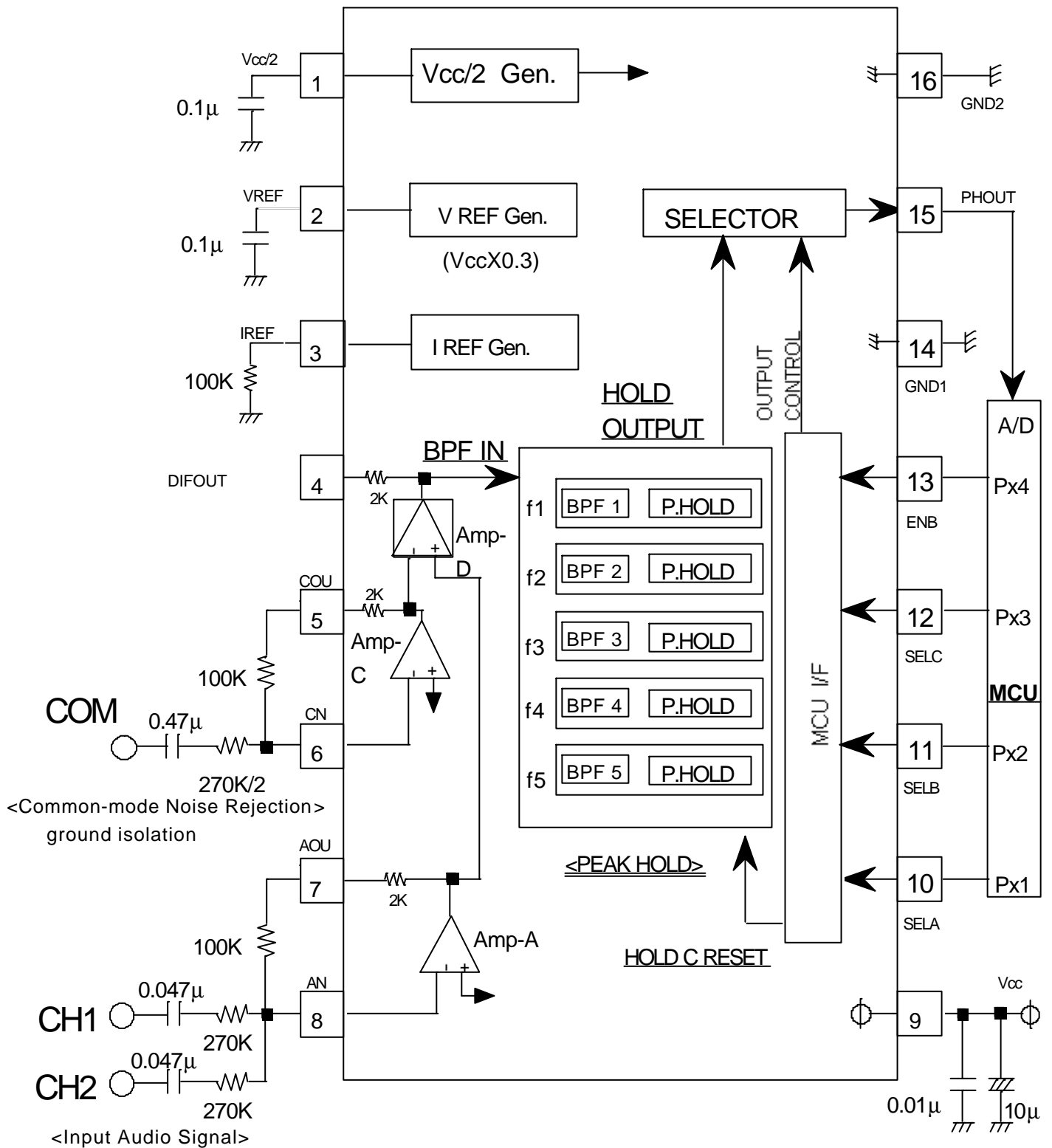
Parameter	Symbol	Condition	Limits			Unit
			Min	typ	Max	
Circuit current	$I_{cc}$	No signal, No select ( $\text{ENB}, \text{SELA}, \text{SELB}, \text{SELC}=0$ )	—	8	13	mA
Maximum output level	$V_o$	f1 to f5 Measured at each output ( $V_{AIN}=-14\text{dBV}$ )	4.0	4.7	—	V
Output offset voltage	$V_{os}$	f1 to f5 Measured at each output (No signal, $\text{ENB}=0/1$ )	—	30	60	mV
Logic input H level	$V_{IH}$		2.5	5.0	$V_{cc}+0.3$	V
Logic input L level	$V_{IL}$		GND -0.3	0	0.5	V
Common-mode rejection ratio	CMRR		25	50	—	dB
f1 output level	$V_{o1}$	f1( $f_{in}=80$ to $130\text{Hz}$ )	0.5	1.0	1.70	V
f2 output level	$V_{o2}$	f2( $f_{in}=270$ to $410\text{Hz}$ )	0.5	1.0	1.70	V
f3 output level	$V_{o3}$	f3( $f_{in}=0.8$ to $1.2\text{KHz}$ )	0.5	1.0	1.70	V
f4 output level	$V_{o4}$	f4( $f_{in}=2.7$ to $4.1\text{KHz}$ )	0.5	1.0	1.70	V
f5 output level	$V_{o5}$	f5( $f_{in}=8.0$ to $13.0\text{KHz}$ )	0.5	1.0	1.70	V
Output response time	$T_s$	The time from the rise of output selection until the rise of $P_{Hout}$ (90% of peak)	—	5	10	$\mu\text{sec}$
Discharge level	DS	<Reference> Inside reset signal $T_r=25\mu\text{secTYP.}$	—	-3	—	dB

# TEST CIRCUIT



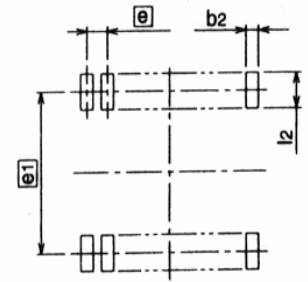
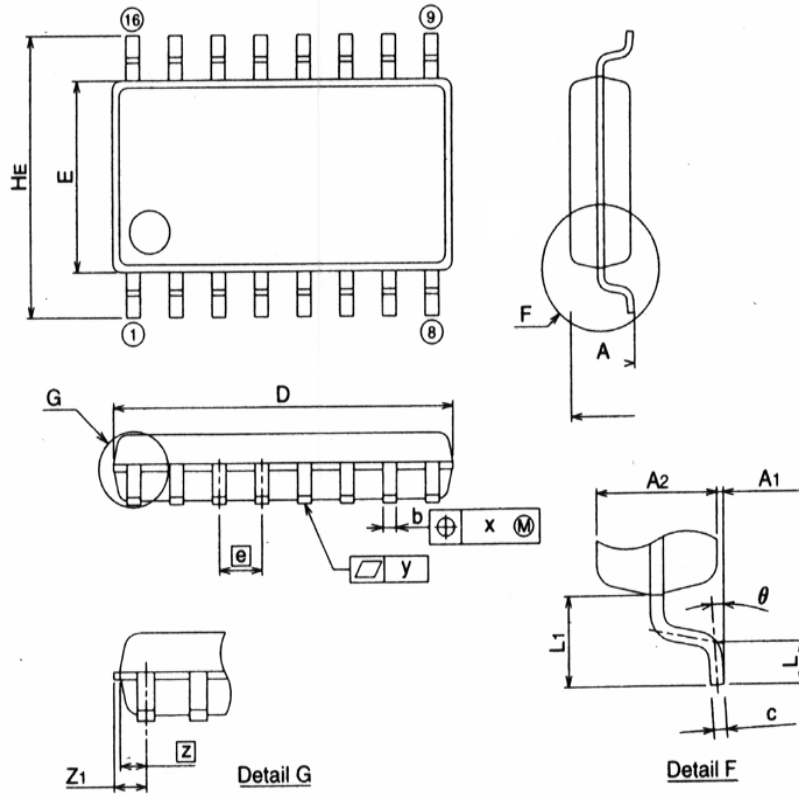
Units resistance:Ω  
 capacitance:F

# APPLICATION EXAMPLE



Units resistance:  $\Omega$   
 capacitance: F

# OUTLINE



Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A			2.1
A1	0	0.1	0.2
A2	-	1.8	-
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	10.0	10.1	10.2
E	5.2	5.3	5.4
e	-	1.27	-
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	-	1.25	-
Z	-	0.605	-
Z1	-	-	0.755
x	-	-	0.25
y	-	-	0.1
$\theta$	0°	-	8°
b2	-	0.76	-
e1	-	7.62	-
l2	1.27	-	-