

M63160J

STEPPING MOTOR DRIVER

REJ03F0038-0110Z Rev.1.1 May.21.2004

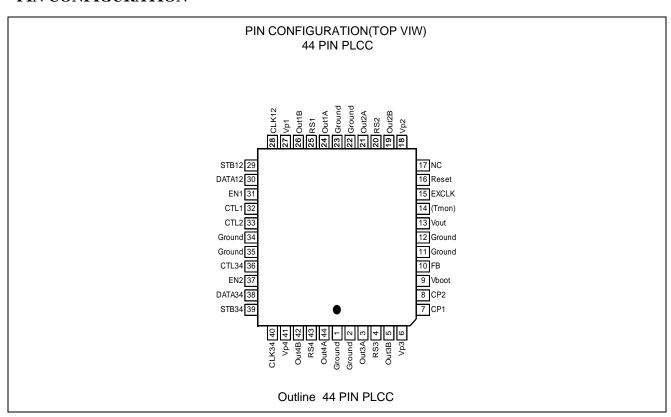
Description

This semiconductor integrated circuit includes for H bridge circuit for stepper Motor drive. Output transistor is DMOS. Motor power supply; is possible to drive until 52V maximum.

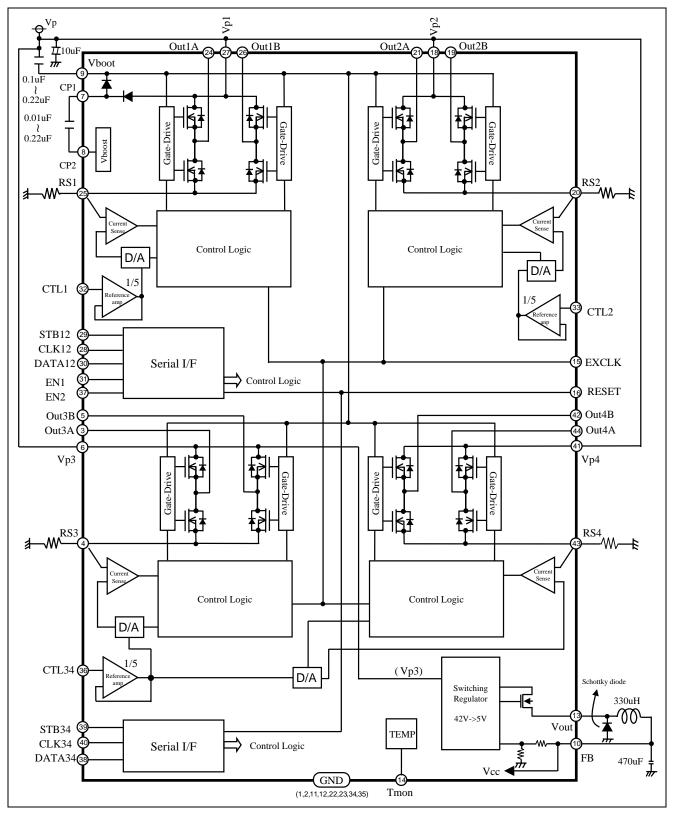
Function Outline

- 1. Maximum output current: Peak 2.0A
- 2. Low output 's Ron.: 1.1Ω
- 3. Includes two stepping motor driver circuit
 - * Two DC Motor and One Stepping Motor possible to drive.
- 4. Motor control by serial interface.(Frequency=20MHz maximum)
- 5. Includes 5V- switching regulator.
- 6. Includes thermal shut down circuit

PIN CONFIGURATION



Block Diagram



^{*}RS resistance is setting up in the limits which does not exceed Iout Max.

Pin Function

| TERMINAL | SYMBOL | TERMINAL FUNCTION | TERMINAL | SYMBOL | TERMINAL FUNCTION |
|----------|--------|-------------------------|----------|--------|-------------------------|
| 1 | Ground | GND | 23 | Ground | GND |
| 2 | Ground | GND | 24 | Out1A | Motor drive output1A |
| 3 | Out3A | Motor drive output3A | 25 | RS1 | Current sense 1 |
| 4 | RS3 | Current sense 3 | 26 | Out1B | Motor drive output1B |
| 5 | Out3B | Motor drive output3B | 27 | Vp1 | Motor power supply 1 |
| 6 | Vp3 | Motor power supply 3 | 28 | CLK12 | Clock in terminal 12 |
| 7 | CP1 | Coupling capacitor1 | 29 | STB12 | Stand by mode select 12 |
| 8 | CP2 | Coupling capacitor2 | 30 | DATA12 | Data input terminal 12 |
| 9 | Vboot | Bootstrap voltage | 31 | EN1 | Enable 1 |
| 10 | FB | Feed back | 32 | CTL1 | Reference control 1 |
| 11 | Ground | GND | 33 | CTL2 | Reference control 2 |
| 12 | Ground | GND | 34 | Ground | GND |
| 13 | Vout | Voltage output | 35 | Ground | GND |
| 14 | (Tmon) | Temperature monitor | 36 | CTL34 | Reference control 34 |
| 15 | EXCLK | External input terminal | 37 | EN2 | Enable 2 |
| 16 | RESET | RESET | 38 | DATA34 | Data input terminal 34 |
| 17 | NC | No contact | 39 | STB34 | Stand by mode select 34 |
| 18 | Vp2 | Motor power supply 2 | 40 | CLK34 | Clock in terminal 34 |
| 19 | Out2B | Motor drive output2B | 41 | Vp4 | Motor power supply 4 |
| 20 | RS2 | Current sense 2 | 42 | Out4B | Motor drive output4B |
| 21 | Out2A | Motor drive output2A | 43 | RS4 | Current sense 4 |
| 22 | Ground | GND | 44 | Out4A | Motor drive output4A |

Absolute Maximam Rating

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|--------|----------------------------|---------------------------------|-------------|------|
| VBOOT | Bootstrap voltage | | 65 | V |
| VP | Motor power supply | | 52 | V |
| Vcc | Power supply | | 6.5 | V |
| lout | Motor output current | | 2.0 | Α |
| Vin | Input voltage of terminals | | -0.3 to 6.5 | V |
| Pt | Power dissipation | Ta=25°C, Grass epoxy board base | 2.5W | W |
| Кθ | Thermal dissipation | Ta=25°C, Grass epoxy board base | 40 | °C/W |
| Tj | Junction temperature | | 150 | °C |
| Topr | Movement Circumference | | -20 to 75 | °C |
| | temperature | | | |
| Tstg | Storage temperature | | -40 to 125 | °C |

Recommended Operating Conditions

(Ta =25°C)

| | | LIMITS | | | |
|--------|------------------------|-------------|--------|--------|------|
| SYMBOL | PARAMETER | MINIMUM | TYPCAL | MAXMUM | UNIT |
| VBOOT | Bootstrap voltage | _ | 52.6 | 61.2 | V |
| Vref | Control Voltage | 0.1 | 2.5 | 2.9 | V |
| VP | Motor power supply | 19.0 — 46.2 | | V | |
| * lout | Motor Current supply | _ | 1.2 | 1.5 | Α |
| EXTCLK | EXTCLK input frequency | 1.8 | 4.0 | 6.1 | MHz |

^{*} Junction temperature at 150°C within

Logic Input Terminal

| SYMBOL | CONDITION | |
|--------|-----------|--|
| STB | Pull Down | |
| CLK | Pull Down | |
| DATA | Pull Down | |
| EN1 | Pull Down | |
| EN2 | Pull Down | |
| RESET | Pull Down | |

Electrical Characteristics

(Ta=25°C, VP=42V unless otherwise noted)

| | | | LIMITS | | | , |
|-----------------|---|---|---------|-----------------|--------|------|
| SYMBOL | PARAMETER | CONDITIONS | MINIMUM | TYPCAL | MAXMUM | UNIT |
| Common Blo | ock | | | | | |
| ICC-L | ICC-L Vcc standby current VCC=5 of Moto | | _ | 5.5 | 7 | mA |
| IM-L | Motor stop current | VP=42V, Circuit current of Motor stopping | _ | 6.0 | 7.5 | mA |
| Vboot | Bootstrap voltage | | _ | 52.6 | 61.2 | V |
| Fcp1 | Bootstrap frequency | | 150 | 200 | 250 | kHz |
| Lvoldl | Regulator voltage detector | The case of supply voltage decreasing | _ | LvoldH -Vhys | _ | V |
| LvoldH | Regulator voltage detector | The case of supply voltage increasing | 4.18 | 4.4 | 4.62 | V |
| Vhys | Vhys | | 180 | 200 | 220 | mV |
| Tmon | Tmon Voltage | Ta=25°C | 710 | 740 | 770 | mV |
| [Power Block | k] | | | | | |
| Ron1 | Output RDS(ON) | Total of top and bottom (Ta=25°C) | _ | 1.1 | 1.4 | Ω |
| Ron2 | Output RDS(ON) | Total of top and bottom (Ta=25°C) | _ | 1.1 | 1.4 | Ω |
| [Logic Input | Terminal] | | | | | |
| VinH | Serial port input voltage High | | 2 | _ | REGout | V |
| VinL | Serial port input voltage Low | | 0 | _ | 0.8 | V |
| linH | Serial port input current High | V force:5V | 50 | 100 | 200 | μΑ |
| linL | Serial port input current Low | V force:0V | -10 | 0 | +10 | μΑ |
| [Serial port] | | | | | | |
| fsclk | Serial port clock frequency | CLK12, CLK34 | _ | _ | 20 | MHz |
| tset | Serial port setup time | | 12.5 | _ | _ | nS |
| thold | Serial port hold time | | 10 | _ | _ | nS |
| [Switching re | egulator] | | | | | |
| REGout1 | 5V regulator output voltage1 | Load current :300mA VP voltage :10V to 47V | 4.75 | 5.00 | 5.25 | V |
| Fclk-Reg | Clock frequency | | 75 | 100 | 125 | kHz |
| Rds(on)- Reg | Sw.RegON | | _ | 0.7 | _ | Ω |
| Sfts | Soft Start | | 5 | 10 | 15 | ms |
| Climit | Output Limits Voltage | Load current : 600mA to 1.2A | _ | 4.75 | _ | V |
| Climit | Cut of FB Voltage | | 0.8 | 1.2 | 1.5 | A |
| lout | REG Output Current | | | 300 | 500 | mA |
| EFFI1 | Efficiency (Design Value) | VP=42V L=330uH C=470μF lout=300mA | _ | 70 | _ | % |
| EFFI2 | Efficiency (Design Value) | VP=15 VL=330uH C=470μF lout=300mA | _ | 80 | _ | % |

(Ta=25°C, VP=42V unless otherwise noted)

| | | - | _ | - |
|--|----|----|---|---|
| | ın | лι | | c |
| | | | | |

| | | 21111113 | | | | |
|--------|-----------------------|--|---------|--------|--------|--------------|
| SYMBOL | PARAMETER | CONDITIONS | MINIMUM | TYPCAL | MAXMUM | UNIT |
| Exdt | External PWM Delay | lout=±1A 50% to 90% | | | | ns |
| | Time | PWM change to source ON | 200 | 500 | 800 | - |
| | | PWM change to source OFF | 50 | 100 | 200 | _ |
| | | PWM change to sink ON | 200 | 500 | 800 | - |
| | | PWM change to sink OFF | 50 | 100 | 200 | - |
| | | Phase change to source ON | 200 | 500 | 800 | _ |
| | | Phase change to source OFF | 50 | 100 | 200 | _ |
| | | Phase change to sink ON | 200 | 500 | 800 | _ |
| | | Phase change to sink OFF | 50 | 100 | 200 | _ |
| Svol1 | Sense Voltage1 | Current ratio 100% Vref(CTL)=2.0V | 384 | 400 | 416 | mV |
| Svol2 | Sense Voltage2 | Current ratio 26.08% Vref(CTL)=2.0V | 93 | 104 | 115 | mV |
| Ictl | Control Input Current | CTL-GND Current | 0.5 | 3 | 5 | μΑ |

Thermal Characteristics

| | | Function | start temper | ature of IC | _ |
|--------|-------------------|----------|--------------|-------------|------|
| SYMBOL | PARAMETER | MINIMUM | TYPCAL | MAXMUM | UNIT |
| TSD | Thermal shut down | _ | 165 | _ | °C |
| ΔHys | TSD Hys | | 35 | | °C |

| | | | LIMITS | | | |
|-------------|----------------|------------------------------------|---------|--------|--------|-------|
| SYMBOL | PARAMETER | CONDITIONS | MINIMUM | TYPCAL | MAXMUM | UNIT |
| Motor Block | Motor Block | | | | | |
| [Power Bloc | k] | | | | | |
| Ron1-125 | Output RDS(ON) | Total of top and bottom (Ta=125°C) | _ | 1.65 | 2.0 | Ω |
| Ron2-125 | Output RDS(ON) | Total of top and bottom | _ | 1.65 | 2.0 | Ω |
| ΔTmon | Tmon | | -1.90 | -1.72 | -1.55 | mV/°C |

Switching Regulator

Explanation

- 1. When using it usually through a switching regulator It is as a 2/15- page block diagram between Vout and FB terminal. Please connect a coil capacitor diode .
- 2. When S/W- REG is not used but voltage is given to a direct FB terminal from the exterior A coil capacitor diode is unnecessary.

Protection function

When voltage is given to a direct FB terminal from the exterior, Current can decrease by about 1mA at the time of Vp standby.

- Vout terminal 1. It has the Gnd short protection function at the time of starting.l
 - 2. It does not have the Gnd short protection function under operation.

FB terminal

- 1. The Gnd short protection function at the time of starting serves as only a current limit.
- 2. During operation, it has the function to make Vout turn off by combined use of current limit detection and a Low Voltage detection machine.

Sequence of operation at the time of starting.

Usually, a state: Power supply injection \rightarrow With no GND short \rightarrow Vout-FB and charge pump operation

GND short state: Power supply injection \rightarrow GND short \rightarrow Vout-FB un-operating Charge pump operation

Sequence during operation.

Vout GND short: Vout operation \rightarrow GND short judging \rightarrow Vout-FB and charge pump operation

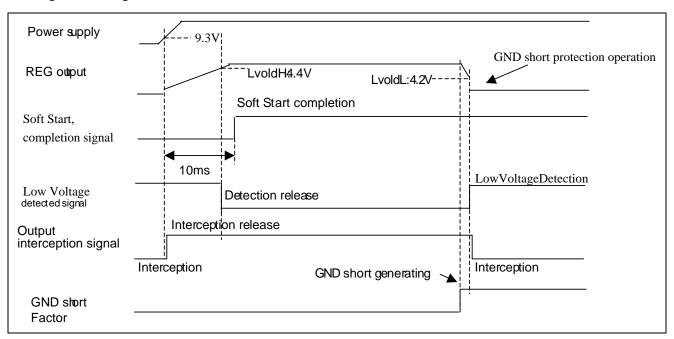
FB GND short: FB operation \rightarrow Current limit operation \rightarrow GND short judging \rightarrow Vout-FB OFF. Charge pump operation

When FB voltage becomes less than [more than 1us4.2V] by current limit detection It becomes a GND short judging and Vout ismade to turn off.

RENESAS

*1 GND short detection function: GND short detection performs GND short detection at the time of starting, It does not have the GND short detection function under operation.

A sequence of operation



Function setup (all initial value is 0, At TSD it is all 0) RESET initialization = "H"

Ch1:

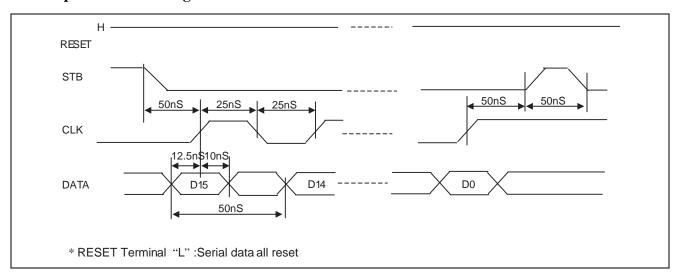
| | OUT1 | OUT2 | OUT1,2 |
|-----|-------------------------|-------------------------|-------------------------|
| D0 | Blank Time LSB | Blank Time LSB | OUT 2 Internal PWM Mode |
| D1 | Blank Time MSB | Blank Time MSB | OUT2 External PWM Mode |
| D2 | Off Time LSB | Off Time LSB | OUT 2 Phase |
| D3 | Off Time Bit1 | Off Time Bit1 | OUT 2 DAC LSB |
| D4 | Off Time Bit2 | Off Time Bit2 | OUT 2 DAC Bit 2 |
| D5 | Off Time Bit3 | Off Time Bit3 | OUT 2 DAC Bit 3 |
| D6 | Off Time MSB | Off Time MSB | OUT 2 DAC Bit MSB |
| D7 | Fast Decay Time Bit LSB | Fast Decay Time Bit LSB | OUT 1 internal PWM Mode |
| D8 | Fast Decay Time Bit 1 | Fast Decay Time Bit 1 | OUT 1 External PWM Mode |
| D9 | Fast Decay time Bit 2 | Fast Decay time Bit 2 | OUT 1 Phase |
| D10 | Fast Decay time MSB | Fast Decay time MSB | OUT 1 DAC LSB |
| D11 | Sync.Rect.Control | Sync.Rect.Control | OUT 1 DAC Bit 2 |
| D12 | Sync.Rect.Enable | Sync.Rect.Enable | OUT 1 DAC Bit 3 |
| D13 | Don't care | Don't care | OUT 1 DAC Bit MSB |
| D14 | Word Select 0=0 | Word Select 0=1 | Word Select 0=0 |
| D15 | Word Select 1=0 | Word Select 1=0 | Word Select 1=1 |
| | | | |

Ch2:

| | OUT3,4 | For TEST | OUT3,4 |
|-----|-------------------------|-----------------|-------------------------|
| D0 | Blank Time LSB | For TEST | OUT 4 Internal PWM Mode |
| D1 | Blank Time MSB | For TEST | Don't care |
| D2 | Off Time LSB | For TEST | OUT 4 Phase |
| D3 | Off Time Bit1 | For TEST | OUT 4 DAC LSB |
| D4 | Off Time Bit2 | For TEST | OUT 4 DAC Bit 2 |
| D5 | Off Time Bit3 | For TEST | OUT 4 DAC Bit 3 |
| D6 | Off Time MSB | For TEST | OUT 4 DAC Bit MSB |
| D7 | Fast Decay Time Bit LSB | For TEST | OUT 3 internal PWM Mode |
| D8 | Fast Decay Time Bit 1 | For TEST | Don't care |
| D9 | Fast Decay time Bit 2 | For TEST | OUT 3 Phase |
| D10 | Fast Decay time MSB | For TEST | OUT 3 DAC LSB |
| D11 | Sync.Rect.Control | For TEST | OUT 3 DAC Bit 2 |
| D12 | Sync.Rect.Enable | For TEST | OUT 3 DAC Bit 3 |
| D13 | Don't care | For TEST | OUT 3 DAC Bit MSB |
| D14 | Word Select 0=0 | Word Select 0=1 | Word Select 0=0 |
| D15 | Word Select 1=0 | Word Select 1=0 | Word Select 1=1 |

^{*} RESET Early Condition = "H"

Serial port Write Timing



A motor control logic condition and explanation

- 1, Data setup
 - 1-1, Data taking in: CLK rising edge
 - 1-2, Data input 1: It carries out in order of D15 > D0.
 - 1-3, Data input 2: A Mode setup is performed after initial setting.
 - 1-4, Every 16 bits, it is a STB signal and it is Closed.
 - 1-5, A data setup of Ch2 For Test is not performed.
 - 1-6, Sync.Rect.Control "Active" At the time of a setup, The inside of Fast Decay performs negative voltage detection. FET is set to all OFF when current flows in the right direction.
- 2, RESET terminal

Low: All data reset(All FET OFF)High: Data setup Standby state

When a RESET terminal is set to "L" and a Motor drive is performed, A REST terminal is set to "H" and serial data is re inputted.

Internal logic reset is Logic composition of a RESET terminal and a Low Voltage detection machine is performed.

When rapid high load is in FB, a Low Voltage detection machine outputs "L", Internal logic is reset when an output does not return to less than 1 μ s at "H."

RESET terminal "L" Internal logic will be in an initial state.(All FET serves as all OFF)

·A S/W- REG part continues operation.

3. EN terminal

Low: External PWM Mode Slow Decay or Fast Decay

Off Time ·Fast Decay Time: Sleep

A current detection condition setup at the time of Decay is performed by Sync.Rect.Control Active or Passive.

However, current detection is effective only at the time of Fast Decay. (Slow is invalid.)

High: Internal PWM Mode Motor drive state FET ON->OFF ->ON

4, Motor drive

Motor drive :RESET terminal "H" EN terminal "H" It drives after a Mode Data setup.

Motor STOP: RESET terminal "L" is STOP.

RESET terminal "H" EN terminal "L": It is set to Decay by External PWM Mode. All FETOFF comes after setting current detection.

EN is not related to "L or H" in early stages. It FET all turns off till control logic initial setting and the completion of a Mode setting. EN is always after control logic initial setting and the completion of a Mode setting at "L.", If it is External PWM Slow Decay Mode, it is Start about Slow Decay.

(It FET all turns off at the time of Fast Decay Mode.)

After control logic initial setting and the completion of a Mode setting, FET is set to being turned on by EN "H" and it is compulsorily set to Decay Mode by EN "L."

However, even if a setup of External PWM Slow Decay Mode is EN "L", it is reflected.

5, Current detection by Decay

The conditions which perform current detection by Decay

Internal PWM: Sync.Rect.EnableControl1 "H", Inside of Fast Decay in Mixed Decay Mode

External PWM: Sync.Rect.EnableControl1 "H", Fast Decay Mode

In addition, Decay current detection is not performed on conditions.

Internal PWM: It changes to Decay from FET ON by the current detection COM., Fast Decay Time-OffTime starts in this stage. It is Start about the current detection in Decay, Fast Decay Time as a trigger. Detection is stopped after Fast Decay Time completion.

When setting Decay current is detected during Fast Decay time, FET is all turned off only within Fast Decay time.

It is referred to as Slow Decay till OFF Time completion after Fast Decay completion.

External PWM: With EN terminal "L", it goes into Regeneration Mode compulsorily. Decay current detection is

Started to a trigger for the signal of EN "L." Detection is continued until the reversal signal from COM comes out.

Decay current detection serves as [EN] STOP by "H", and FET is turned on

BlankTime of OUT1 OUT2 & OUT3 OUT4

| D0 | D1 | BLANKTIME |
|----|----|-----------|
| 0 | 0 | 4/ fosc |
| 0 | 1 | 6/fosc |
| 1 | 0 | 12/fosc |
| 1 | 1 | 24/ fosc |

Fixed-Off Time control of OUT1 • OUT2 & OUT3 • OUT4 With D2-D6

Toff=(8[1+N]/fosc)- 1/ fosc Where N = 0...31

Fast Decay Time control of OUT1-OUT2 & OUT3 - OUT4 With D7-D10

Tfd=(8[1+N]/fosc)- 1/fosc Where N=0...15

Sync.Rect.Control1of OUT1 • OUT2 & OUT3-OUT4 With D11

| | Sync.Rect. | FUNCTION |
|---|------------|--|
| 0 | Active | Output turn off when output current leach to zero. |
| 1 | Passive | Reversal current bias until vref setting value. |

With D12

| | Sync.Rect. | FUNCTION |
|---|------------|---------------|
| 0 | Disable | NO Sync.Rect. |
| 1 | Enabled | Sync.Rect |

Word Select 0 / 1 of Ch1 Mode

| Select0 | Select1 | Select Mode |
|---------|---------|-------------|
| 0 | 0 | OUT1 |
| 1 | 0 | OUT2 |
| 0 | 1 | OUT1/2 |

WordSelect0 / 1 of Ch2 Mode

| Select0 | Select1 | Select Mode |
|---------|---------|-------------|
| 0 | 0 | OUT3/4- A |
| 1 | 0 | For TEST |
| 0 | 1 | OUT3/4- B |

Internal PMWMode select by OUT1/2 & OUT3/4

| | Decay Mode |
|---|------------|
| 0 | Mixed |
| 1 | Slow |

External PMWMode select by OUT1/2

| | Decay Mode |
|---|------------|
| 0 | Fast |
| 1 | Slow |

Phase control by OUT1/2

| | Phase | OUTA | OUTB |
|---|---------|------|------|
| 0 | Reverse | Low | High |
| 1 | Forward | High | Low |

DAC

| MSB | bit3 | Bit2 | LSB | Current Ratio(% |
|-----|------|------|-----|-----------------|
| 1 | 1 | 1 | 1 | 100 |
| 1 | 1 | 1 | 0 | 95.65 |
| 1 | 1 | 0 | 1 | 91.3 |
| 1 | 1 | 0 | 0 | 8695 |
| 1 | 0 | 1 | 1 | 82.61 |
| 1 | 0 | 1 | 0 | 7826 |
| 1 | 0 | 0 | 1 | 7391 |
| 1 | 0 | 0 | 0 | 6956 |
| 0 | 1 | 1 | 1 | 6087 |
| 0 | 1 | 1 | 0 | 52.17 |
| 0 | 1 | 0 | 1 | 4348 |
| 0 | 1 | 0 | 0 | 34.78 |
| 0 | 0 | 1 | 1 | 26.08 |
| 0 | 0 | 1 | 0 | 1739 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | Disable |

*ITRIP=VREF × Current Ratio/ (5×RSENSE)

Motor control functional explanation

1, Blank Time

A Mask time setup of the recovery current generated in Motor ON Timing is performed.

2, Off Time

The Motor OFF time after Itrip is set up.

3, Fast Decay Time

Fast Decay time in Mixed Decay Mode is set up.

(invalid at the time of Slow Decay and External PWM)

- 4, Sync.Rect
 - 4-1, Active :FET is all turned off by current zero among Decay.
 - 4-2, Passive :Reverse current is passed to a Vref setting value, and FET is all turned off after that.

Conditions1: Internal PWM ·Sync.Rect.EnableControl1 "H"·Mixed Decay Mode

State1: Only the inside of Fast Decay is effective.

(When not reaching into Fast Decay at the above-mentioned setting value, it moves Slow Decay)

Conditions2 :External PWM ·Sync.Rect.EnableControl1 "H" ·Fast Decay Mode

- 5, Sync.Rect.Enable
 - 5-1, Disabled :Sync.Rect.EnableControl1 "L"→Decay by the external diode is performed.
 - 5-2, Enabled :Sync.Rect.EnableControl1 "H" ">Decay with an internal transistor is performed.
- 6. Word Select

The taking- in place of serial data is set up (OUT1,OUT2,OUT1/OUT2).

7, Internal PWM

Decay is set up.

Decay Mode: Mixed /Slow

Mixed Decay: Fast Decay to Slow Decay

8, External PWM

A Decay setup at the time of the external control by EN terminal

Decay Mode :Fast /Slow

9, Phase Control

The direction to which current flows is set up.

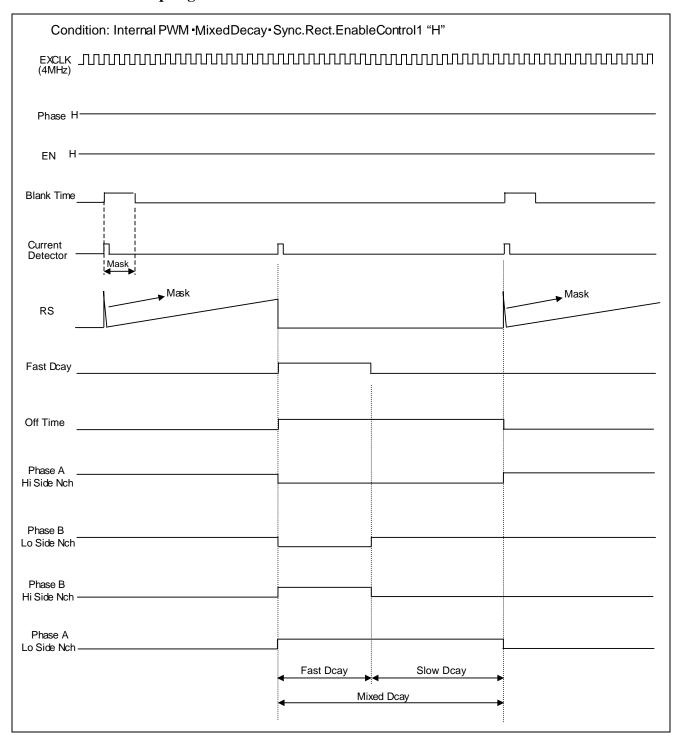
Reverse: Phase $B \rightarrow$ Phase A Forward: Phase $A \rightarrow$ Phase B

10, DAC

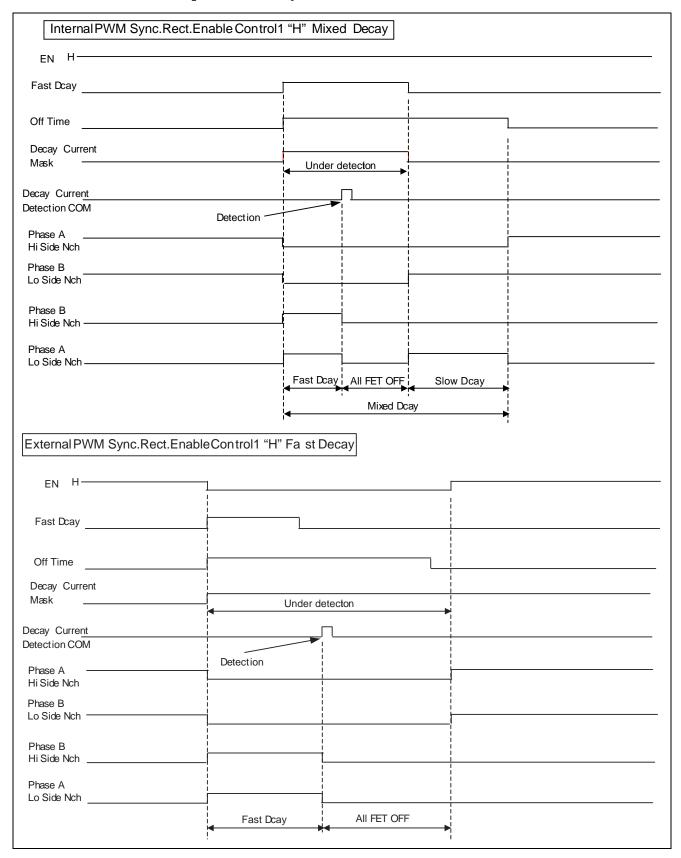
The current which FET passes is set up.

Itrip is set up.

Motor control concept figure



The current detection sequence in Decay



External PWM Mode

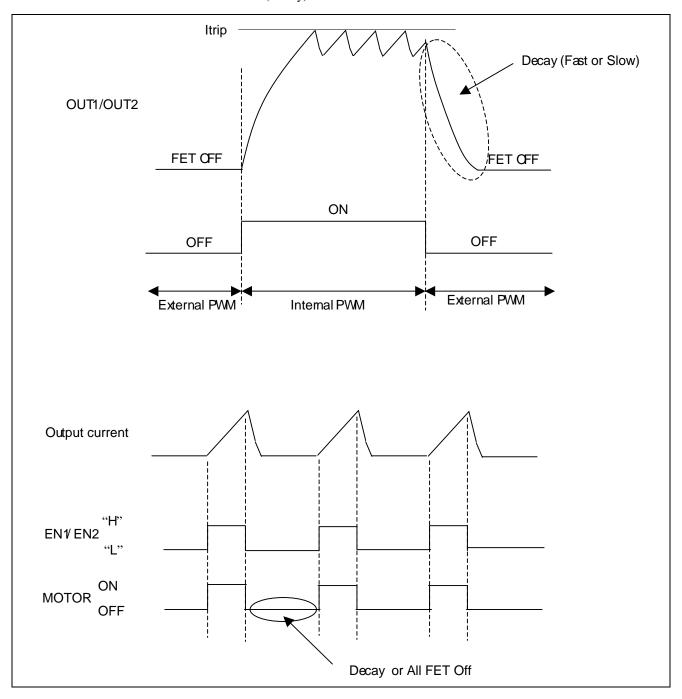
External PWM Function

Enable Logic (External PWM)

| EN1 | OUT1 | EN2 | OUT2 |
|-----|----------|-----|----------|
| 0 | External | 0 | External |
| 1 | Internal | 1 | Internal |

EN1/EN2 L->H: Motor Start(FET ON)

L=External Mode...>FET OFF(Decay)



Package Outline

44P0X

Note: Please contact Renesas Technology Corporation for further details.

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Renesas Technology (Shanghai) Co., Ltd. 26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632 Tel: <65> 6213-0200, Fax: <65> 6278-8001