

**1.1GHz/500MHz DUAL PLL FREQUENCY SYNTHESIZER FOR DIGITAL CELLULAR PHONE**

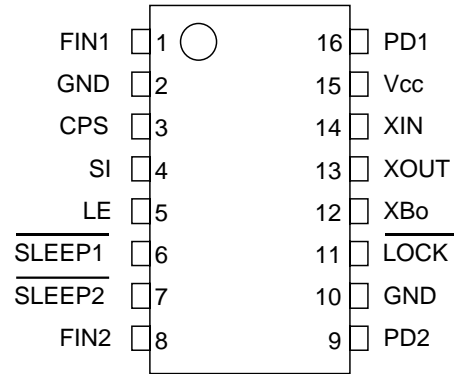
DESCRIPTION

The M64811AGP is a 1.1GHz/500MHz band two-system one-chip PLL frequency synthesizer . Using a high performance Bi-CMOS process , the product contains one two-modulus (1/32 and 1/33) prescaler that accepts inputs up to 1.1GHz and another two-modulus (1/16 and 1/17) prescaler that accepts inputs up to 500MHz ,thus helping make the equipment compact .

FEATURES

- Operating supply voltage : 2.7V~3.6V
- Operating temperature : -30°C~+85°C
- 2 PLL systems (1.1GHz and 500MHz) are on one chip  
 PLL1 : 700MHz~1.1GHz    PLL2 : 100MHz~500MHz
- Low power consumption (I<sub>cc</sub>=8mA Typ at V<sub>cc</sub>=3V) .
- Dividing ratio setting ranges :  
 FIN1 for 1.1GHz    VCO.....N(VCO1)=1,024~131,071  
 FIN2 for 500MHz    VCO.....N(VCO2)=256~131,071  
 OSC for Fref .....N(Fref)=5~2,047
- Each loop has input pin for sleep mode .  
 Power supplies to 2 loops can be independently turned ON/OFF .  
 Also can be controlled by the serial data . (When SLEEP1 and SLEEP2 is "H" . )
- The PLL standard oscillation circuit can adopt a B-E Colpitts type oscillation circuit to form a stable oscillation circuit.
- Current controlled charge pump . (I<sub>cp</sub>=±2mA const.)
- Locked condition detecting output  
 If a phase difference smaller than 3 times (Δt) of the OSC period continues for 15 periods or longer , the condition is judged as locked, and the LOCK terminal goes to "L" .  
 (When , for example , f<sub>osc</sub>=19.2 MHz , Δt=156 ns)
- PLL lock/unlock status indicate function .  
 (Judged in the system turned on if the other system is turned off . )
- Small package (16pin SSOP, lead pitch : 0.65mm)

**PIN CONFIGURATION (TOP VIEW)**

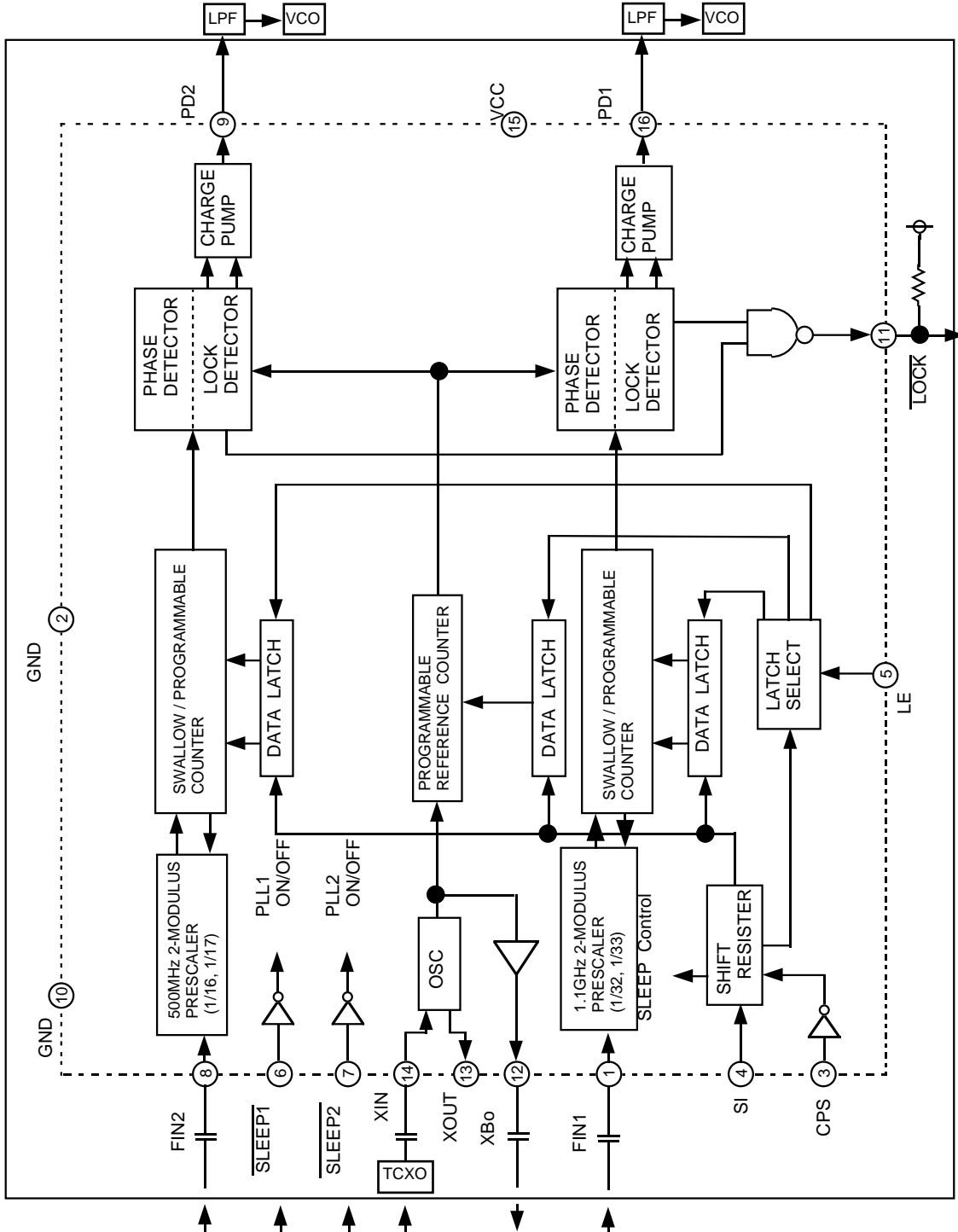


APPLICATION

- Digital cordless phone (CT2)
- Digital cellular phone (PDC)

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BLOCK DIAGRAM



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## FUNCTION DESCRIPTION OF PINS

Pin No.	Pin Identification	Description
1	FIN1	Input from the VCO , Fmax = 1.1GHz .
2	GND	Ground .
3	CPS	Clock pulse input . Shift register clock input pin .
4	SI	Binary serial data input . Shift register data input pin
5	LE	Load enable input . When LE is HIGH , data stored in the shift registers is loaded into the appropriate latch .
6	$\overline{\text{SLEEP1}}$	PLL1 power control . "H" = normal operation , "L"=power down .
7	$\overline{\text{SLEEP2}}$	PLL2 power control . "H" = normal operation , "L"=power down .
8	FIN2	Input from the VCO , Fmax = 500MHz .
9	PD2	Charge pump2 output . Tristate output . High Z when PLL2 power is off .
10	GND	Ground .
11	$\overline{\text{LOCK}}$	When loops are locked ..... "L" , When one of loops is unlocked..... "High Z" . If one loop is sleep mode , the status of the other loop is checked for judgment .
12	XBo	Buffer output of oscillator .
13	XOUT	Crystal Oscillator input .
14	XIN	
15	Vcc	Power supply . Vcc = 2.7~3.6V .
16	PD1	Charge pump1 output . Tristate output . High Z when PLL1 power is off .

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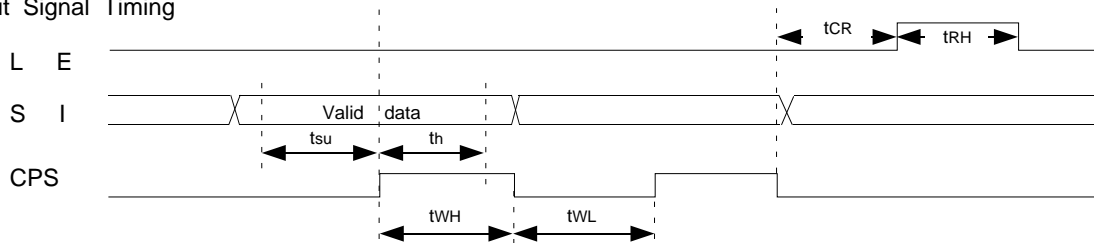
**FUNCTION DESCRIPTION**

**1.Data Input**



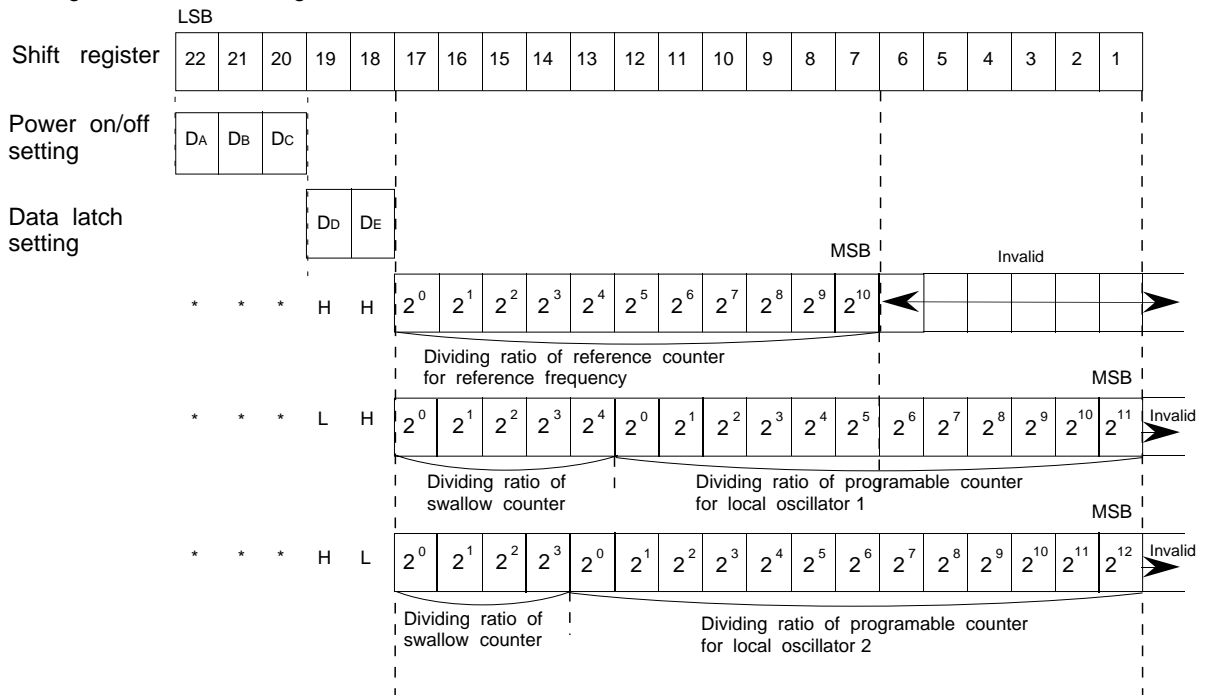
- Note 1) At the leading edge of the CPS input, the status of the SI input is written into the shift register.
- Note 2) The bit just before LE becomes "H" is LSB, and SI before MSB becomes invalid.
- Note 3) When LE is "H", the data stored in the shift registers is loaded into the appropriate latch.

**2.Input Signal Timing**



$t_{su}=t_h=t_{WH}=t_{WL}=0.1\mu\text{smin.}$   
 $t_{CR}=t_{RH}=0.1\mu\text{smin.}$

**3.Bit Configuration of Shift Register**



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Note 4) Power on/off control of PLL system is set by DA, DB, and DC.

External Control Pin		Serial Data			Description			
SLEEP1	SLEEP2	DA	DB	DC	PLL1	PLL2	OSC	XBo
L	L	*	*	*	OFF	OFF	ON	ON
L	H	0	0	*	OFF	ON	ON	ON
L	H	0	1	*	OFF	OFF	ON	ON
L	H	1	0	*	OFF	ON	ON	ON
L	H	1	1	*	OFF	OFF	ON	ON
H	L	0	0	*	ON	OFF	ON	ON
H	L	0	1	*	ON	OFF	ON	ON
H	L	1	0	*	OFF	OFF	ON	ON
H	L	1	1	*	OFF	OFF	ON	ON
H	H	1	1	1	OFF	OFF	OFF	OFF
H	H	1	1	0	OFF	OFF	ON	ON
H	H	1	0	1	OFF	ON	ON	OFF
H	H	1	0	0	OFF	ON	ON	ON
H	H	0	1	1	ON	OFF	ON	OFF
H	H	0	1	0	ON	OFF	ON	ON
H	H	0	0	1	ON	ON	ON	OFF
H	H	0	0	0	ON	ON	ON	ON

ON;Power on , OFF;Power off

Note 5) DD and DE are used to select latched data to be updated.

Data		Description
DD	DE	
0	0	Unused.
0	1	Data latched for local oscillator 1 is updated.
1	0	Data latched for local oscillator 2 is updated.
1	1	Data latched for reference frequency .

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Note 6) Dividing ratio of the reference counter for reference frequency is given by 11-bit binary coads .

$$N(\text{fREF1})=5\sim 2047$$

Note 7) Dividing ratio  $N(\text{VCO1})$  of VCO1 for local oscillator1 is given by 5-bit swallow counter and 12-bit programable counter .

$$N(\text{VCO1})=32 \times M+A \quad (A<M)$$

M : Preset dividing ratio of 12-bit programmable counter (32~4095)  
 A : Preset dividing ratio of 5-bit swallow counter (0~31)

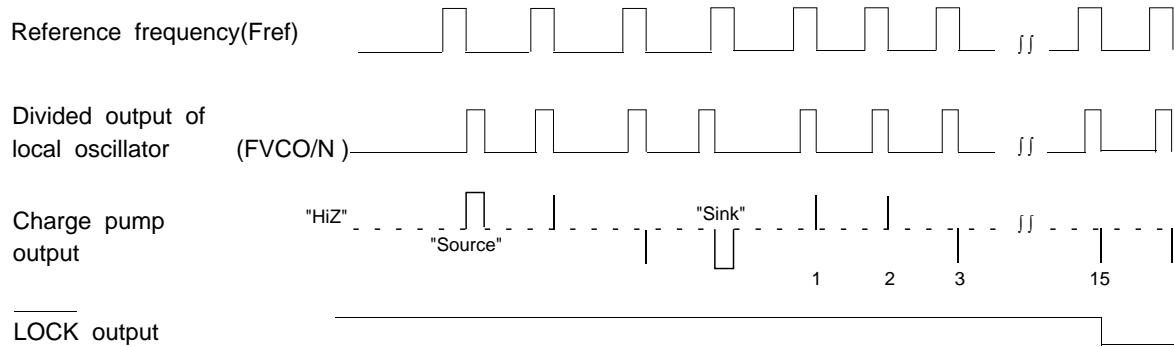
Note 8) Dividing ratio  $N(\text{VCO2})$  of VCO2 for local oscillator2 is given by 4-bit swallow counter and 13-bit programable counter .

$$N(\text{VCO2})=16 \times M+A \quad (A<M)$$

M : Preset dividing ratio of 13-bit programmable counter (16~38191)  
 A : Preset dividing ratio of 4-bit swallow counter (0~315)

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4. Charge Pump and LOCK Detection



Note 9) If the phase of divided local oscillator output (FVCO/N) is behind that of the reference frequency (Fref), the charge pump output becomes "Source" status, if advancing, "Sink" status.

Note 10) If a phase difference smaller than 3 times of the OSC period continues for 15 periods longer, the LOCK output becomes "L".  
 (When, for example,  $F_{osc} = 19.2 \text{ MHz}$ ,  $\Delta t = 156 \text{ ns}$ )

Note 11) If one of the power supplies to PLLs is turned off, a judgment is made based on only the condition of the other loop.

Note 12) The LOCK output circuit yields an open drain N-channel transistor output. It should be pulled up to  $V_{cc}$ .

5. Sleep Mode Input

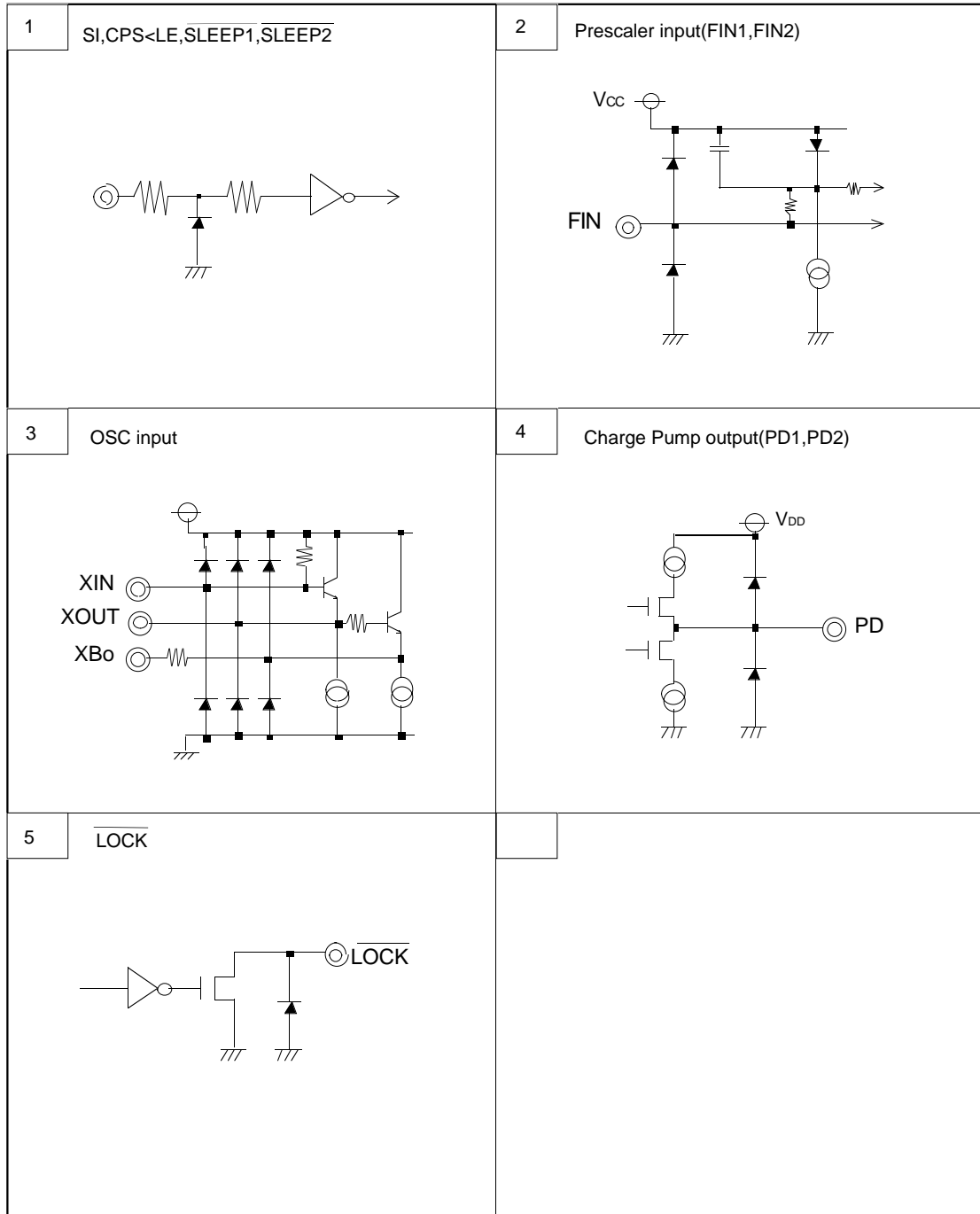
By status of SLEEP1 and SLEEP2, each PLL can be selected to either sleep mode (Power supply is turned off.) or operation mode.

If SLEEP input is "H", the PLL becomes normal operation mode.  
 (Power supplies to turn ON/OFF can be controlled by the serial data; submit to note 4.)

If SLEEP input is "L", the PLL becomes sleep mode. (Power supply is turned off.)

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INPUT / OUTPUT CIRCUIT DIAGRAM





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ABSOLUTE MAXIMUM RATINGS (Ta= -30~85°C, unless otherwise specified .)

Symbol	Parameter	Test Condition	Ratings		Unit
			Min.	Max.	
Vcc	Supply Voltage	GND=0V	-0.3	4.5	V
V	Input Voltage	SI , CPS , LE pin : GND=0V	-0.3	4.5	V
VO	Output Voltage	Output pin : GND=0V	-0.3	4.5	V
Pd	Power Dissipation	Ta=85°C( Allowable dissipation of package )		250	mW
Vopd	Open Drain Voltage	GND=0V	-0.3	4.5	V
Topr	Operating Temperature		-30	85	°C
Tstg	Storage Temperature		-40	125	°C

RECOMMENDED OPERATING CONDITIONS (Ta= -30~85°C, unless otherwise specified .)

Symbol	Parameter	Test Condition	Limits			Unit
			Min.	Typ.	Max.	
Vcc	Supply Voltage		2.7		3.6	V
FIN1	Operating Frequency	Vcc=2.7~3.6V	0.7		1.1	GHz
FIN2			100		500	MHz
VIN1	Input Sensitivity	FIN1=1.0~2.0GHz	-10		2	dBm
VIN2		FIN2=100~500MHz	-16		-4	
VXIN	Oscillator Sensitivity @	Vcc=2.7~3.6V	0.4		1.0	Vp-p

@Recommendation : X'tal (19.2MHz)

ELECTRICAL CHARACTERISTICS (Ta= 25°C, unless otherwise specified .)

Symbol	Parameter	Pin	Test Condition	Limits			Unit
				Min.	Typ.	Max.	
I <sub>PD-SOURCE</sub>	Charge Pump Output (Source) Current	PD1 , PD2	Vcc=3.0V , VPD=Vcc/2		2.0		mA
I <sub>PD-SINK</sub>	Charge Pump Output (Sink) Current				-2.0		
Icc1	Supply Current	Vcc	Vcc=3V , Both PLLs are on .		8.0		mA
Icc2			Vcc=3V , Only PLL1 is on .		5.5		
Icc3			Vcc=3V , Only PLL2 is on .		4.5		
Icc4			Vcc=3V , Both PLLs are off .			10	µA

HANDLING PRECAUTIONS

1. This IC contains fine structure components to achieve high performance . Therefore , take extra precaution to protect the IC from surge voltage caused by static electricity .
2. If one of two PLLs is not used , please make power supply of that turn off .