

**PRELIMINARY**  
 Notice ; This is not a final specification.  
 some parametric limits are subject to change.

# M65850P/FP



## DIGITAL ECHO(DIGITAL DELAY)

### DESCRIPTION

The M65850P/FP is a CMOS IC for generating echo to be added to the voice through a "karaoke" microphone.  
 It is optimal to provide the echo effect function for karaoke player, such as radio cassette recorders, mini audio components and television sets.  
 Increased master clock frequency assures high-performance short delay, enabling the IC to be used for dolby prologic surround system.

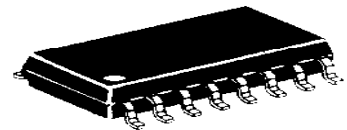
### FEATURES

- Built-in input/output filters, A-D and D-A converters, and memory realize a delay system with only a single chip.
- Built-in current control type clock oscillator circuit avoids clock affection outside, thus allowing prevention of undesired radiation.
- Delay time = 164 ms (with master clock set at 1MHz)  
 (Selection of delay time in a range between 15ms and 200ms)
- Small package (14-pin DIP : 14P4, 16-pin SOP:16P2N)
- Built-in 20Kbit SRAM
- Built-in auto reset circuit (The IC reset as power is turned on)
- Single power supply (5V)

### PACKAGE



Outline 14 P 4 ( P )  
 2.54mm pitch 300mil DIP



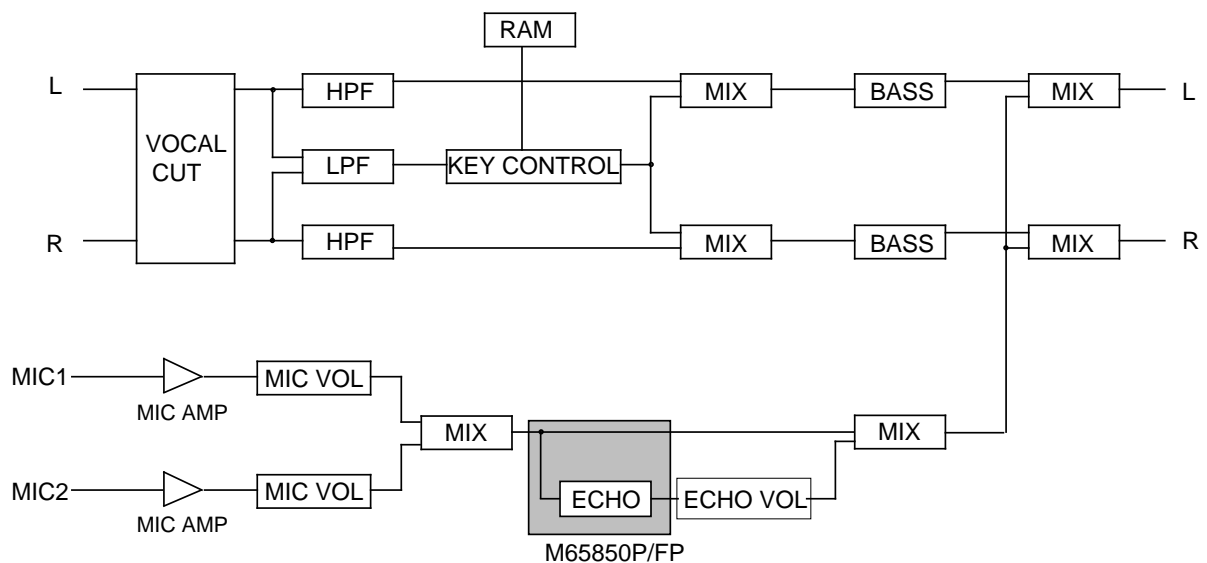
Outline 16 P 2 N ( FP )  
 1.27mm pitch 300mil SOP

### RECOMMENDED OPERATING CONDITION

Supply voltage range ••••• Vcc=3.5~5.5V

Rated supply voltage •••••••••• Vcc=5V

### SYSTEM CONFIGURATION



Note : Dolby is the registered trademarks of dolby laboratories licensing corporation.

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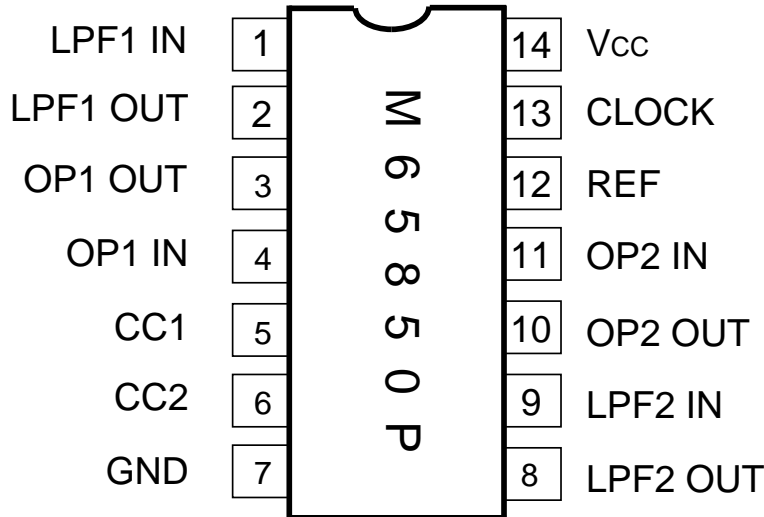
**M65850P/FP**



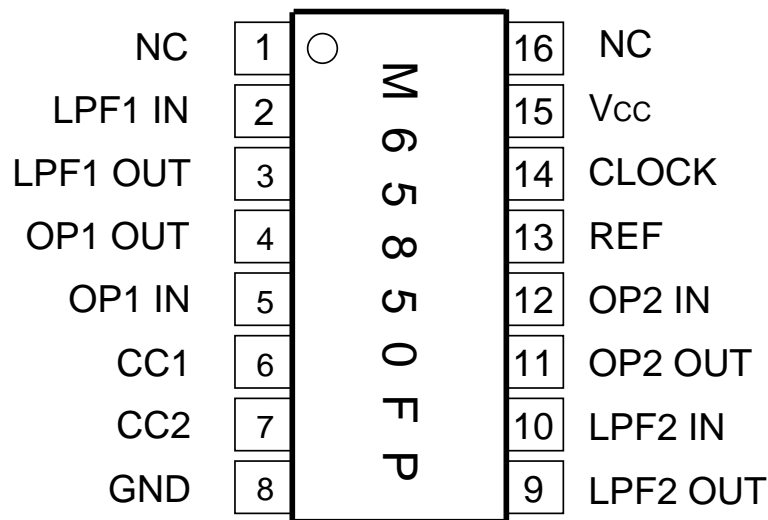
**DIGITAL ECHO(DIGITAL DELAY)**

**PIN CONFIGURATION**

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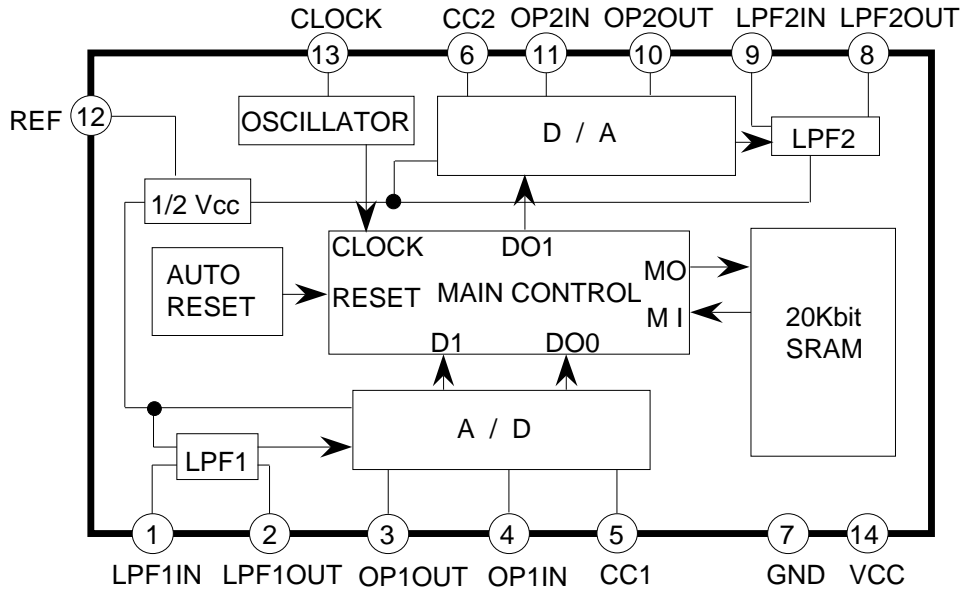
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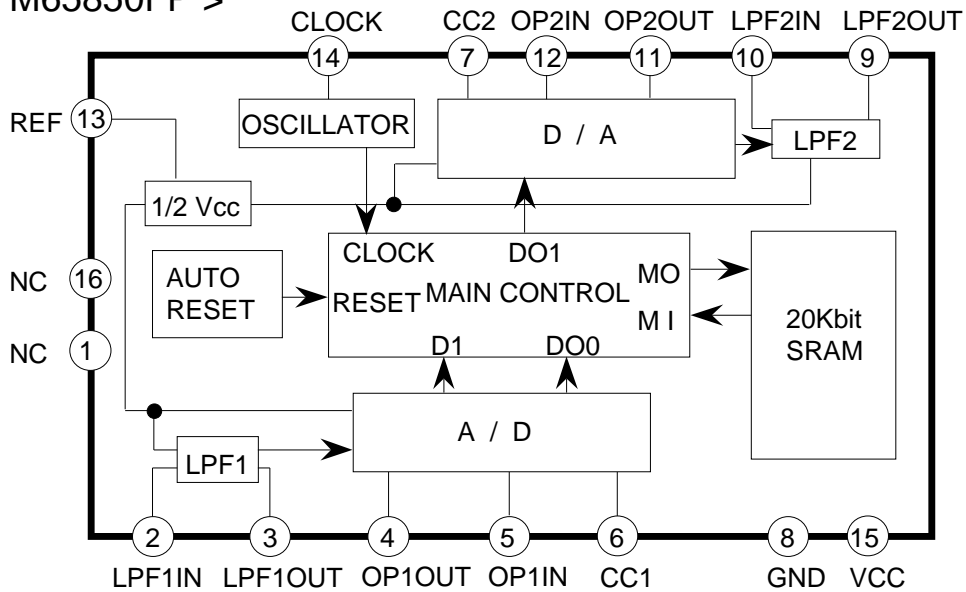
## DIGITAL ECHO(DIGITAL DELAY)

### IC INTERNAL BLOCK DIAGRAM

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**PIN DESCRIPTION**

Pin No.		Symbol	Name	I/O	Function
P	FP				
1	2	LPF1 IN	Low pass filter 1 input	I	To form input-side low pass filter by connecting external capacitor and resistor
2	3	LPF1 OUT	Low pass filter 1 output	O	
3	4	OP1 OUT	Operational amplifier1 output	O	To form A-D conversion integrator by connecting external capacitor
4	5	OP1 IN	Operational amplifier 1 input	I	
5	6	CC1	Current control 1	-	ADM control of A-D converter
6	7	CC2	Current control 2	-	ADM control of D-A converter
7	8	GND	GND	-	
8	9	LPF2 OUT	Low pass filter 2 output	O	To form input-side low pass filter by connecting external capacitor and resistor
9	10	LPF2 IN	Low pass filter 2 input	I	
10	11	OP2 OUT	Operational amplifier 2 output	O	To form D-A conversion integrator by connecting external capacitor
11	12	OP2 IN	Operational amplifier 2 input	I	
12	13	REF	Reference	-	Analog reference voltage $\frac{1}{2}V_{CC}$
13	14	CLOCK	Clock generator input	I	To form clock generator by connecting external resistor
14	15	Vcc	Supply voltage	-	To apply 3.5 ~ 5.5 V power (Rated voltage : 5 V)
-	1/16	NC	No connection	-	

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## DIGITAL ECHO(DIGITAL DELAY)

### ABSOLUTE MAXIMUM RATINGS

( Ta = 25°C, unless otherwise noted )

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		6.0	V
Icc	Circuit current		100	mA
Pd	Power dissipation		800(P),550(FP)	mW
Topr	Operating temperature		-20 ~ 75	°C
Tstg	Storage temperature		-40 ~ 125	°C

### RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Conditions	Limits			Unit
			Min	Typ	Max	
Vcc	Supply Voltage		3.5	5	5.5	V
fck	Clock frequency		0.8	—	11.0	MHz

### ELECTRICAL CHARACTERISTICS

(Vcc=5V, f=1kHz, Vi=100mV(rms), fck=1MHz, Ta=25°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
Icc	Circuit current	No signal input	5	13	25	mA
Gv	Voltage gain	RL=47k	-3.0	0	3.0	dB
Vomax	Maximum output voltage	THD=10%	0.7	1.0	—	V(rms)
THD	Total harmonic distortion	30kHz LPF	—	1.2	3.0	%
No	Output noise voltage	DIN-AUDIO	—	-85	-70	dBV
fck	Clock frequency	Rc=120k	0.85	1	1.15	MHz

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## DIGITAL ECHO(DIGITAL DELAY)

### FUNCTION DESCRIPTION

#### (1) Delay time Td

The delay time can be calculated by the equation :

$$T_d = 8N / f_{ck} \quad (N = \text{the number of memory bits} = 20480)$$

When  $f_{ck} = 1\text{MHz}$  ( $f_s = 125\text{kHz}$ ),  $T_d$  can be set at 164ms.

« Reference »

The M65850P/FP adopts ADM ( Adaptive Delta Modulation ) system in A-D,D-A converters.

The sampling frequency can be calculated by the following equation :

$$f_s = \text{clock frequency} / 8 \text{ ( Hz )}$$

For clock frequency (  $f_{ck}$  ) = 1MHz, the calculated sampling frequency is :

$$f_s = 1\text{MHz} / 8 = 125\text{kHz}$$

#### (2) Clock oscillator circuit

The M65850P incorporates a current control type clock oscillator circuit in it, thus providing circuit configuration just by connecting a resistor for current control to pin (13) ( FP:pin (14) ) CLOCK.

Fully internal clock supply prevents occurrence of undesired radiation without affecting any external circuit.

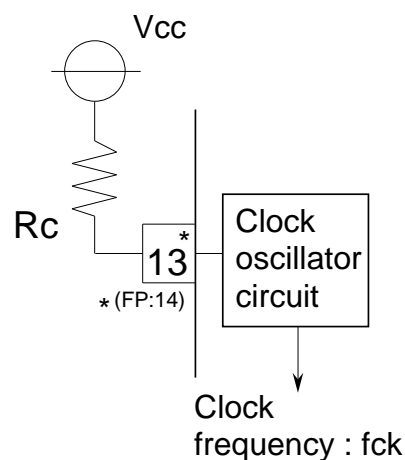
The oscillator frequency is:

$$f_{ck} = 1 \text{ MHz. ( } R_c = 120\text{k } )$$

The resistor for current control can be calculated using the following equation.

$$R_c = \frac{K}{\text{Clock frequency ( } f_{ck} \text{ ) [ Hz ]}}$$

K is the coefficient, and changes according to clock frequency ,as shown below.



Delay Time ( ms )	Clock Frequency ( Hz )	K value	Rc ( )
15~30	11.0M~5.5M	$0.8 \times 10^{11}$	7.5k~15k
31~100	5.3M~1.64M	$1.0 \times 10^{11}$	18k~62k
101~200	1.62M~800K	$1.2 \times 10^{11}$	75k~150k

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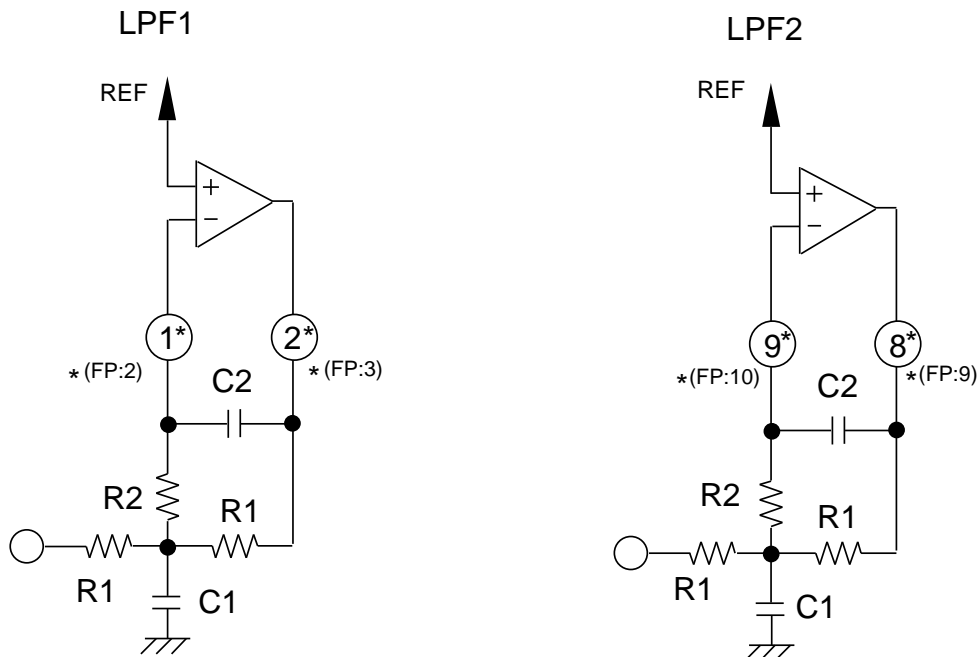
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## DIGITAL ECHO(DIGITAL DELAY)

### (3) Input/output LPF

It is necessary to change the LPF setting ( signal pass band,fsig )  
 of digital echo according to the clock frequency. ( Refer to the table below )



$$f_{sig} = \frac{1}{2 \sqrt{C1 \cdot C2 \cdot R1 \cdot R2}}$$

Delay time ( ms )	Clock frequency( Hz )	signal pass band ( Hz )	LPF				Distortion (Reference value) (%)
			R1( )	R2( )	C1 (F)	C2 (F)	
15~30	11.0M ~ 5.5M	7k	15k	15k	3300p	680p	0.2% (Td=20ms)
31~100	5.3M ~ 1.64M	5k	13k	13k	4700p	1000p	0.3% (Td=50ms)
101~200	1.62M ~ 800k	3k	16k	16k	6800p	1500p	1.2% (Td=160ms)

•Test Condition is Vcc=5V,Vi=100mV(rms),f=1kHz,Ta=25°C

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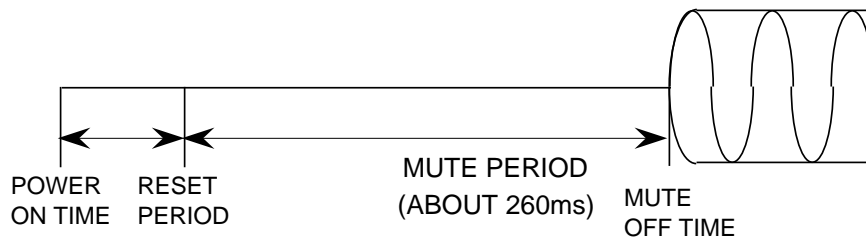
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## DIGITAL ECHO(DIGITAL DELAY)

### (4) Mute

When power is turned on, the mute function works automatically to prevent noise generation. (Here, however, "mute" means the function which prevents noise generation after the reset time.)



WHEN POWER IS ON (f<sub>ck</sub>=1MHz)

### TEST CONDITIONS

Symbol	Parameter	S 1	S 1 4	Remarks
I <sub>cc</sub>	Circuit current	2	2	No-signal time
G <sub>v</sub>	Voltage gain between input and output	1	1	RL=47k
V <sub>omax</sub>	Maximum output voltage	1	1	THD=10%
THD	Output distortion	1	1	30kHz LPF
No	Output noise voltage	2	1	DIN-AUDIO



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MITSUBISHI SOUND PROCESSOR ICs

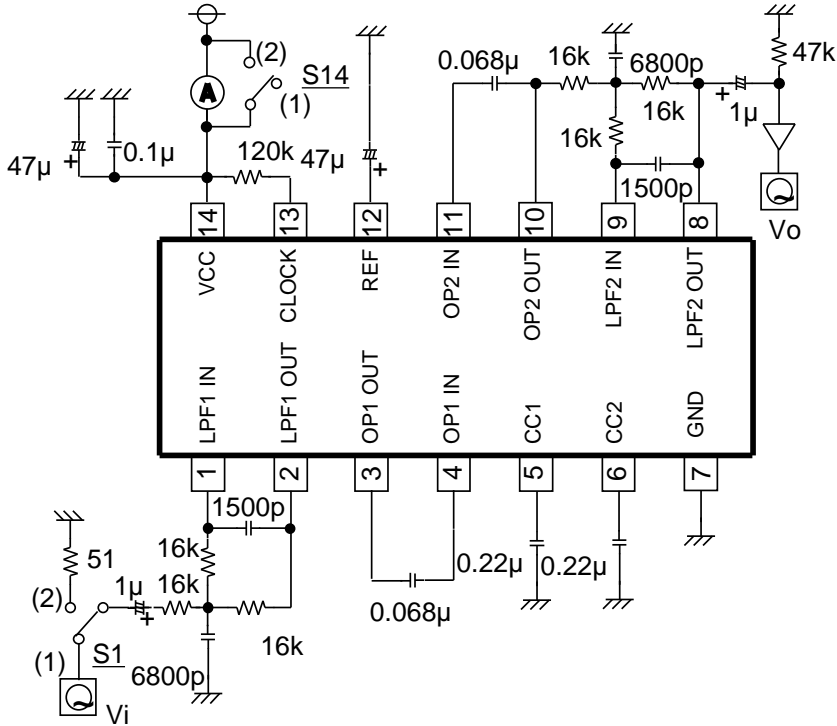
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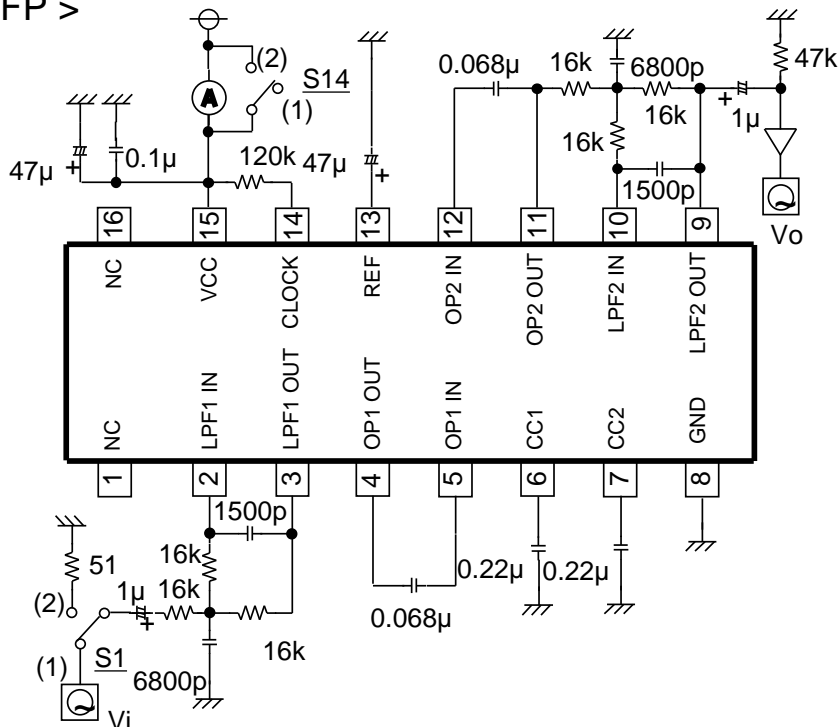
## DIGITAL ECHO(DIGITAL DELAY)

### TEST CIRCUIT

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Units  
 Resistance :  
 Capacitance:F

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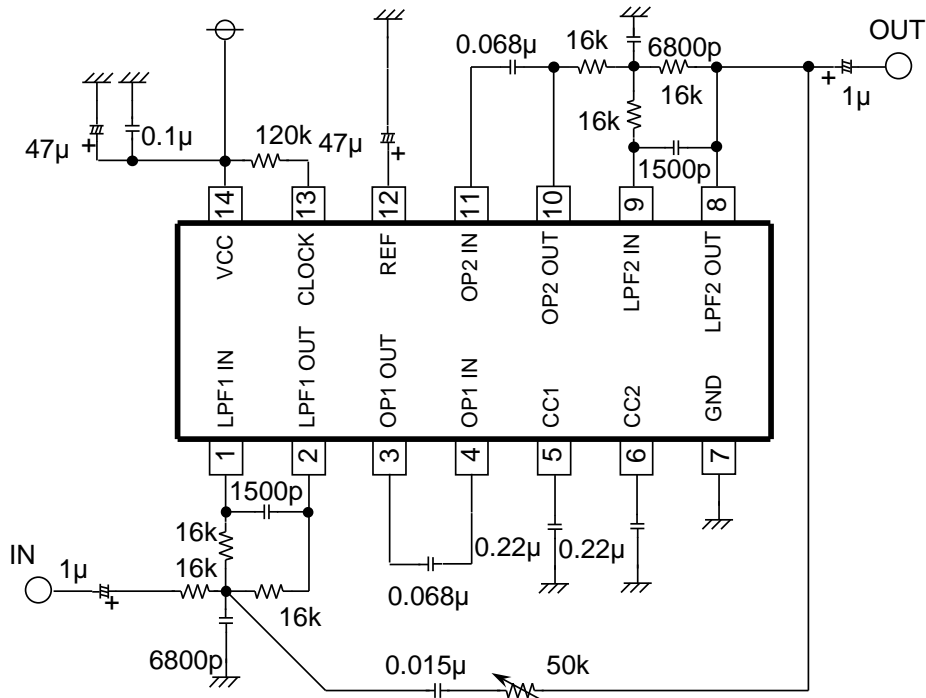
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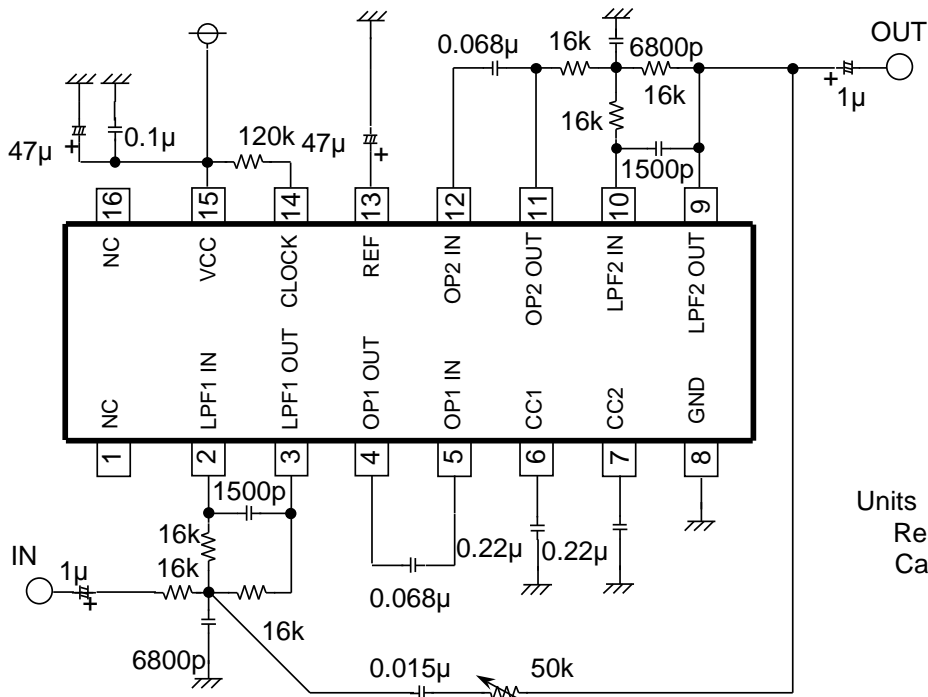
## DIGITAL ECHO(DIGITAL DELAY)

### APPLICATION EXAMPLE

- ECHO Delay time 164ms (Signal pass band 3kHz)  
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FEEDBACK GAIN SETTING VOLUME

Units  
 Resistance :  
 Capacitance : F

FEEDBACK GAIN SETTING VOLUME

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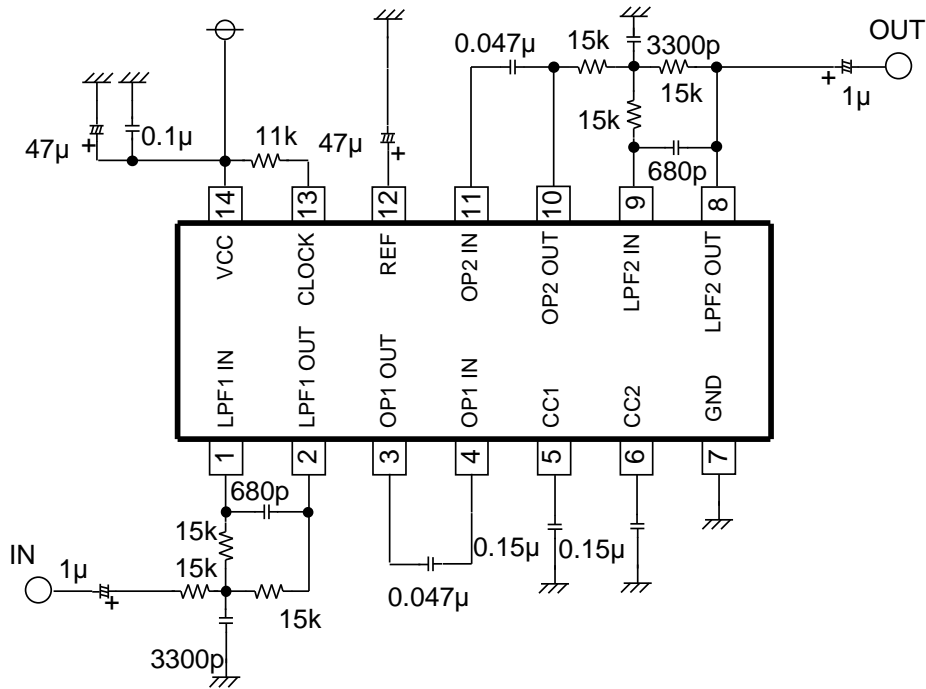
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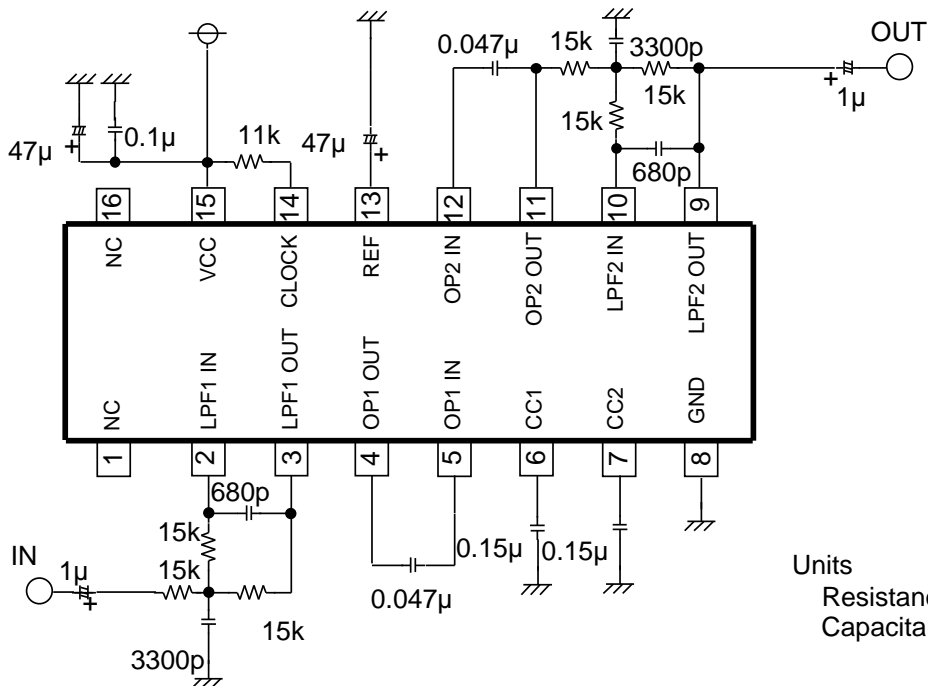
## DIGITAL ECHO(DIGITAL DELAY)

- SURROUND Delay time 20ms ( Signal pass band 7kHz )

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Units  
 Resistance :  
 Capacitance : F