

HC651 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE, INV.) HC652 OCTAL BUS TRANSCEIVER/REGISTER (3-STATE)

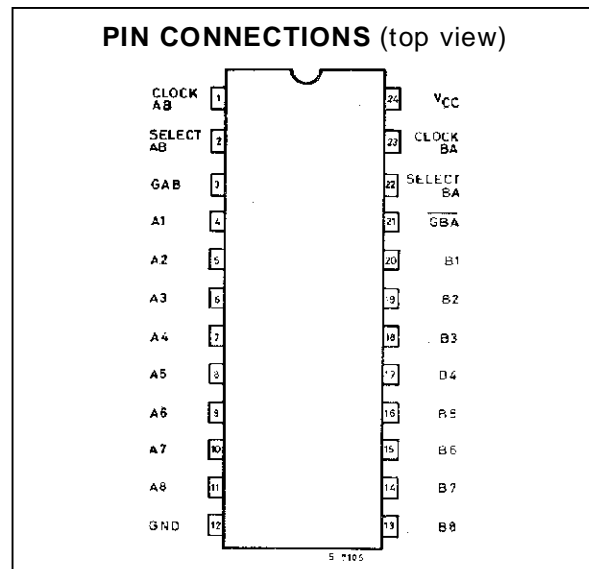
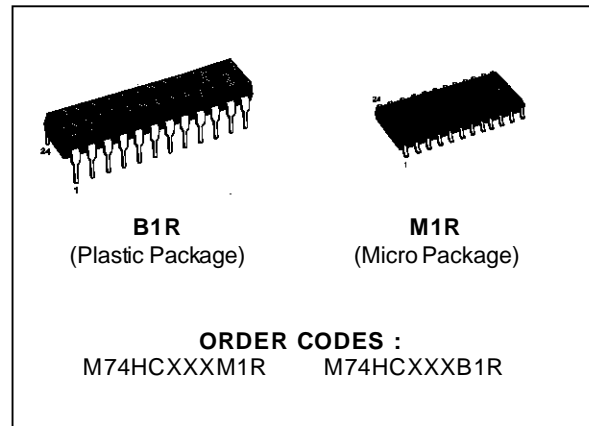
- HIGH SPEED
f_{MAX} = 73 MHz (TYP.) AT V_{CC} = 5V
- LOW POWER DISSIPATION
I_{CC} = 4 μA (MAX.) AT T_A = 25 °C
- HIGH NOISE IMMUNITY
V_{NIH} = V_{NIL} = 28 % V_{CC} (MIN.)
- OUTPUT DRIVE CAPABILITY
15 LSTTL LOADS
- SYMMETRICAL OUTPUT IMPEDANCE
|I_{OH}| = I_{OL} = 6 mA (MIN.)
- BALANCED PROPAGATION DELAYS
t_{PLH} = t_{PHL}
- WIDE OPERATING VOLTAGE RANGE
V_{CC} (OPR) = 2 V TO 6 V
- PIN AND FUNCTION COMPATIBLE
WITH 54/74LS651/652

DESCRIPTION

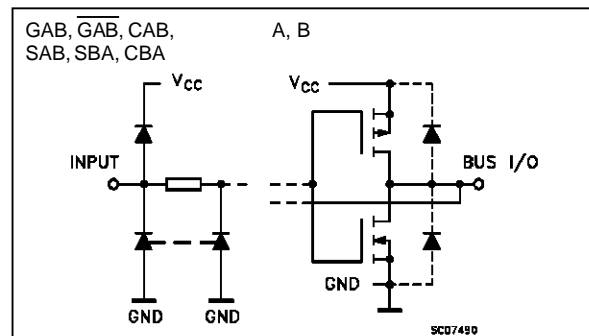
M74HC651/652 are high speed CMOS OCTAL BUS TRANSCEIVERS AND REGISTERS (3-STATE), fabricated in silicon gate C²MOS technology. They have the same high speed performance of LSTTL combined with true CMOS low power consumption. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal storage registers. Enable GAB and GBA are provided to control the transceiver functions.

Select AB and Select BA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data.

Data on the A or B bus, or both, can be stored in the internal D flip-flops by low-to-high transitions on the appropriate clock pins (CLOCK AB or CLOCK BA) regardless of the select or enable control pins. When select AB and select BA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and GBA. In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state. All inputs are equipped with protection circuits against static discharge and transient excess voltage.

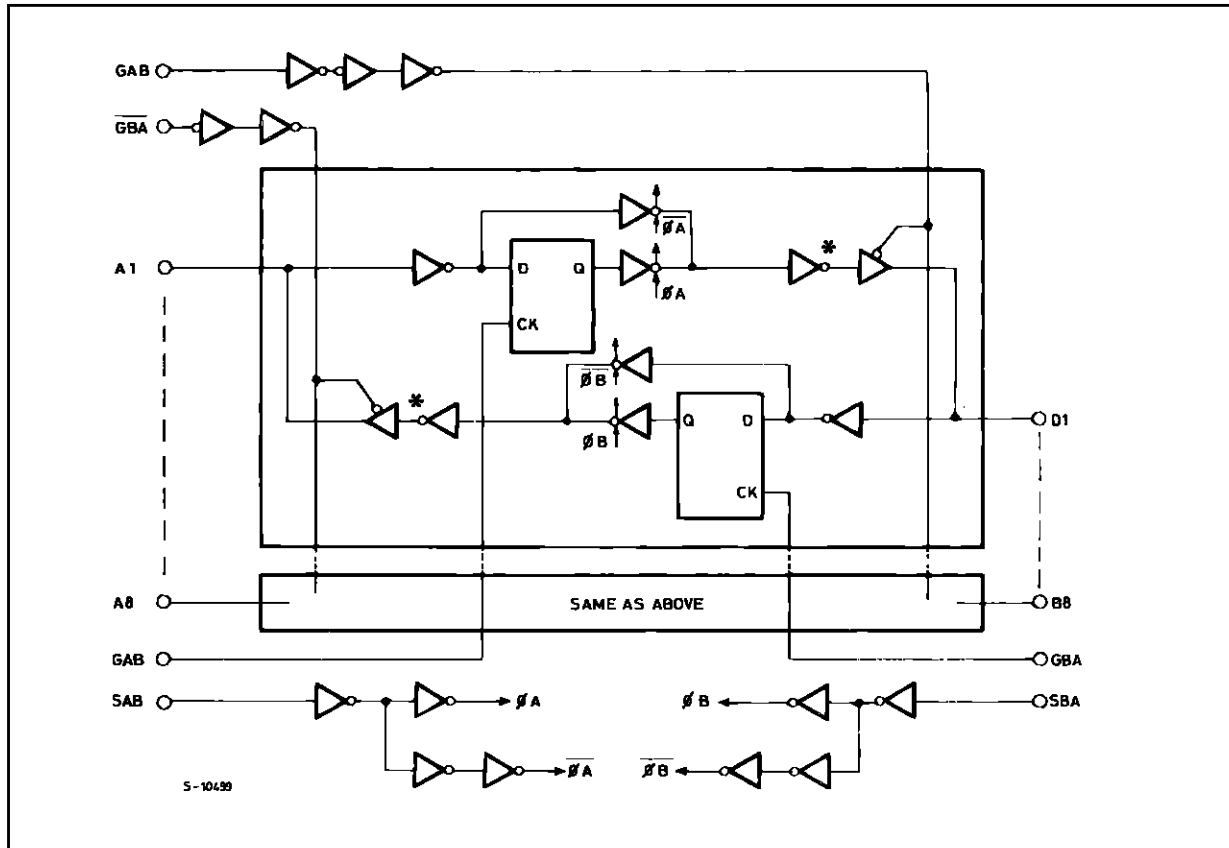


INPUT AND OUTPUT EQUIVALENT CIRCUIT



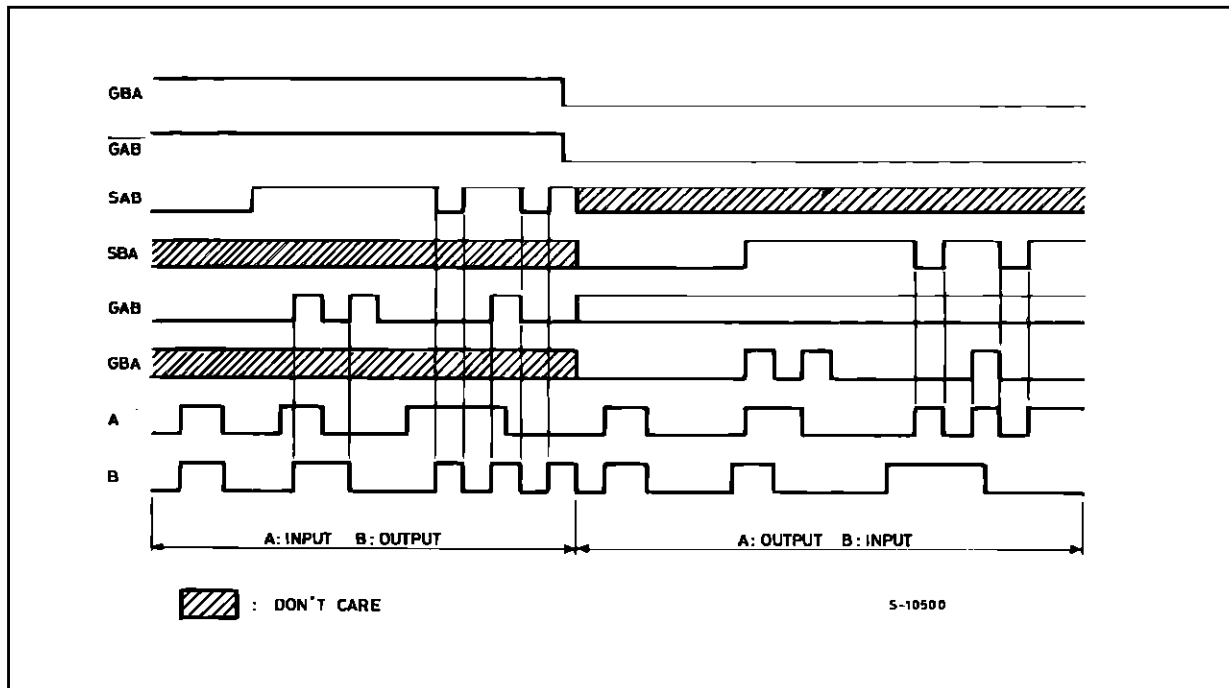
M74HC651/652

LOGIC DIAGRAM (HC652)



Note : In case of M74HC652 output inverter marked * at A bus and B bus are eliminated.

TIMING CHART



TRUTH TABLE

HC652 (The truth table for HC651 is the same as this, but with the outputs inverted)

GAB	GBA	CAB	CBA	SAB	SBA	A	B	FUNCTION
L	H					INPUTS	INPUTS	Both the A bus and the B bus are inputs
		X	X	X	X	Z	Z	The output functions of the A and B bus are disabled
		\square	\square	X	X	INPUTS	INPUTS	Both the A and B bus are used for inputs to the internal flip-flops. Data at the bus will be stored on low to high transition of the clock inputs
L	L					OUTPUTS	INPUTS	The A bus are outputs and the B bus are inputs
		X*	X	X	L	L	L	The data at the B bus are displayed at the A bus
		X*	\square	X	L	L	L	The data at the B bus are displayed at the A bus. The data of the B bus are stored to the internal flip-flop on low to high transition of the clock pulse
		X*	X	X	H	Qn	X	The data stored to the internal flip-flop are displayed at the A bus
		X*	\square	X	H	L	L	The data at the B bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the A bus
H	H					INPUTS	OUTPUTS	The A bus are inputs and the B bus are outputs
		X	X*	L	X	L	L	The data at the A bus are displayed at the B bus
		\square	X*	L	X	L	L	The data at the A bus are displayed at the B bus. The data of the A bus are stored to the internal flip-flop on low to high transition of the clock pulse
		X	X*	H	X	X	Qn	The data stored to the internal flip-flops are displayed at the B bus
		\square	X*	H	X	L	L	The data at the A bus are stored to the internal flip-flop on low to high transition of the clock pulse. The states of the internal flip-flops output directly to the B bus
H	L					OUTPUTS	OUTPUTS	Both the A bus and the B bus are outputs
		X	X	H	H	Qn	Qn	The data stored to the internal flip-flops are displayed at the A and B bus respectively
		\square	\square	H	H	Qn	Qn	The output at the A bus are displayed at the B bus, the output at the B bus are displayed at the A bus respectively

X : DON'T CARE

Z : HIGH IMPEDANCE

Qn : THE DATA STORED TO THE INTERNAL FLIP-FLOPS BY MOST RECENT LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

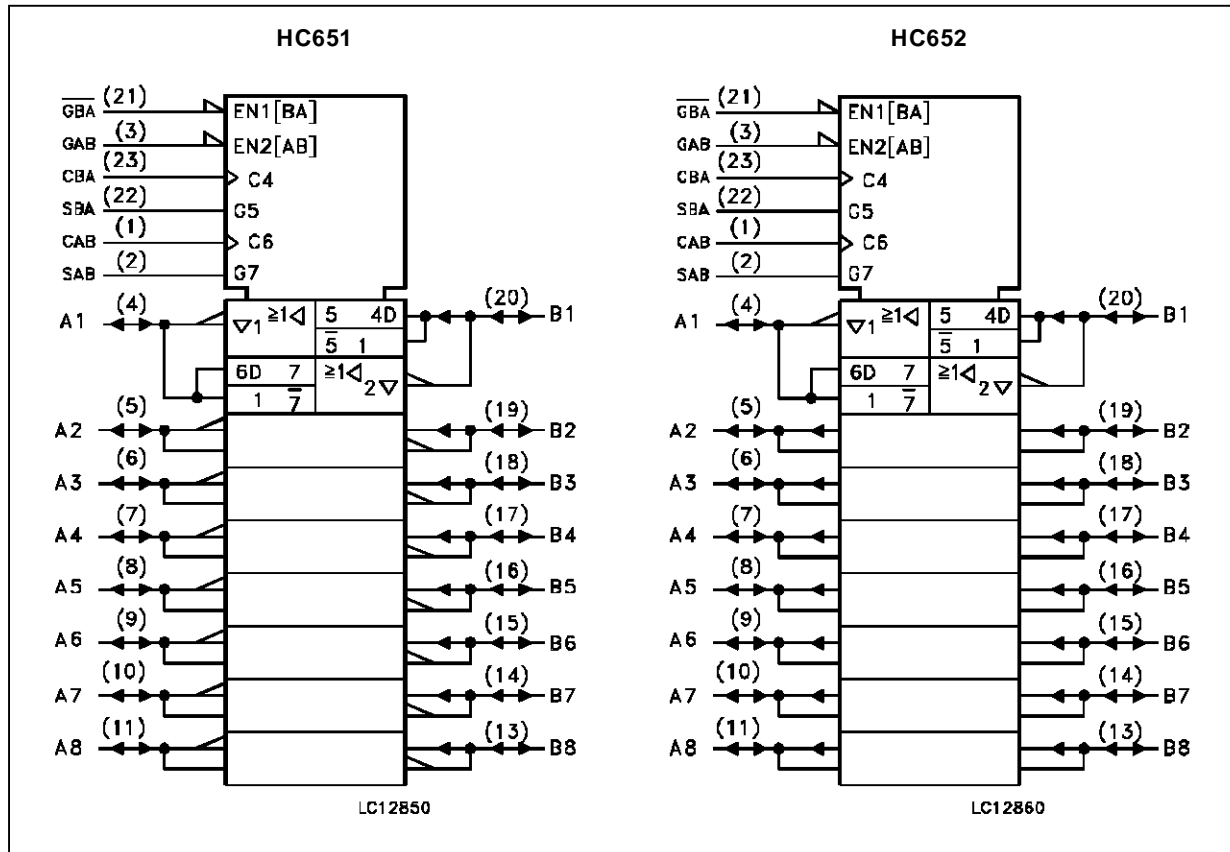
* : THE DATA AT THE A AND B BUS WILL BE STORED TO THE INTERNAL FLIP-FLOPS ON EVERY LOW TO HIGH TRANSITION OF THE CLOCK INPUTS

M74HC651/652

PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	CLOCK AB	A to B Clock Input (LOW to HIGH, Edge-Triggered)
2	SELECT AB	Select A to B Source Input
3	GAB	Direction Control Input
4, 5, 6, 7, 8, 9, 10, 11	A1 to A8	A data Inputs/Outputs
20, 19, 18, 17, 16, 15, 14, 13	B1 to B8	B Data Inputs/Outputs
21	$\overline{\text{GBA}}$	Output Enable Input (Active LOW)
22	SELECT BA	Select B to A Source Input
23	CLOCK BA	B to A Clock Input (LOW to HIGH, Edge-Triggered)
12	GND	Ground (0V)
24	Vcc	Positive Supply Voltage

IEC LOGIC SYMBOLS



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7	V
V _I	DC Input Voltage	-0.5 to V _{CC} + 0.5	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Source Sink Current Per Output Pin	± 35	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 70	mA
P _D	Power Dissipation	500 (*)	mW
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

(*) 500 mW: ≡ 65 °C derate to 300 mW by 10mW/°C: 65 °C to 85 °C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2 to 6	V
V _I	Input Voltage	0 to V _{CC}	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature:	-40 to +85	°C
t _r , t _f	Input Rise and Fall Time	V _{CC} = 2 V	ns
		V _{CC} = 4.5 V	
		V _{CC} = 6 V	

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C			
				Min.	Typ.	Max.	Min.	Max.		
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		V	
		4.5		3.15			3.15			
		6.0		4.2			4.2			
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5	V	
		4.5				1.35		1.35		
		6.0				1.8		1.8		
V _{OH}	High Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = -20 μA	1.9	2.0		1.9		V
		4.5			4.4	4.5		4.4		
		6.0			5.9	6.0		5.9		
		4.5	I _O = -6.0 mA	4.18	4.31		4.13			
		6.0		I _O = -7.8 mA	5.68	5.8		5.63		
V _{OL}	Low Level Output Voltage	2.0	V _I = V _{IH} or V _{IL}	I _O = 20 μA		0.0	0.1		0.1	V
		4.5				0.0	0.1		0.1	
		6.0				0.0	0.1		0.1	
		4.5	I _O = 6.0 mA		0.17	0.26		0.37		
		6.0		I _O = 7.8 mA		0.18	0.26		0.37	
I _I	Input Leakage Current	6.0	V _I = V _{CC} or GND				±0.1		±1	μA
I _{OZ}	3 State Output Off State Current	6.0	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND				±0.5		±5.0	μA
I _{CC}	Quiescent Supply Current	6.0	V _I = V _{CC} or GND				4		40	μA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 6 ns)

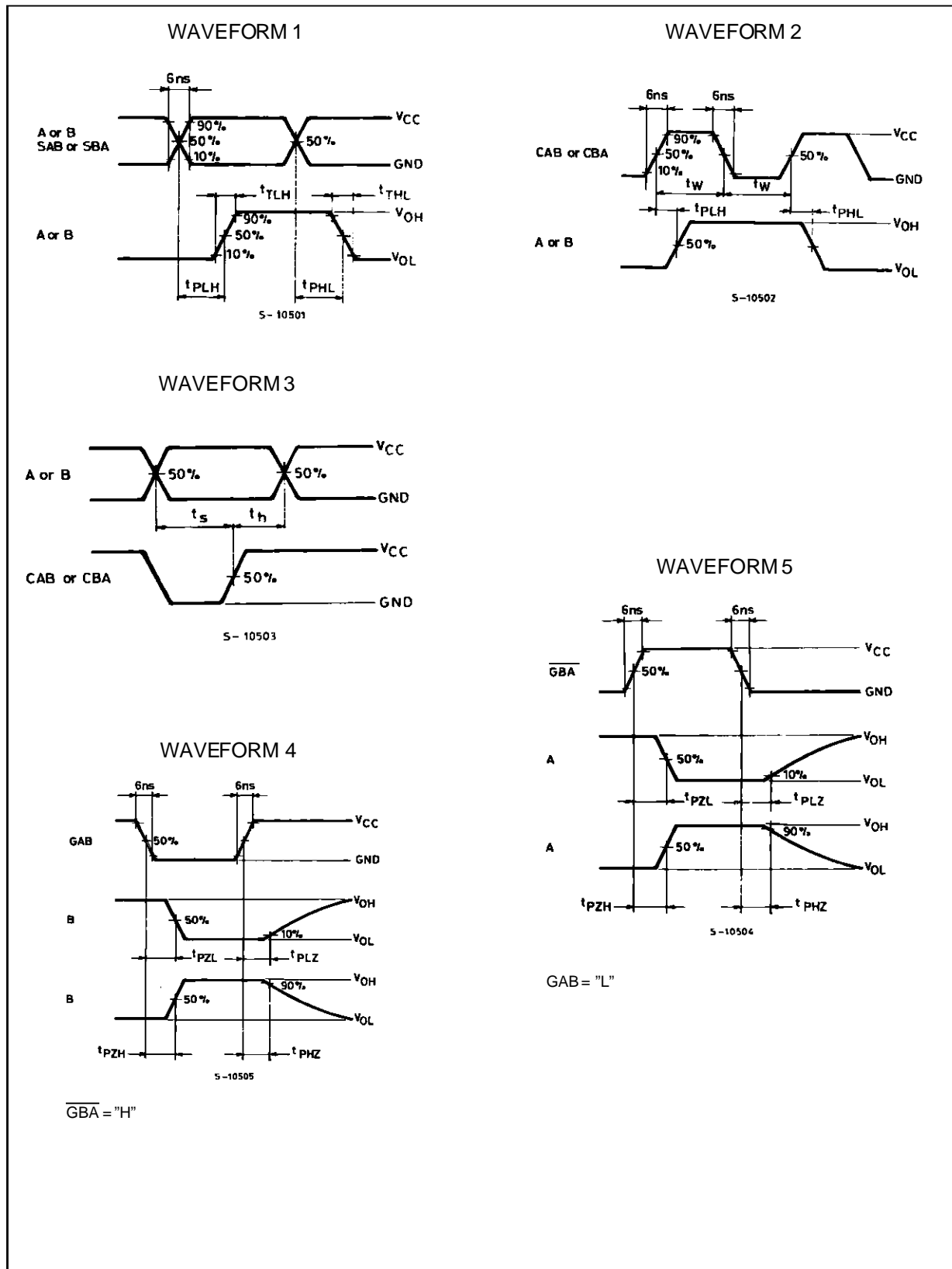
Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)	C _L (pF)	T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
t _{TLH} t _{THL}	Output Transition Time	2.0	50		25	60		75	ns
		4.5		7	12		15		
		6.0		6	10		13		
t _{PLH} t _{PHL}	Propagation Delay Time (BUS - BUS)	2.0	50		74	150		190	ns
		4.5		21	30		38		
		6.0		18	26		32		
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK - BUS)	2.0	150		91	190		240	ns
		4.5		26	38		48		
		6.0		22	32		41		
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK - BUS)	2.0	50		98	210		265	ns
		4.5		28	42		53		
		6.0		24	36		45		
t _{PLH} t _{PHL}	Propagation Delay Time (CLOCK - BUS)	2.0	150		116	250		315	ns
		4.5		33	50		63		
		6.0		28	43		54		

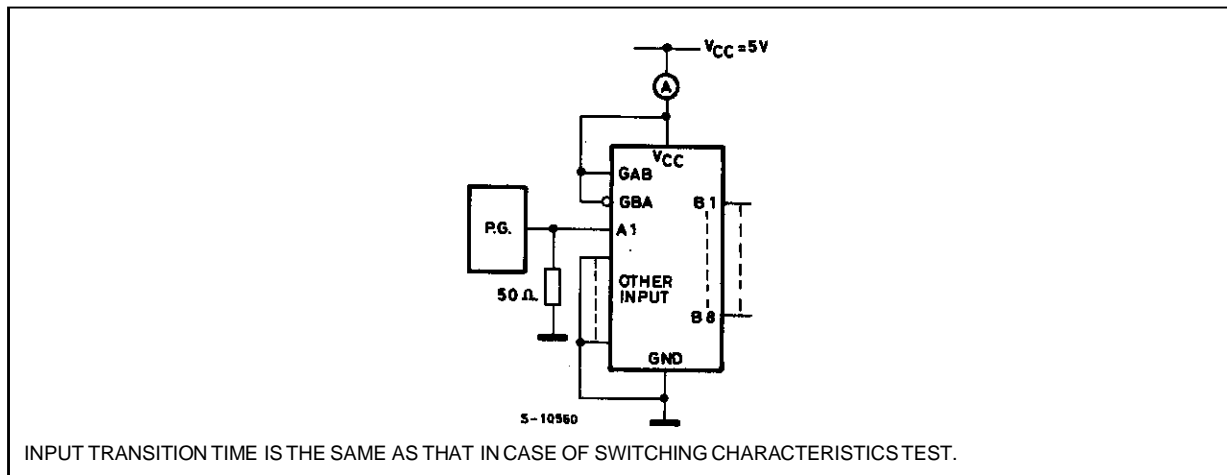
AC ELECTRICAL CHARACTERISTICS (Continued)

Symbol	Parameter	Test Conditions			Value					Unit	
		V _{CC} (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C			
					Min.	Typ.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay Time (SELECT - BUS)	2.0	50			81	170		215	ns	
		4.5				23	34		43		
		6.0				20	29		37		
		2.0	150			98	210		265		ns
		4.5				28	42		53		
		6.0				24	36		45		
t _{PZL} t _{PZH}	3-State Output Enable Time	2.0	50	R _L = 1 KΩ		74	175		220	ns	
		4.5				21	35		44		
		6.0				18	30		37		
		2.0	150		R _L = 1 KΩ		91	215		270	ns
		4.5					26	43		54	
		6.0					22	37		46	
t _{PLZ} t _{PHZ}	Output Disable Time	2.0	50	R _L = 1 KΩ			50	175		220	ns
		4.5					21	35		44	
		6.0					18	30		37	
f _{MAX}	Maximum Clock Frequency	2.0	50		6	19		4.8		MHz	
		4.5			30	67		24			
		6.0			35	79		28			
t _{W(H)} t _{W(L)}	Minimum Clock Pulse Width	2.0	50			30	75		95	ns	
		4.5				7	15		19		
		6.0				6	13		16		
t _s	Minimum Set-up Time	2.0	50			16	50		65	ns	
		4.5				4	10		13		
		6.0				3	9		11		
t _h	Minimum Hold Time	2.0	50				5		5	ns	
		4.5					5		5		
		6.0					5		5		
C _{IN}	Input Capacitance					5	10		10	pF	
C _{I/O}	Bus Terminal Capacitance					10				pF	
C _{PD} (*)	Power Dissipation Capacitance			for HC651 for HC652		39 38					pF

(*) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} • V_{CC} • f_{IN} + I_{CC}/8 (per Channel)

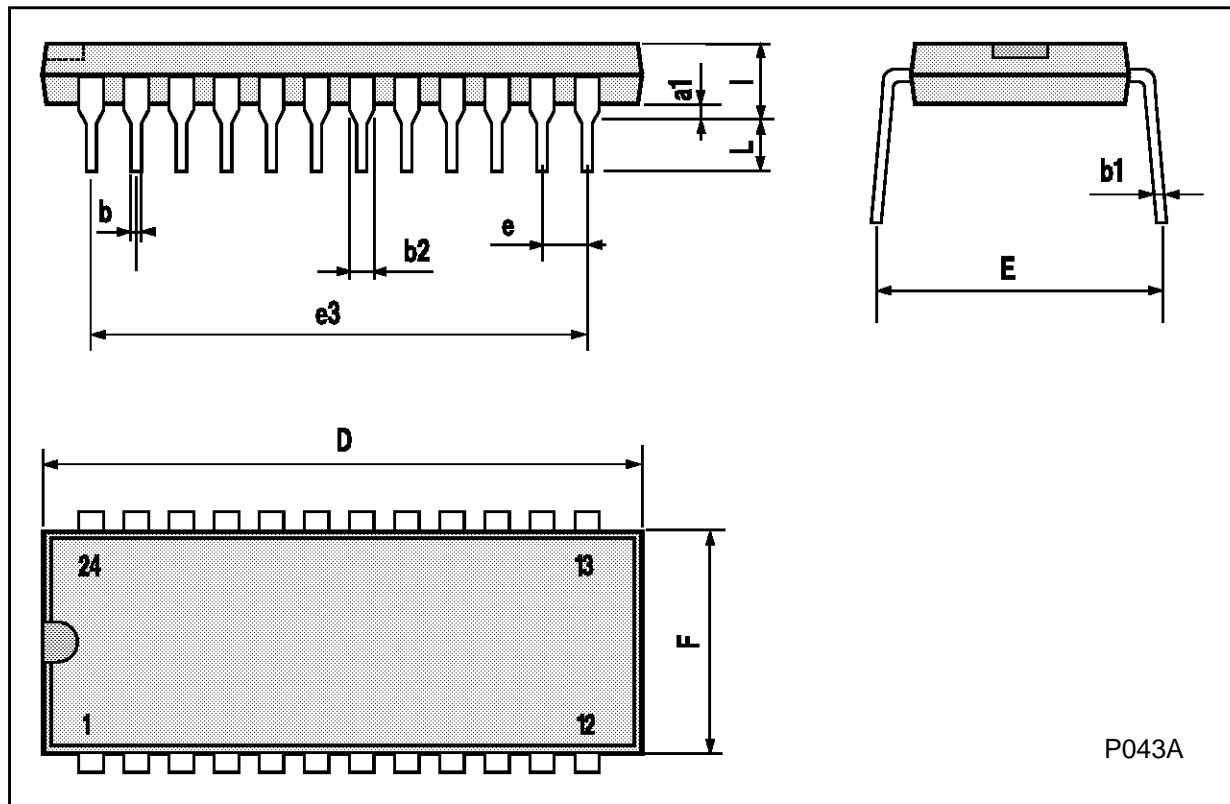
SWITCHING CHARACTERISTICS TEST CIRCUIT AND WAVEFORM



TEST WAVEFORM I_{cc} (Opr.)

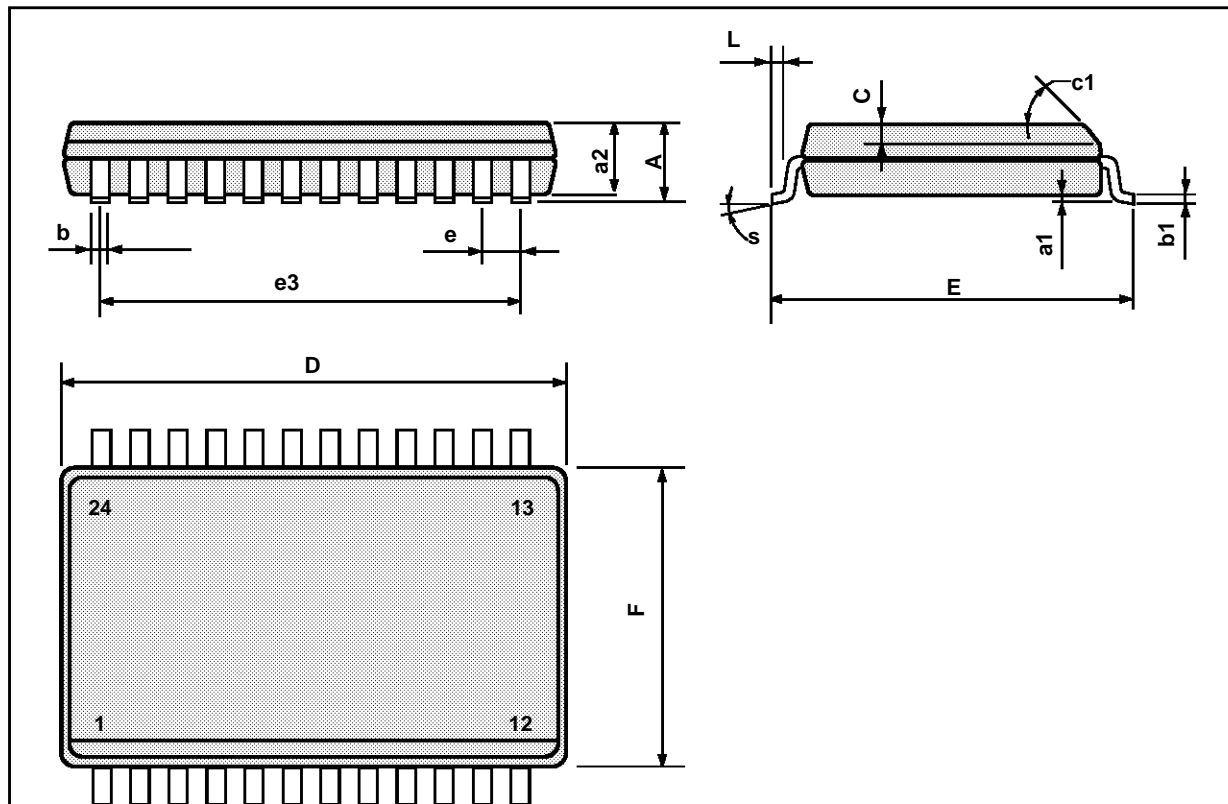
Plastic DIP24 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1		0.63			0.025	
b		0.45			0.018	
b1	0.23		0.31	0.009		0.012
b2		1.27			0.050	
D			32.2			1.268
E	15.2		16.68	0.598		0.657
e		2.54			0.100	
e3		27.94			1.100	
F			14.1			0.555
l		4.445			0.175	
L		3.3			0.130	



SO24 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			2.65			0.104
a1	0.10		0.20	0.004		0.007
a2			2.45			0.096
b	0.35		0.49	0.013		0.019
b1	0.23		0.32	0.009		0.012
C		0.50			0.020	
c1	45° (typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.420
e		1.27			0.05	
e3		13.97			0.55	
F	7.40		7.60	0.291		0.299
L	0.50		1.27	0.19		0.050
S	8° (max.)					



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