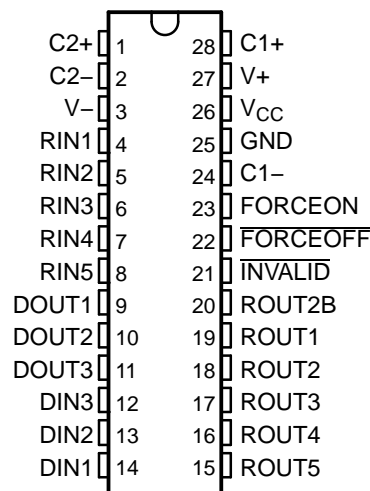


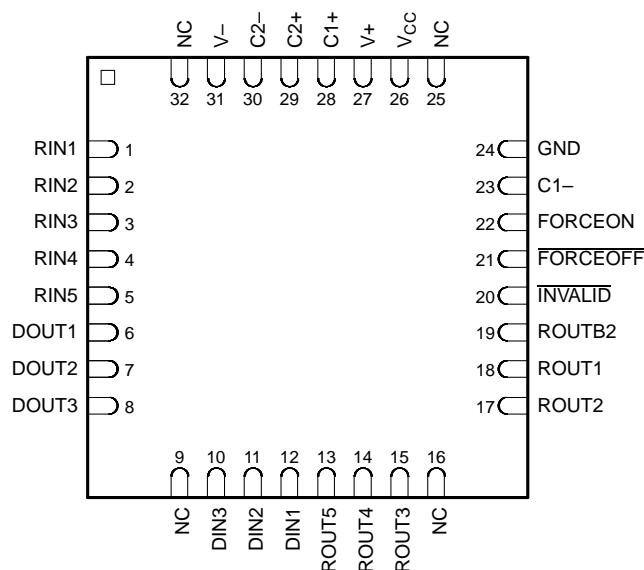
FEATURES

- **Single-Chip and Single-Supply Interface for IBM™ PC/AT™ Serial Port**
- **ESD Protection for RS-232 Bus Pins**
 - ± 15 -kV Human-Body Model (HBM)
 - ± 8 -kV IEC61000-4-2, Contact Discharge
 - ± 15 -kV IEC61000-4-2, Air-Gap Discharge
- **Meets or Exceeds Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V V_{CC} Supply**
- **Always-Active Noninverting Receiver Output (ROUT2B)**
- **Designed to Transmit at a Data Rate up to 500 kbit/s**
- **Low Standby Current . . . 1 μ A Typ**
- **External Capacitors . . . $4 \times 0.1 \mu$ F**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Designed to Be Interchangeable With Maxim MAX3243E**
- **Serial-Mouse Driveability**
- **Auto-Powerdown Feature to Disable Driver Outputs When No Valid RS-232 Signal Is Sensed**
- **Applications**
 - **Battery-Powered Systems, PDAs, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment**
- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages**

**DB, DW, OR PW PACKAGE
(TOP VIEW)**



**QFN PACKAGE
(TOP VIEW)**



DESCRIPTION

The MAX3243E device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ± 15 -kV ESD (HBM and IEC61000-4-2, Air-Gap Discharge) and ± 8 -kV ESD (IEC61000-4-2, Contact Discharge) protection on serial-port connection pins. The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for the typical serial port used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 250 kbit/s and a maximum of 30-V/ μ s driver output slew rate.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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MAX3243E
3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER
WITH ±15-kV IEC ESD PROTECTION

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DESCRIPTION (CONTINUED)

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and FORCEOFF are high, and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30 μs. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μs. Refer to Figure 5 for receiver input levels.

The MAX3243EC is characterized for operation from 0°C to 70°C. The MAX3243EI is characterized for operation from -40°C to 85°C.

AVAILABLE OPTIONS

T _A	PACKAGED DEVICES ⁽¹⁾			
	SHRINK SMALL OUTLINE (DB)	SMALL OUTLINE (DB)	THIN SHRINK SMALL OUTLINE (PW)	QUAD FLAT NO-LEAD (RHB)
0°C to 70°C	MAX3243ECDB	MAX3243ECDW	MAX3243ECPW	MAX3243ECRHBR (Preview)
-40°C to 85°C	MAX3243EIDB	MAX3243EIDW	MAX3243EIPW	MAX3243EIRHBR (Preview)

(1) The DB, DW, and PW packages are available in both tube and taped & reeled. Add the suffix R to orderable (e.g. MAX3243ECDBR for taped & reeled version).

FUNCTION TABLES

EACH DRIVER⁽¹⁾

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER⁽¹⁾

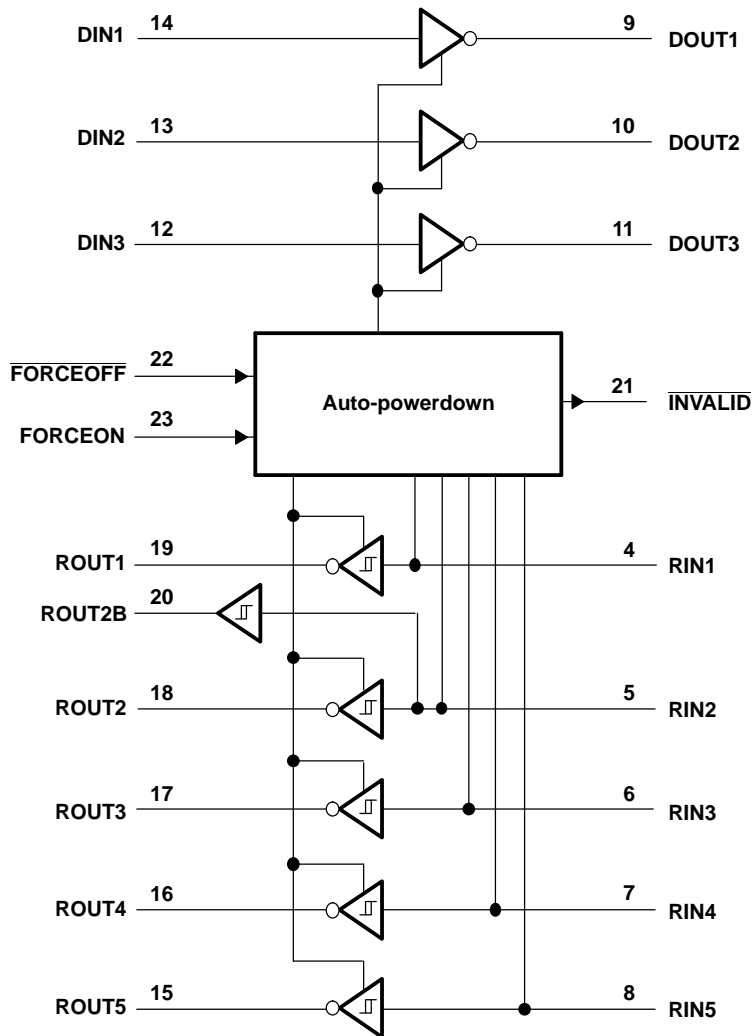
INPUTS				OUTPUTS		RECEIVER STATUS
RIN2	RIN1, RIN3-RIN5	FORCEOFF	VALID RIN RS-232 LEVEL	ROUT2B	ROUT	
L	X	L	X	L	Z	Powered off while ROUT2B is active
H	X	L	X	H	Z	
L	L	H	Yes	L	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	Yes	L	L	
H	L	H	Yes	H	H	
H	H	H	Yes	H	L	
Open	Open	H	Yes	L	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

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LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	-0.3	6	V
V+	Positive output supply voltage range ⁽²⁾	-0.3	7	V
V-	Negative output supply voltage range ⁽²⁾	0.3	-7	V
V+ - V-	Output supply voltage difference ⁽²⁾		13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON)		V
V _O	Output voltage range	Driver		V
θ_{JA}	Package thermal impedance ⁽³⁾⁽⁴⁾	DB package		°C/W
		DW package		
		PW package		
Lead temperature 1,6 mm (1/16 in) from case for 10 s			260	°C
T _{stg}	Storage temperature range	-65	150	°C

- Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltages are with respect to network GND.
- Maximum power dissipation is a function of T_{J(max)}, θ_{JA} , and T_A. The maximum allowable power dissipation at any allowable ambient temperature is P_D = (T_{J(max)} - T_A)/ θ_{JA} . Operating at the absolute maximum T_J of 150°C can affect reliability.
- The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

See Figure 6

		MIN	NOM	MAX	UNIT	
Supply voltage		V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON			V	
		V _{CC} = 3.3 V	2			
		V _{CC} = 5 V	2.4			
V _{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON		0.8	V	
V _I	Driver and control input voltage	DIN, FORCEOFF, FORCEON		0	5.5	V
V _I	Receiver input voltage			-25	25	V
T _A	Operating free-air temperature	MAX3243EC		0	70	°C
		MAX3243EI		-40	85	

- Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _I	Input leakage current	FORCEOFF, FORCEON		± 0.01	± 1	μ A
I _{CC}	Supply current (T _A = 25°C)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V _{CC}	0.3	1	mA
		Powered off	No load, FORCEOFF at GND	1	10	
		Auto-powerdown enabled	No load, FORCEOFF at V _{CC} , FORCEON at GND, All RIN are open or grounded, All DIN are grounded	1	10	μ A

- Test conditions are C1–C4 = 0.1 μ F at V_{CC} = 3.3 V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at V_{CC} = 5 V \pm 0.5 V.
- All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

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DRIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL} Low-level output voltage	All DOUT at R _L = 3 kΩ to GND	-5	-5.4		V
V _O Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5			V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL} Low-level input current	V _I at GND		±0.01	±1	μA
V _{hys} Input hysteresis				±1	V
I _{OS} Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V			±60	mA
	V _{CC} = 5.5 V, V _O = 0 V				
r _o Output resistance	V _{CC} , V+, and V- = 0 V, V _O = ±2 V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND, V _O = ±12 V, V _{CC} = 0 to 5.5 V			±25	μA

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

Switching Characteristics⁽¹⁾

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT	
Maximum data rate	C _L = 1000 pF, R _L = 3 kΩ One DOUT switching, See Figure 1	250	500		kbit/s	
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 150 pF to 2500 pF, R _L = 3 kΩ to 7 kΩ, See Figure 2		100		ns	
SR(tr) Slew rate, transition region (see Figure 1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ, PRR = 250 kbit/s		C _L = 150 pF to 1000 pF	6	30	V/μs
			C _L = 150 pF to 2500 pF	4	30	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver outputs (pins 9–11)	HBM	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	kV
	IEC61000-4-2, Contact Discharge	±8	kV

RECEIVER SECTION

Electrical Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V_{OH}	High-level output voltage	$I_{OH} = -1$ mA	$V_{CC} - 0.6$	$V_{CC} - 0.1$		V
V_{OL}	Low-level output voltage	$I_{OH} = 1.6$ mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	$V_{CC} = 3.3$ V		1.6	2.4	V
		$V_{CC} = 5$ V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	$V_{CC} = 3.3$ V	0.6	1.1		V
		$V_{CC} = 5$ V	0.8	1.4		
V_{hys}	Input hysteresis ($V_{IT+} - V_{IT-}$)			0.5		V
I_{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		± 0.05	± 10	μ A
r_i	Input resistance	$V_I = \pm 3$ V or ± 25 V	3	5	7	k Ω

(1) Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

(2) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ$ C.

Switching Characteristics⁽¹⁾

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	$C_L = 150$ pF, See Figure 3	150	ns
t_{PHL}	Propagation delay time, high- to low-level output		150	ns
t_{en}	Output enable time	$C_L = 150$ pF, $R_L = 3$ k Ω , See Figure 4	200	ns
t_{dis}	Output disable time		200	ns
$t_{sk(p)}$	Pulse skew ⁽³⁾	See Figure 3	50	ns

(1) Test conditions are C1–C4 = 0.1 μ F at $V_{CC} = 3.3$ V \pm 0.3 V; C1 = 0.047 μ F, C2–C4 = 0.33 μ F at $V_{CC} = 5$ V \pm 0.5 V.

(2) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ$ C.

(3) Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.

ESD Protection

PARAMETER	TEST CONDITIONS	TYP	UNIT
Driver outputs (pins 4–8)	HBM	± 15	kV
	IEC61000-4-2, Air-Gap discharge	± 15	kV
	IEC61000-4-2, Contact Discharge	± 8	kV

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AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}		2.7	V
$V_{IT-(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND, FORCEOFF = V_{CC}	-0.3	0.3	V
V_{OH}	$\overline{INVALID}$ high-level output voltage	$I_{OH} = -1$ mA, FORCEON = GND, FORCEOFF = V_{CC}	$V_{CC} - 0.6$		V
V_{OL}	$\overline{INVALID}$ low-level output voltage	$I_{OL} = 1.6$ mA, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

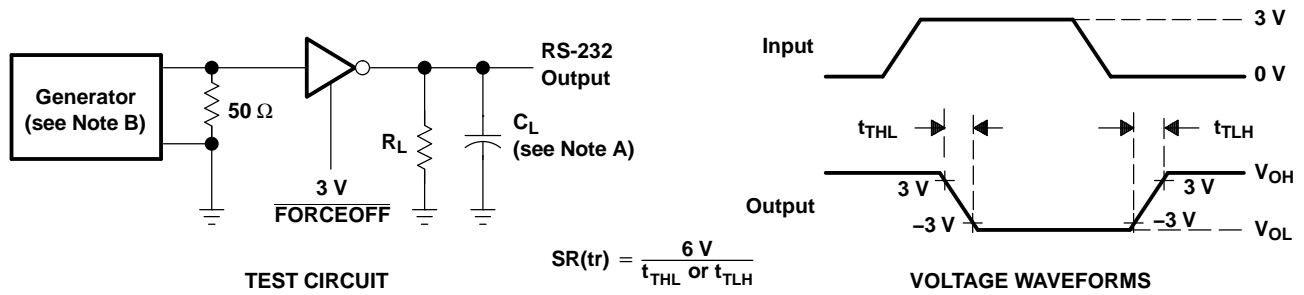
Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t_{valid}	Propagation delay time, low- to high-level output	$V_{CC} = 5$ V	1	μ s
$t_{invalid}$	Propagation delay time, high- to low-level output	$V_{CC} = 5$ V	30	μ s
t_{en}	Supply enable time	$V_{CC} = 5$ V	100	μ s

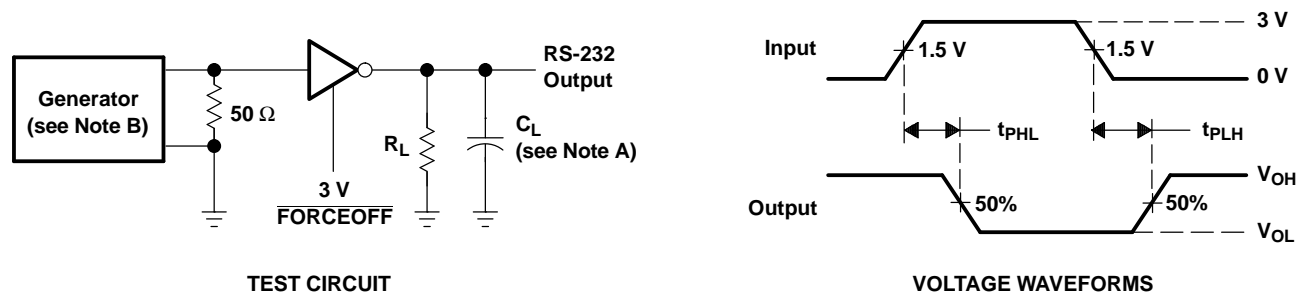
(1) All typical values are at $V_{CC} = 3.3$ V or $V_{CC} = 5$ V, and $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



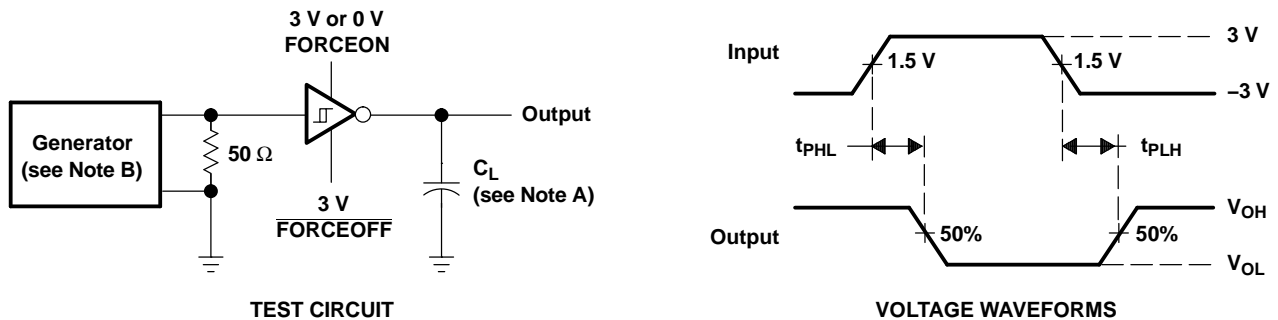
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 1. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

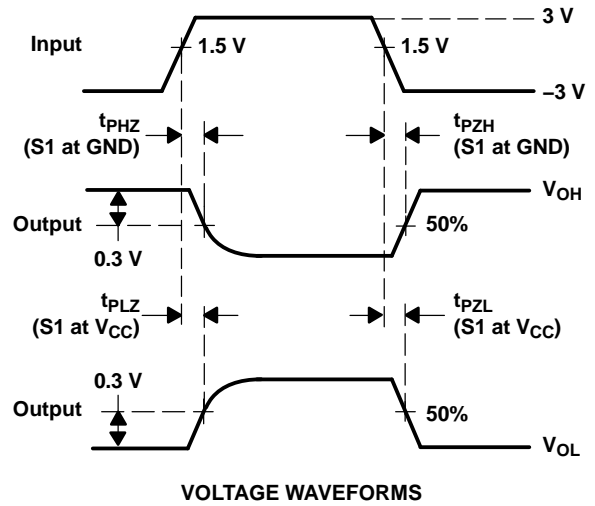
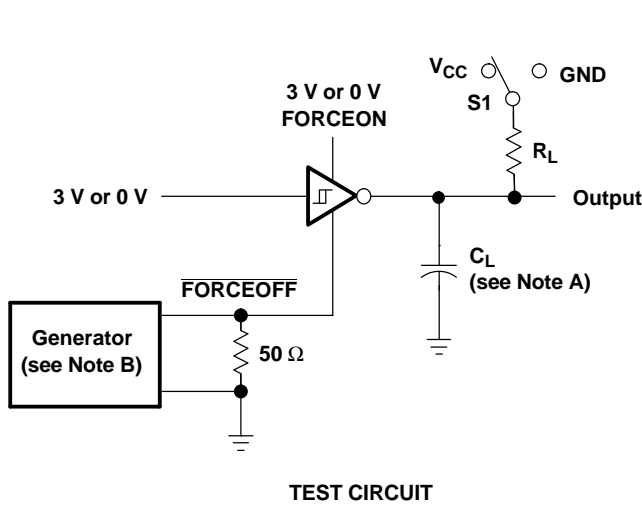
Figure 2. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 3. Receiver Propagation Delay Times

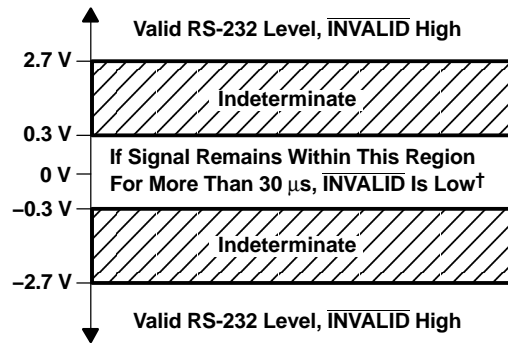
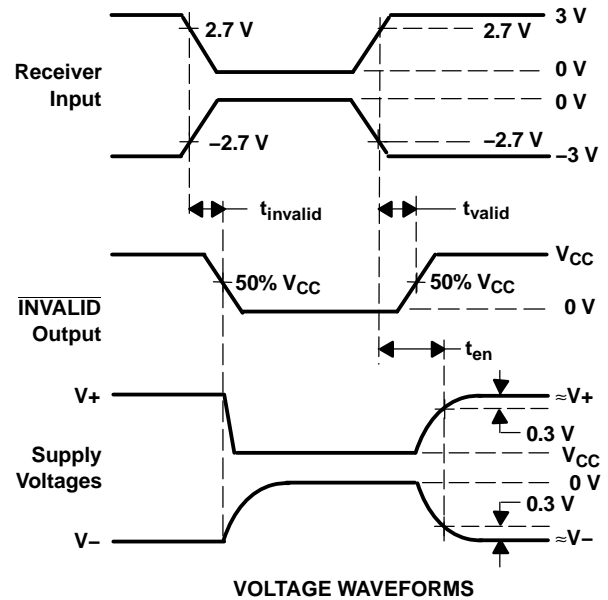
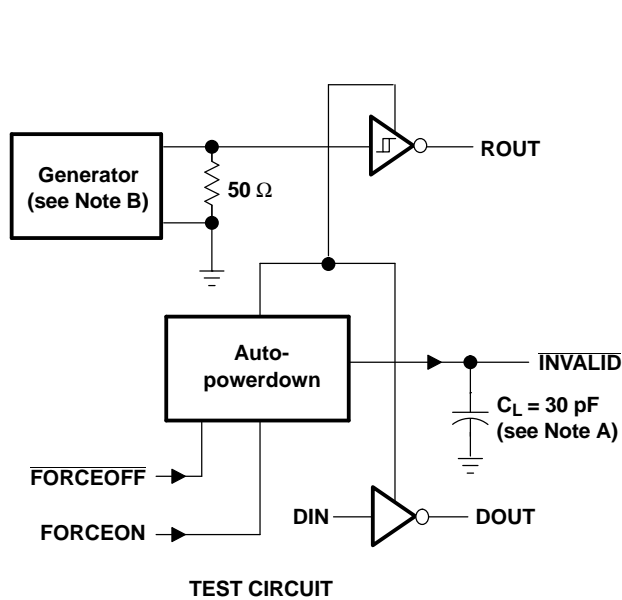
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 4. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION

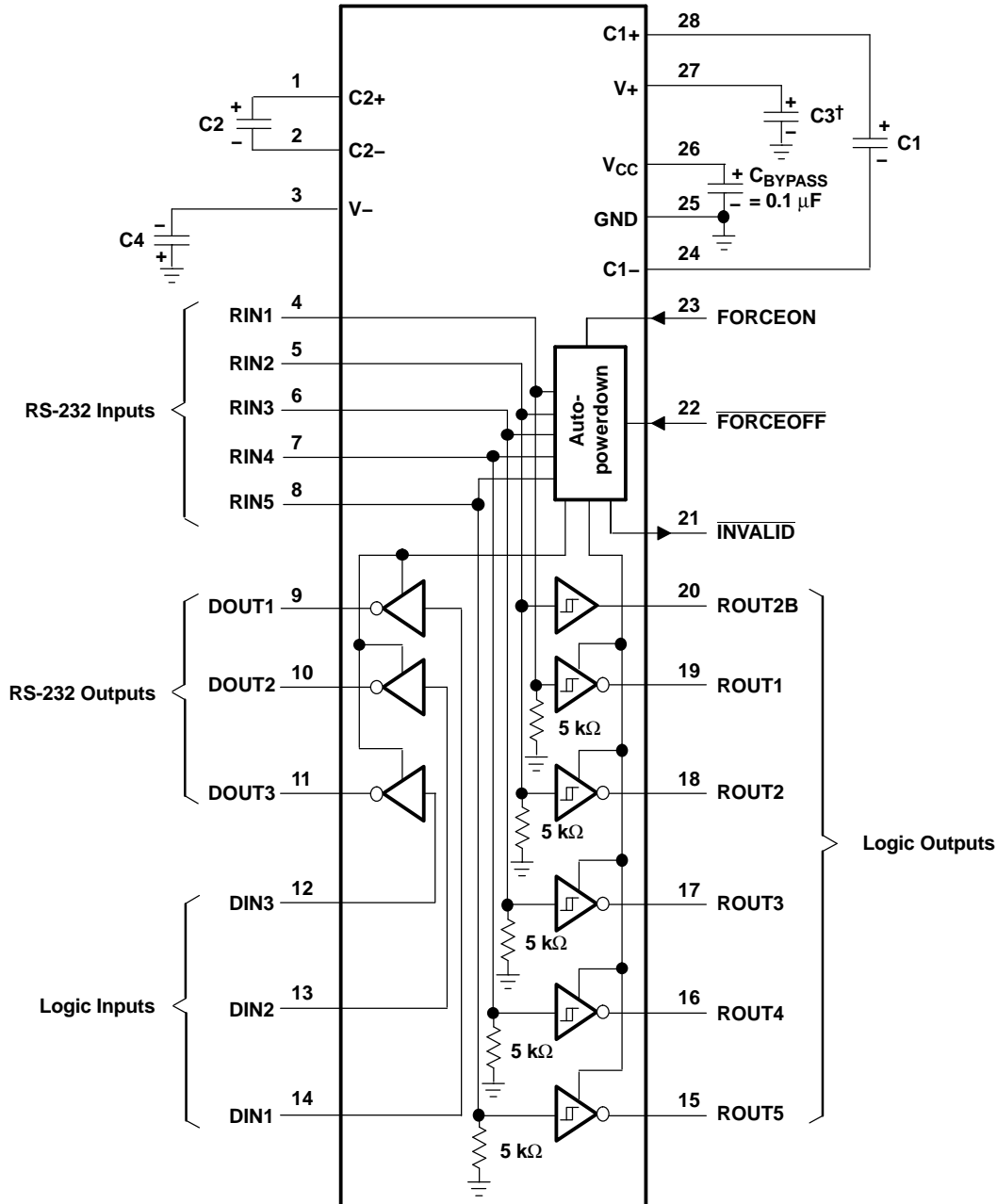


[†] Auto-powerdown disables drivers and reduces supply current to 1 μ A.

- NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 5. $\overline{INVALID}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V _{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

Figure 6. Typical Operating Circuit and Capacitor Values

APPLICATION INFORMATION

ESD Protection

TI MAX3243E devices have standard ESD protection structures incorporated on the pins to protect against electrostatic discharges encountered during assembly and handling. In addition, the RS232 bus pins (driver outputs and receiver inputs) of these devices have an extra level of ESD protection. Advanced ESD structures were designed to successfully protect these bus pins against ESD discharge of ± 15 -kV in all states: normal operation, shutdown, and powered down. The MAX3243E devices are designed to continue functioning properly after an ESD occurrence without any latching.

The MAX3243E devices have three specified ESD limits on the driver outputs and receiver inputs, with respect to GND:

- ± 15 -kV Human Body Model (HBM)
- ± 15 -kV IEC61000-4-2, Air-Gap Discharge (formerly IEC1000-4-2)
- ± 8 -kV IEC61000-4-2, Contact Discharge

ESD Test Conditions

ESD testing is stringently performed by TI, based on various conditions and procedures. Please contact TI for a reliability report that documents test setup, methodology, and results.

Human Body Model (HBM)

The Human Body Model of ESD testing is shown in Figure 7, while Figure 8 shows the current waveform that is generated during a discharge into a low impedance. The model consists of a 100-pF capacitor, charged to the ESD voltage of concern, and subsequently discharged into the DUT through a 1.5k- Ω resistor.

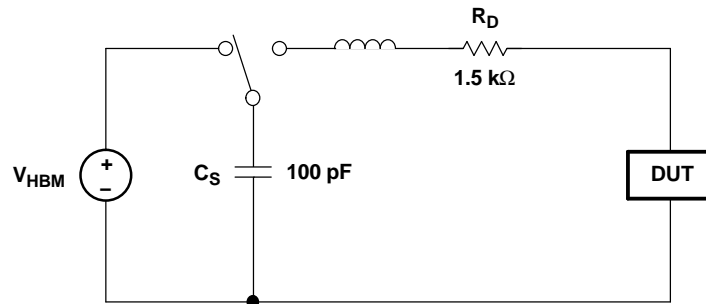


Figure 7. HBM ESD Test Circuit

APPLICATION INFORMATION

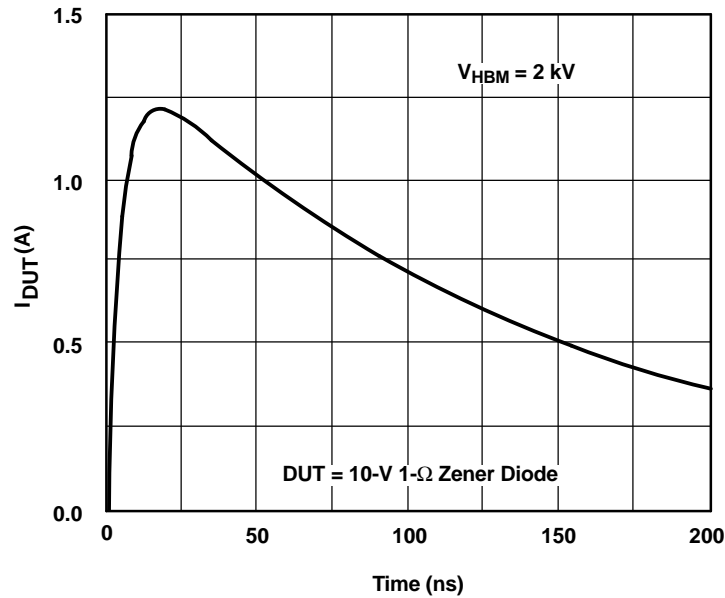


Figure 8. Typical HBM Current Waveform

IEC61000-4-2 (Formerly Known as IEC1000-4-2)

Unlike the HBM, MM, and CDM ESD tests that apply to component level integrated circuits, the IEC61000-4-2 is a system-level ESD testing and performance standard that pertains to the end equipment. The MAX3243E is designed to enable the manufacturer in meeting the highest level (Level 4) of IEC61000-4-2 ESD protection with no further need of external ESD protection circuitry. The more stringent IEC test standard has a higher peak current than the HBM, due to the lower series resistance in the IEC model.

Figure 9 shows the IEC61000-4-2 model, and Figure 10 shows the current waveform for the corresponding ± 8 -kV Contact-Discharge (Level 4) test. This waveform is applied to a probe that has been connected to the DUT. On the other hand, the corresponding ± 15 -kV (Level 4) Air-Gap Discharge test involves approaching the DUT with an already energized probe.

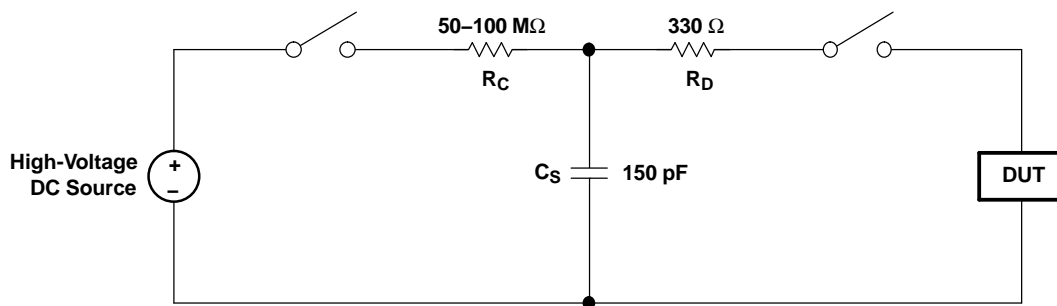


Figure 9. Simplified IEC61000-4-2 ESD Test Circuit

APPLICATION INFORMATION

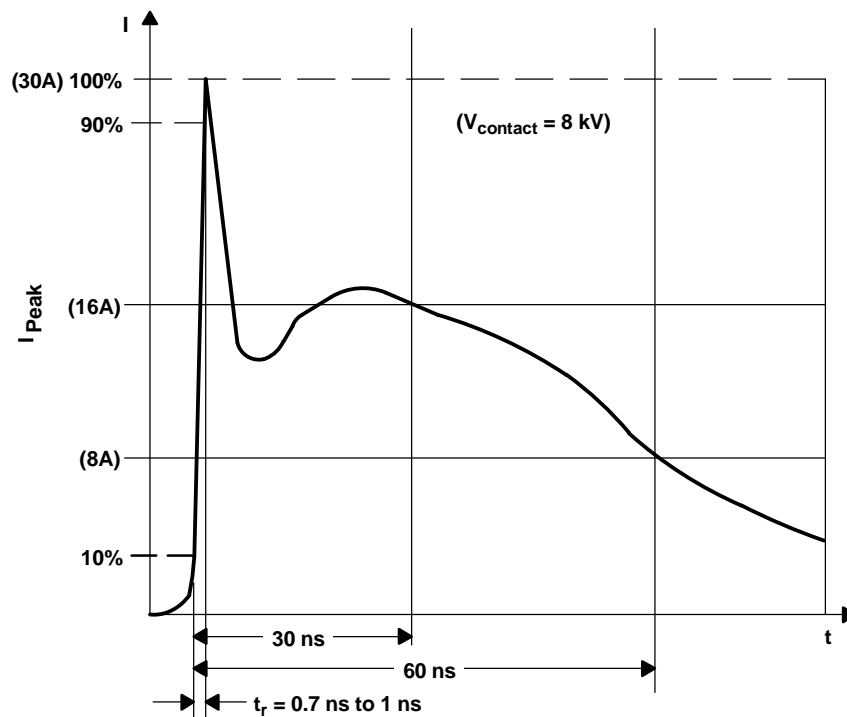


Figure 10. Typical Current Waveform of IEC61000-4-2 ESD Generator

Machine Model

The Machine Model (MM) ESD test applies to all pins using a 200-pF capacitor with no discharge resistance. The purpose of the MM test is to simulate possible ESD conditions that can occur during the handling and assembly processes of manufacturing. In this case, ESD protection is required for all pins, not just RS-232 pins. However, after PC board assembly, the MM test is no longer as pertinent to the RS-232 pins.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
MAX3243ECDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECDBE4	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECDBRE4	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECPWE4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECPWRE4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243ECRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
MAX3243ECRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
MAX3243EIDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIDW	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIDWR	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIPWE4	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIPWRE4	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
MAX3243EIRHBR	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
MAX3243EIRHBRG4	ACTIVE	QFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

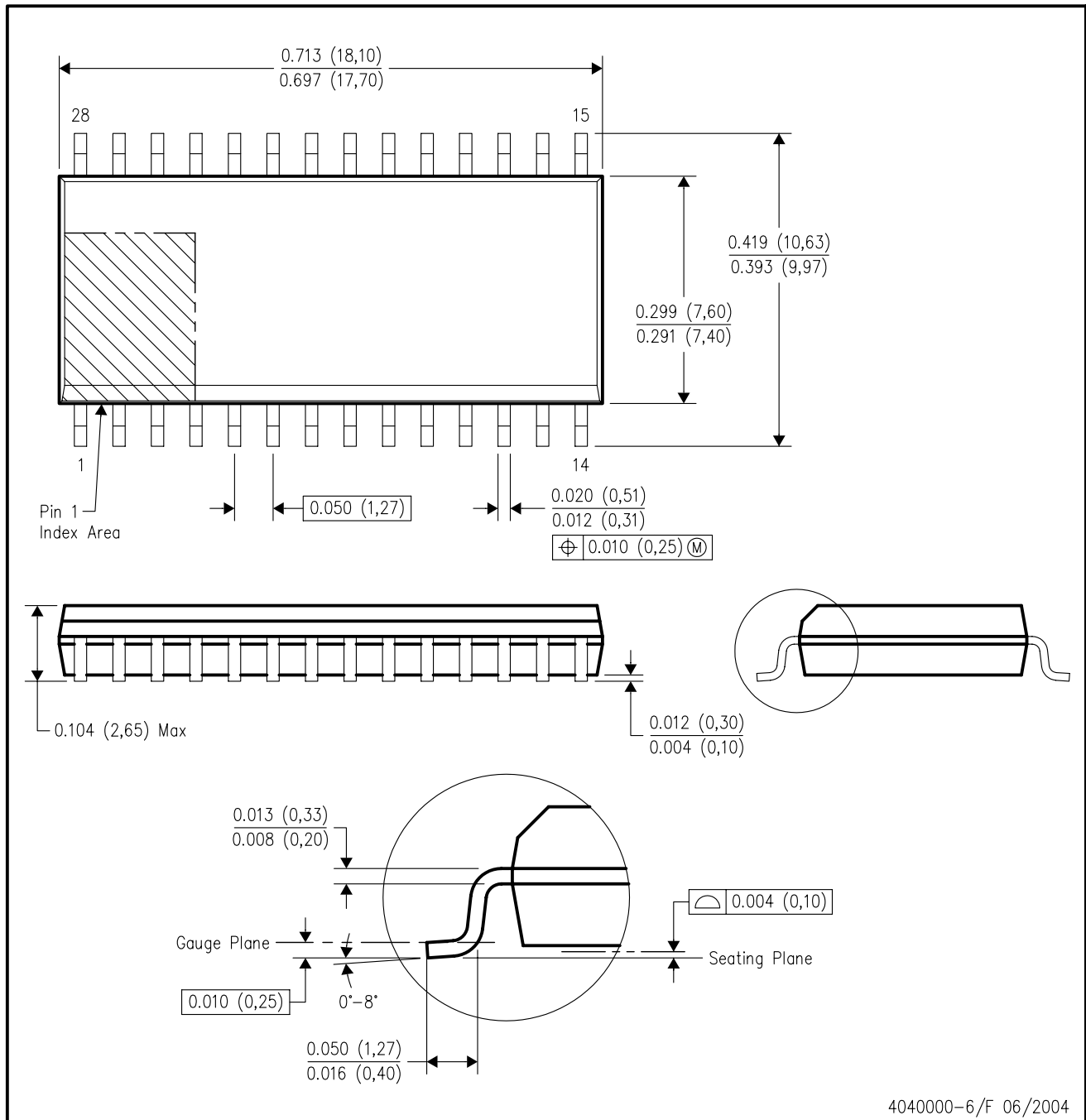
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DW (R-PDSO-G28)

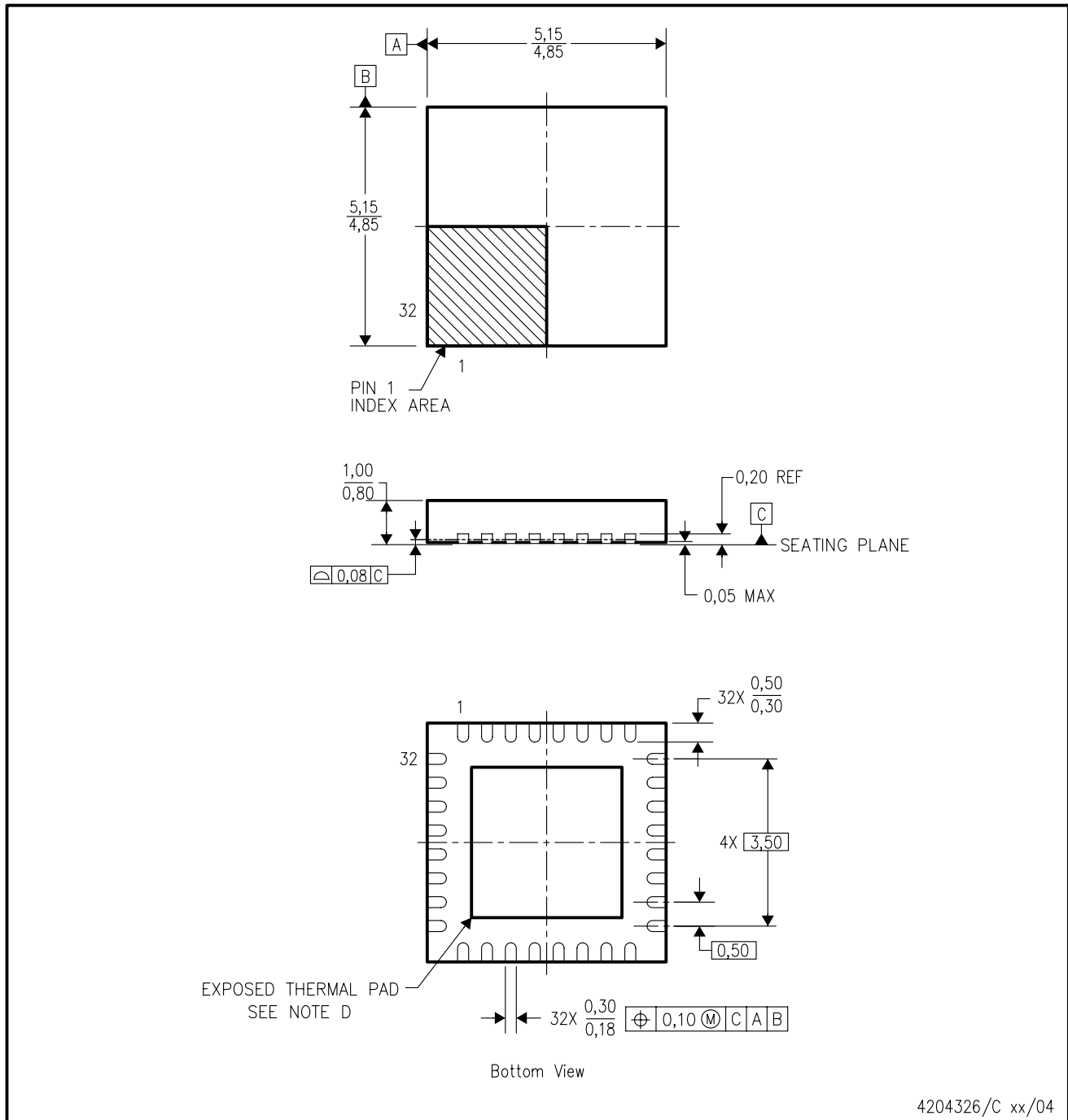
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AE.

RHB (S-PQFP-N32)

PLASTIC QUAD FLATPACK



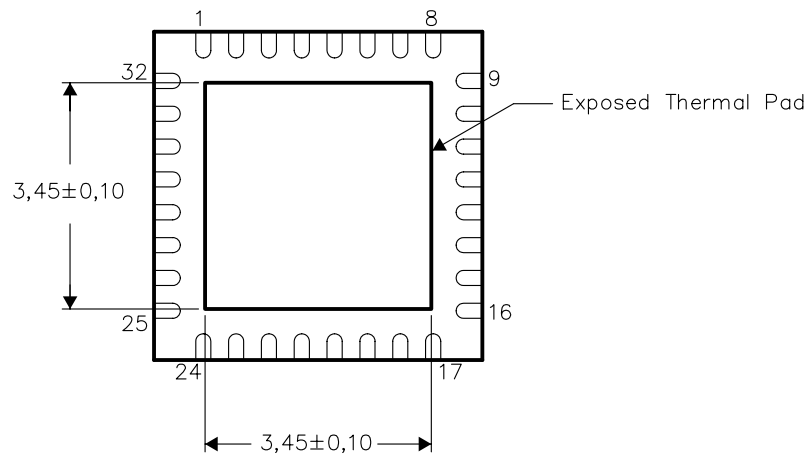
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) Package configuration.
 - D. The Package thermal pad must be soldered to the board for thermal and mechanical performance. See product data sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

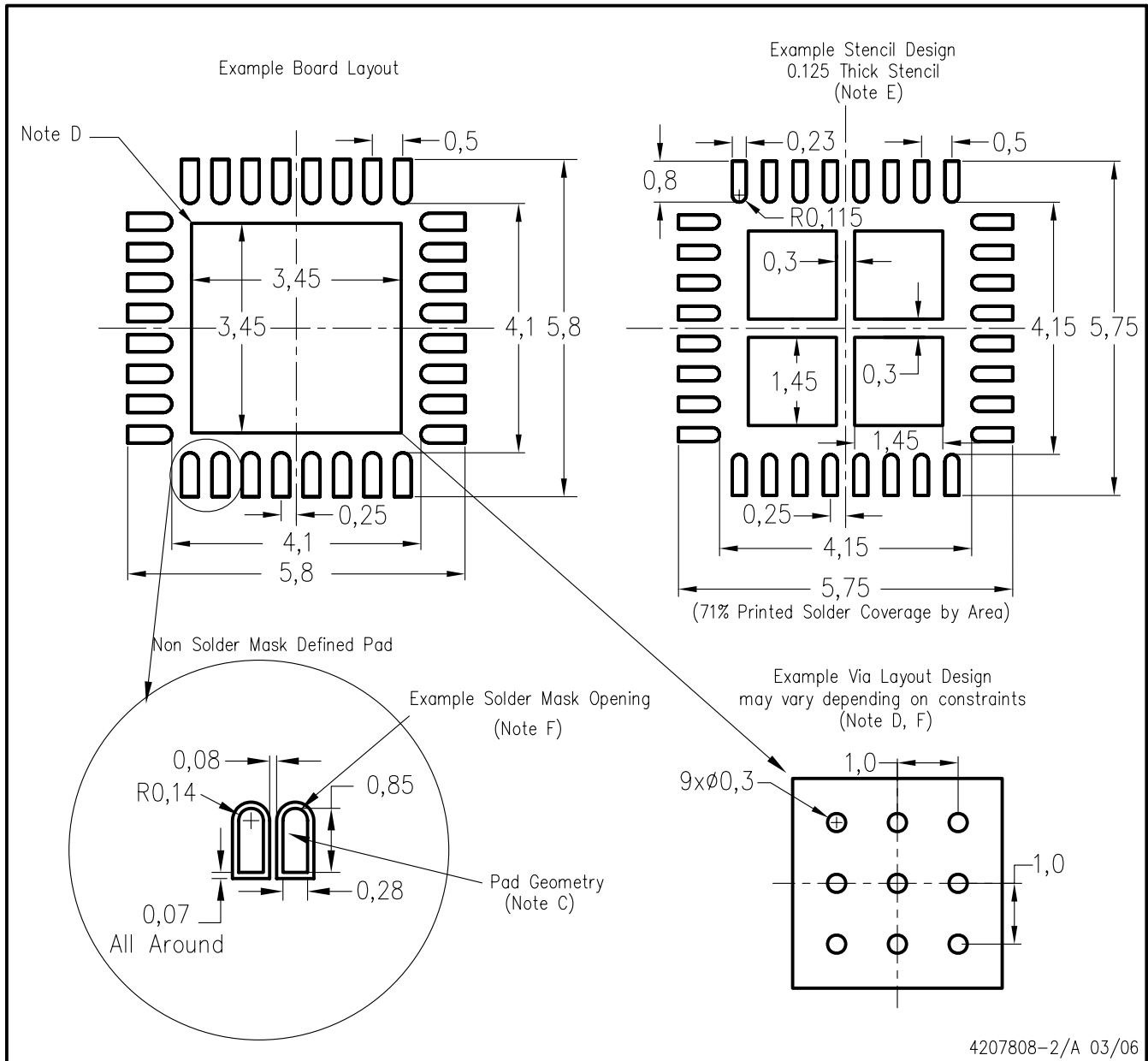


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RHB (S-PQFP-N32)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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